SED1280

CMOS DOT MATRIX LCD CONTROLLER DRIVER

■ DESCRIPTION

The SED1280 is a character LCD controller-driver, capable of driving displays as large as 2 lines of 8 characters (5 × 8 pixels), with minimum external components.

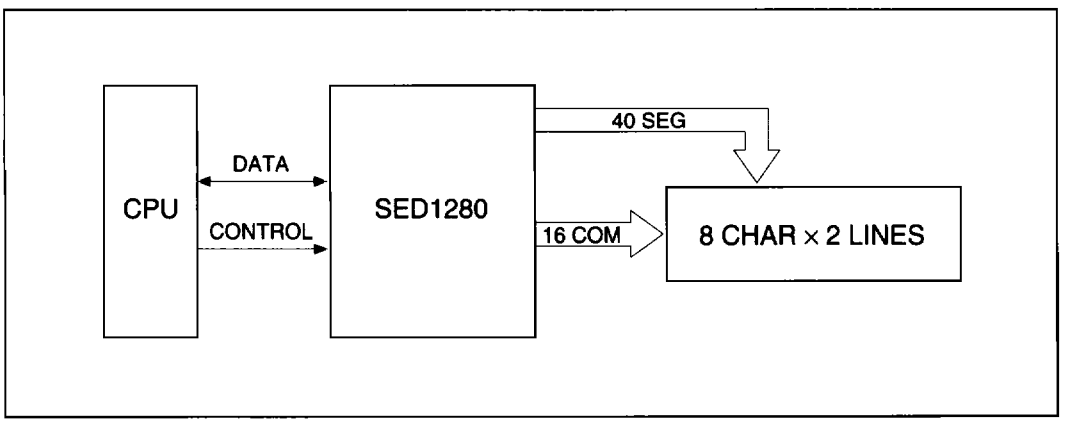
The SED1280 has an internal CGROM consisting of 240 characters (5 × 7) plus the underline cursor, JIS, ASCII, and eight user-programmable characters in RAM.

The SED1280 has 40 segment output and 16 common output built-in. Thus, one chip is capable of displaying up to 16 characters. The SED1280 can display one line of 48 characters using an SED1681F (80-bit output) as an expansions segment driver, since the driver is provided with the SED1278F core. Also, the LSI features serial data interface to interface to MPU, key matrix controller, LED controller and input/output ports. These features are suitable for applications such as facsimile machines.

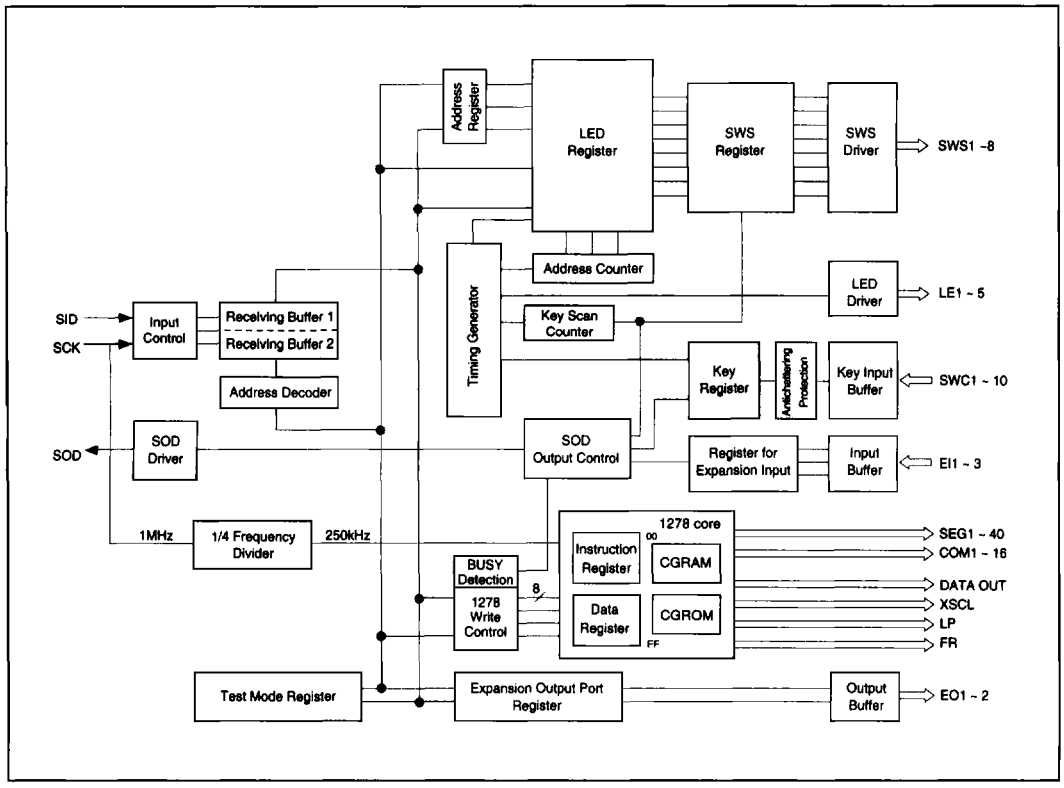
■ FEATURES

- Low-power CMOS technology
- 40 segment output
- 16 common output
- Duty ..... 1/8 or 1/16 (set by command)
- Serial data interface, TTL compatible
- Two-frame AC drive waveform
- CGROM ..... 240 characters
- CGRAM ..... 8 characters
- Display data RAM .... 80 × 8 bits (80 characters)
- Recommended expansion segment driver:
  SED1181 (64-bit output)
  SED1681 (80-bit output)
- Key matrix scan controller:
  Capable of controlling 8 × 10 keys
- LED controller:
  Capable of controlling 5 × 8 LEDs
- I/O ports ..... 3 input, 2 output
- Built-in RC oscillator
- Built-in LCD driver voltage-divider network
- TTL compatible CPU interface
- Supply voltage: .. Logic ..... 4.5V to 5.5V
  LCD ..... 3.5V to 5.5V
- Package: ..... QFP5-100 pins (F_{OA}, F_{OB}, F_{OC})
  Al pad (D_{OA}, D_{OB}, D_{OC})

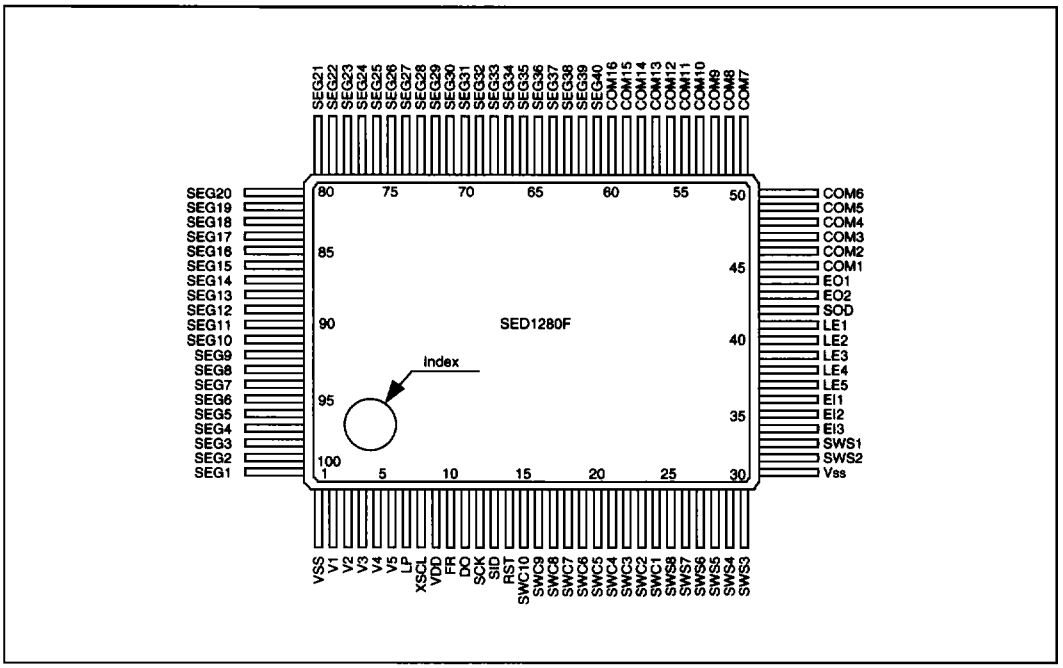
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT


SEG21 SEG22 SEG23 SEG24 SEG25 SEG26 SEG27 SEG28 SEG29 SEG30 SEG31 SEG32 SEG33 SEG34 SEG35 SEG36 SEG37 SEG38 SEG39 SEG40 COM16 COM15 COM14 COM13 COM12 COM11 COM10 COM9 COM8 COM7
SEG20 SEG19 SEG18 SEG17 SEG16 SEG15 SEG14 SEG13 SEG12 SEG11 SEG10 SEG9 SEG8 SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1
80 75 70 65 60 55 50
85
45
90
40
95
35
100 1 5 10 15 20 25 30
SED1280F
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COM6 COM5 COM4 COM3 COM2 COM1 EO1 EO2 SOD LE1 LE2 LE3 LE4 LE5 EI1 EI2 EI3 SWS1 SWS2 Vss
VSS V1 V2 V3 V4 V5 LP XSCL VDD FR DO SCK SID RST SWC10 SWC9 SWC8 SWC7 SWC6 SWC5 SWC4 SWC3 SWC2 SWC1 SWS8 SWS7 SWS6 SWS5 SWS4 SWS3

■ PIN DESCRIPTION

Pin Name	I/O	Pull-up resistance	Functions	Number of terminals
SID	I	None	Serial data input	1
SOD	O	—	Serial data output. (For use input status of expansion input port (EI) and key input port (SWC))	1
SCK	I	None	1 MHz system clock input. System clock synchronized serial data input/output, LCD display and key input control.	1
Segment driver signal output pin for expansion				
LP	O	—	Data latching pulse	1
XSCL	O	—	Data transfer clock	1
FR	O	—	LCD AC driving signal	1
D0	O	—	Serial data	1
LCD AC drive pin				
COM1 to COM16	O	—	Common output	16
SEG1 to SEG40	O	—	Segment output	40
V1 to V5	Power supply	—	LCD driving power	5
Key/LED control pin				
SWS1 to SWS8	O	—	Output port for commonly driving key and LED by time sharing	8
LE1 to LE5	O	—	LED driver	5
SWC1 to SWC10	I	Existing	Key input port	10
Expansion input port				
EI1 to EI3	I	—	Input port, 3 input port	3
Expansion output port				
EO1 to EO2	O	—	Output port, 2	2
RST	I	—	System reset	1
Power supply pin				
V_{DD}	Power supply	—	+5V	1
V_{SS}	Power supply	—	0V (GND)	2