

**CCSSC14N40A10**  
**Solidtron™**

N-Type Semiconductor Discharge Switch,  
 ThinPak™  
 Data Sheet (Rev 0 - 07/16/08)

**Description**

This current controlled Solidtron™ (CCS) discharge switch is an n-type Thyristor in a high performance single chip module. The device gate is similar to that found on a traditional GTO Thyristor.

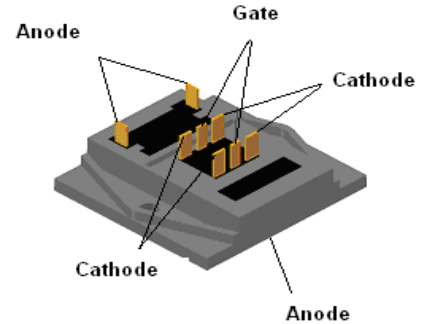
The CCS features the high peak current capability and low On-state voltage drop common to SCR thyristors combined with high di/dt capability. This semiconductor is intended to be a solid state replacement for spark or gas type devices commonly used in pulse power applications.

This single chip package contains a ThinPak™ which is a perforated, metalized ceramic substrate attached to the silicon using 302°C solder. The ThinPak™ is attached to a metal baseplate using 60Pb40Sn eutectic solder. It's small size and low profile make it extremely attractive for high di/dt applications where stray series inductance must be kept to a minimum.

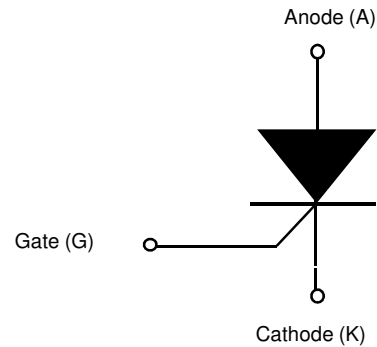
**Features**

- 4000V Peak Off-State Voltage
- 10 kA Repetitive I<sub>pk</sub> Capability
- 30 KA/uS di/dt Capability
- Low On-State Voltage
- Low trigger current
- Low Inductance Package

**Single Size - 12 Chip Module**



**Schematic Symbol**



**Absolute Maximum Ratings**

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	V <sub>DRM</sub>	4	kV
Peak Reverse Voltage	V <sub>RRM</sub>	-5	V
Off-State Rate of Change of Voltage Immunity*	dv/dt	1	kV/uSec
Continuous Anode Current at T <sub>j</sub> = 125 °C	I <sub>A110</sub>	100	A
Repetitive Peak Anode Current (Pulse Width=10uSec)	I <sub>ASM</sub>	10.0	kA
Nonrepetitive Peak Anode Current (Pulse Width=10uSec)	I <sub>ASM</sub>	14	kA
Rate of Change of Current	dI/dt	30	kA/uSec
Peak Gate Current (1 uS)	I <sub>Gpk</sub>	100	A
Max. Reverse Gate-Cathode Voltage	V <sub>GR</sub>	-9	V
Maximum Junction Temperature	T <sub>JM</sub>	125	°C

This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

5,521,436	5,446,316	5,105,536	5,209,390	4,958,211	5,206,186	4,857,983	5,082,795	4,644,637
5,585,310	5,557,656	5,777,346	5,139,972	5,111,268	5,757,036	4,888,627	4,980,741	4,374,389
5,248,901	5,564,226	5,446,316	5,103,290	5,260,590	5,777,346	4,912,541	4,941,026	4,750,666
5,366,932	5,517,058	5,577,656	5,028,987	5,350,935	5,995,349	5,424,563	4,927,772	4,429,011
5,497,013	4,814,283	5,473,193	5,304,847	5,640,300	4,801,985	5,399,892	4,739,387	5,293,070
5,532,635	5,135,890	5,166,773	5,569,957	5,184,206	4,476,671	5,468,668	4,648,174	

**Preliminary Data Sheet** - Product Status : First Production : This data sheet contains preliminary data . Supplementary data will be published at a later date. Silicon Power reserves the right to make changes at any time without notice.

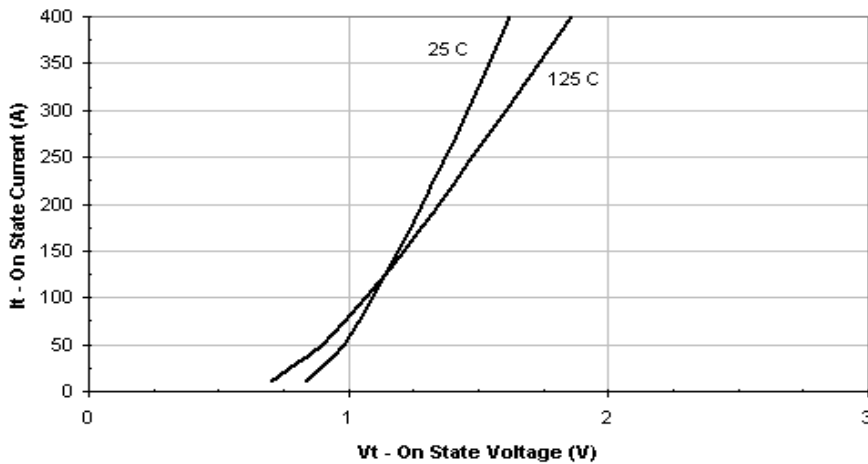
\* Requires a 10 ohm gate to cathode shorting resistor.

Performance Characteristics		T <sub>j</sub> =25°C unless otherwise specified		Measurements			
Parameters	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	V <sub>DR</sub>	V <sub>GK</sub> =0V, I <sub>A</sub> =1mA		4			kV
Anode-Cathode Off-State Current	I <sub>D</sub>	V <sub>GK</sub> =0V, V <sub>AK</sub> =4000V	T <sub>J</sub> =25°C		<50	100	µA
			T <sub>J</sub> =125°C		100	800	µA
Turn-On Threshold Current	V <sub>GK(TH)</sub>	V <sub>AK</sub> =V <sub>GK</sub> , I <sub>AK</sub> =1mA, see Note 1			5		mA
Gate-Cathode Leakage Current	I <sub>GK(lkg)</sub>	V <sub>GK</sub> =0V, see Note 1				20	µA
Anode-Cathode On-State Voltage	V <sub>T</sub>	I <sub>T</sub> =400A I <sub>g</sub> = 500 mA	T <sub>J</sub> =25°C		1.7		V
			T <sub>J</sub> =125°C		1.9		V
Turn-on Delay Time	t <sub>D(ON)</sub>	0.75 µF Capacitor discharge			200		ns
Pk Rate of Change of Current (measured)	di/dt	V <sub>AK</sub> = 3.95 kV T <sub>J</sub> =25°C			30		kA/us
Peak Anode Current	I <sub>P</sub>	R <sub>gk</sub> = 10 ohms, L <sub>s</sub> = 90 nH			10		kA
		Gate di/dt = 100 A/us					

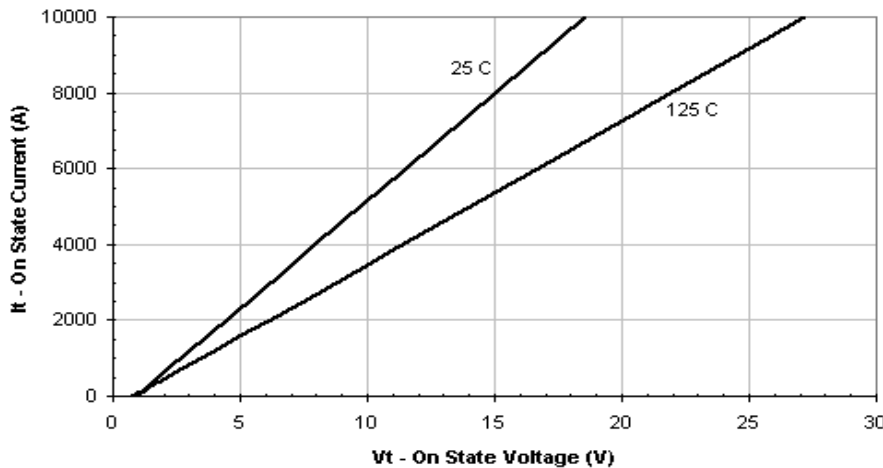
Notes:

1. Measurements made with a 10 Ohm shorting resistor connected between the gate and cathode.

**Typical Performance Curves** (unless otherwise specified)

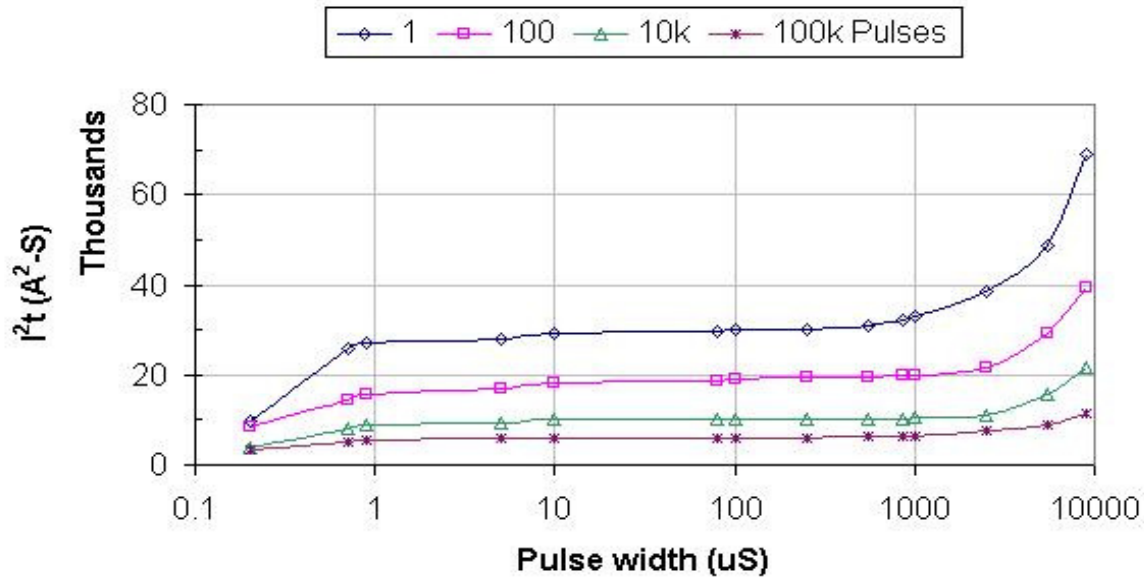


**Figure 1.**  
 Measured Low current  
 On-State Characteristics.



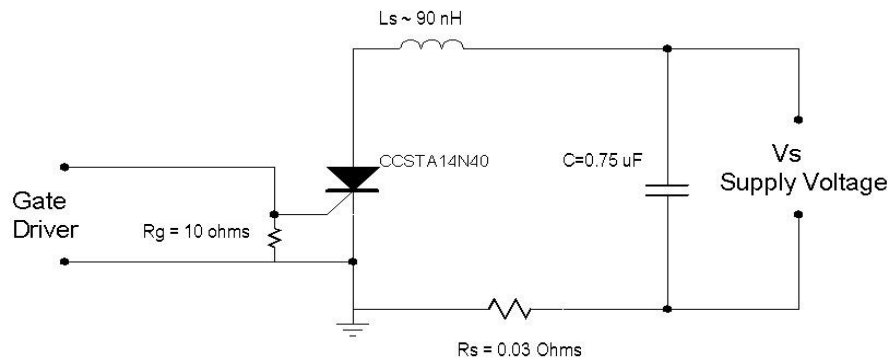
**Figure 2.**  
 Predicted high current  
 On-State Characteristics.

**Typical Performance Curves** (Continued)

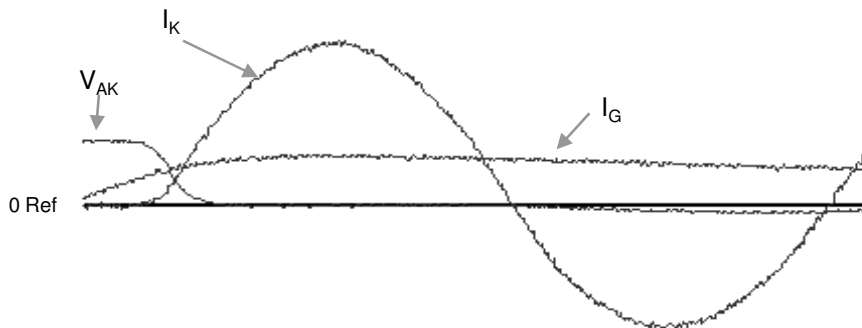


**Figure 3.** Predicted  $I^2t$  data for various number of discharge cycles. Pulses are assumed rectangular. The device junction temperature  $T_j$  is assumed to be at 25°C before each discharge event.

**Test Circuit**



- $L_{SERIES(TOTAL)}$  is calculated using  $1 / (f 2\pi)^2 C$  where  $f$  = frequency of  $I_A$  when using CCSTA14N40 for circuit set up and calibration.
- $R_{SENSE}$  is a calibrated Current Viewing Resistor (CVR)



- The waveform shown is representative of one produced using a very low inductance circuit (<100nH) as shown in the circuit diagram using the CCSTA14N40 Solidtron. The supply voltage ( $V_s$ ) in this example was 4kV.  $I_k$  peaked at 10kA and the peak gate current  $I_g$  is 500mA.

**Figure 4.** Typical test circuit and waveforms.

**Application Notes**

**A1. Pulse Transformer Gating**

A preferred method of isolation, a pulse transformer may be used to predictably and reliably trigger the Thyristor. This gating method allows the user to easily connect the devices in parallel or series (See Fig. A1.2 for series example).

**Components (Fig. A1.1)**

**T<sub>1</sub>** - Method of electrically isolating the device from control circuitry. Pulse X-former insulation characteristic must be selected based on application requirements.

**R<sub>1</sub>** (or **R<sub>GK</sub>**) - Serves as a keep-off resistor, shunting dv/dt induced, capacitively coupled Anode-Gate current to the Cathode. The lower the value of R<sub>1</sub>, the better the dv/dt immunity of the sub-circuit. In the event R<sub>1</sub> must be increased to the point where its resistance compromises the dv/dt requirement of the application, a low voltage capacitor (.1-.2uF) may be placed in parallel to provide a more responsive shunt path; however, the added capacitance will require more charge be delivered to satisfy the turn-on requirements outlined in the simplified theory of operation.

**D<sub>1</sub> & D<sub>2</sub>** - Current steering diodes. Reverse gate current increases the impedance of the device ("attempted turn-off"). Reverse gate current experienced during a high current discharge event may permanently damage the device. D<sub>1</sub> restricts the direction of current flow through the secondary while D<sub>2</sub> provides a "free-wheeling" or holding path to the gate.

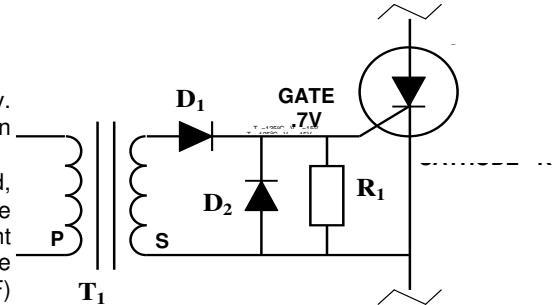
It is highly recommended that the components listed above, specifically R<sub>1</sub> and D<sub>2</sub> be placed in as close physical/electrical proximity to the device as the application will allow. Parasitic inductance in series with the Gate to Cathode shunt path will also compromise the dv/dt immunity of the device.

**Theory of Operation (Refer to Fig. A1.1)**

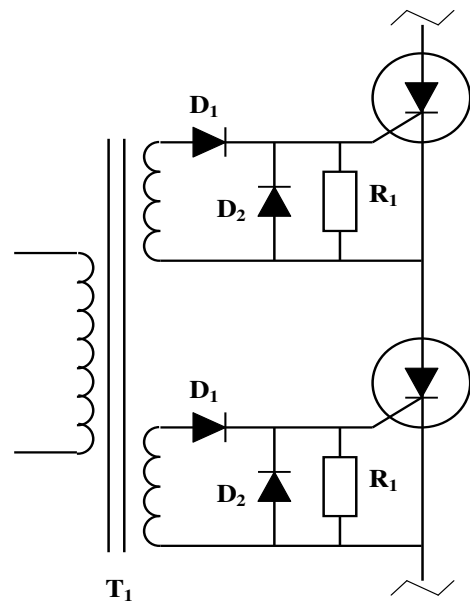
A current pulse supplied to the primary of T<sub>1</sub> induces a current into the secondary of T<sub>1</sub>. Current supplied by the T<sub>1</sub> secondary forward biases D<sub>1</sub> supplying current through R<sub>1</sub>; thus, developing voltage across R<sub>1</sub> until the gate of the Thyristor is forward biased (~0.7V). Current is then supplied to the Gate of the Thyristor until turn-on (latched-on) is achieved. Following the discharge event, once the Thyristor current reaches zero and its stored charge is cleared (Storage Time) the circuit is reset and Anode voltage may be reapplied.

**Example:** Turn-on will occur with R<sub>1</sub>=5 ohms, I<sub>T1-S</sub> => 140mA  
 It is recommended that T<sub>1</sub> secondary current (I<sub>T1-S</sub>) => 0.7V / R<sub>1</sub> be supplied for approximately 2uSec. Device turn-on delay (T<sub>D-ON</sub>) is typically less than 200nSec.

Although I<sub>T1-S</sub> = 0.7V / R<sub>1</sub> is sufficient to turn the device on, we typically recommend, where possible, I<sub>T1-S</sub> => >500mA, Pulse Duration => 5uSec with R<sub>1</sub>= 10 ohms.



**Figure A1.1**  
**Basic Pulse X-Former Gating Circuit**



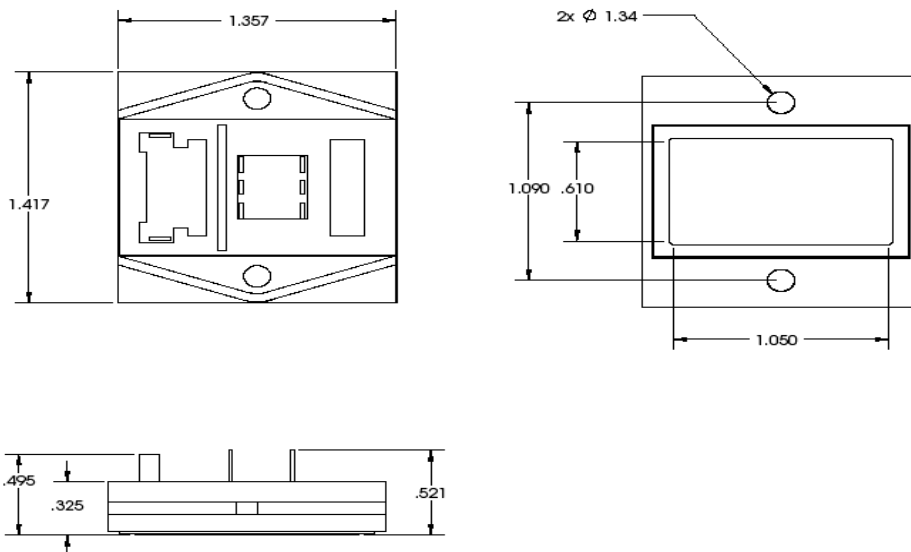
**Figure A1.2**  
**Series Connection Pulse X-Former Gating**

**Packaging and Handling**

1. Use thermal grease to mount device to cold plate.
2. Consult factory for mounting torque.
3. Do not exceed 175°C device body temperature when soldering leads of the package or internal package gradation may result.
4. 'ATTENTION OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE DEVICES IN ALL ASSEMBLY AND TEST AREAS'
5. Shorting resistor RGK is application specific. It can control the gate drive requirements and some device properties. However, RGK = 10 Ohms satisfies most application requirements.
6. All metal surfaces are flash gold over nickel plating for solderability.



**Dimensions**



**Revision History**

Rev	Date	EA #	Nature of Change
0	07-16-2008	04242009-NB-0018	Initial Issue