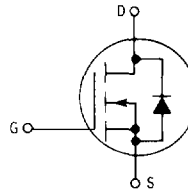


*Designer's Data Sheet*  
**Power Field Effect Transistor**  
**N-Channel Enhancement-Mode**  
**Silicon Gate TMOS**

**MTH40N08**  
**MTH40N10**  
**MTH40N05**  
**MTH40N06**

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data —  $I_{DSS}$ ,  $V_{DS(on)}$ ,  $V_{GS(th)}$  and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



**TMOS POWER FETs**  
**and AMPERES**  
 $r_{DS(on)} = 0.04 \text{ OHM}$   
**80 and 100 VOLTS**  
 $r_{DS(on)} = 0.028 \text{ OHM}$   
**50 and 60 VOLTS**



**CASE 340-02**  
**TO-218AC**

**MAXIMUM RATINGS**

Rating	Symbol	MTH				Unit
		40N05	40N06	40N08	40N10	
Drain-Source Voltage	$V_{DSS}$	50	60	80	100	Vdc
Drain-Gate Voltage ( $R_{GS} = 1 \text{ M}\Omega$ )	$V_{DGR}$	50	60	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ( $t_p \leq 50 \mu\text{s}$ )	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 40$				Vdc Vpk
Drain Current Continuous Pulsed	$I_D$ $I_{DM}$	40 140		40 120		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	150 1.2				Watts W/°C
Operating and Storage Temperature Range	$T_J, T_{stg}$	-65 to 150				°C

**THERMAL CHARACTERISTICS**

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.833 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	275	°C

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTH40N08, 10, 05, 06

**ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Drain-Source Breakdown Voltage ( $V_{GS} = 0, I_D = 0.25 \text{ mA}$ )	$V_{(BR)DSS}$			Vdc
MTH40N05		50	—	
MTH40N06		60	—	
MTH40N08		80	—	
MTH40N10		100	—	
Zero Gate Voltage Drain Current ( $V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$ ) ( $V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$ )	$I_{DSS}$	—	10	$\mu\text{Adc}$
Gate-Body Leakage Current, Forward ( $V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSSF}$	—	500	nAdc
Gate Body Leakage Current, Reverse ( $V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSSR}$	—	500	nAdc
<b>ON CHARACTERISTICS</b>				
Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1 \text{ mA}$ ) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ( $V_{GS} = 10 \text{ Vdc}, I_D = 20 \text{ Adc}$ )	$r_{DS(on)}$	—	0.028 0.04	Ohm
MTH40N05/06				
MTH40N08/10				
Drain-Source On-Voltage ( $V_{GS} = 10 \text{ V}$ ) ( $I_D = 40 \text{ Adc}$ ) ( $I_D = 20 \text{ Adc}, T_J = 100^\circ\text{C}$ ) ( $I_D = 40 \text{ Adc}$ ) ( $I_D = 20 \text{ Adc}, T_C 100^\circ\text{C}$ )	$V_{DS(on)}$	—	1.4 1.12 2 1.6	Vdc
MTH40N05/06				
MTH40N05/06				
MTH40N08/10				
MTH40N08/10				
Forward Transconductance ( $V_{DS} = 15 \text{ V}, I_D = 20 \text{ A}$ )	$g_{FS}$	10	—	mhos
<b>DYNAMIC CHARACTERISTICS</b>				
Input Capacitance	( $V_{DS} = 25 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$ ) See Figure 8	$C_{iss}$	—	5000
Output Capacitance		$C_{oss}$	—	2500
Reverse Transfer Capacitance		$C_{rss}$	—	1000
<b>SWITCHING CHARACTERISTICS</b> ( $T_J = 100^\circ\text{C}$ )				
Turn-On Delay Time	( $V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50 \text{ ohms}$ ) See Figure 16	$t_{d(on)}$	—	100
Rise Time		$t_r$	—	330
Turn-Off Delay Time		$t_{d(off)}$	—	330
Fall Time		$t_f$	—	360
Total Gate Charge	( $V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = \text{Rated } I_D, V_{GS} = 10 \text{ Vdc}$ ) See Figure 15	$Q_g$	105 (Typ)	120
Gate-Source Charge		$Q_{gs}$	74 (Typ)	—
Gate-Drain Charge		$Q_{gd}$	31 (Typ)	—
<b>SOURCE DRAIN DIODE CHARACTERISTICS</b>				
Forward On-Voltage	( $I_S = \text{Rated } I_D,$ $V_{GS} = 0$ )	$V_{SD}$	2.2 (Typ)	3
Forward Turn-On Time		$t_{on}$	Limited by stray inductance	
Reverse Recovery Time		$t_{rr}$	75 (Typ)	—
<b>INTERNAL PACKAGE INDUCTANCE</b>				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	$L_D$	4 (Typ) 5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	$L_S$	10 (Typ)	—	

TYPICAL CHARACTERISTICS

MTH40N05, MTH40N06

FIGURE 1 — ON-REGION CHARACTERISTICS

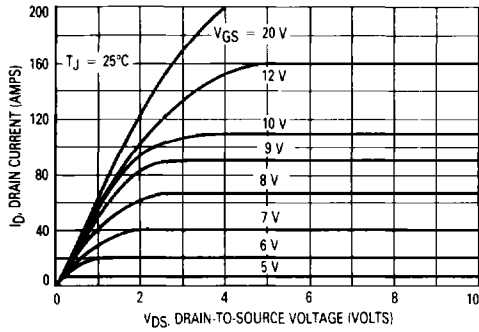


FIGURE 3 — TRANSFER CHARACTERISTICS

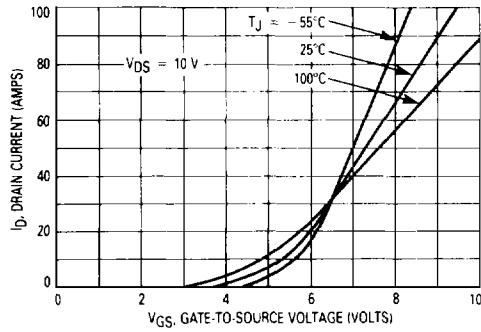
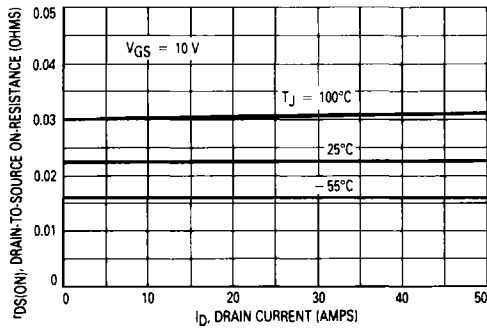


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT



MTH40N08, MTH40N10

FIGURE 2 — ON-REGION CHARACTERISTICS

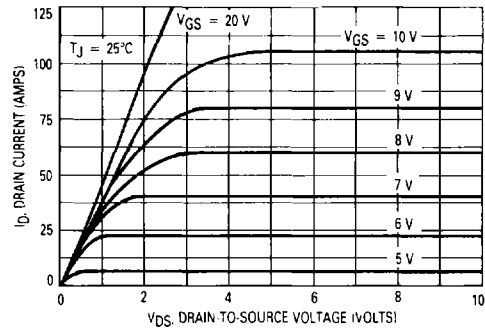


FIGURE 4 — TRANSFER CHARACTERISTICS

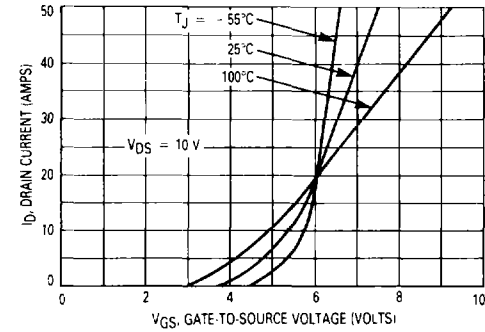
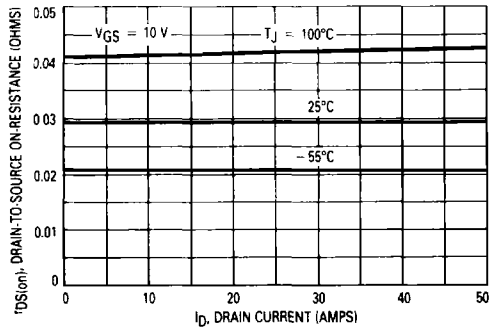


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

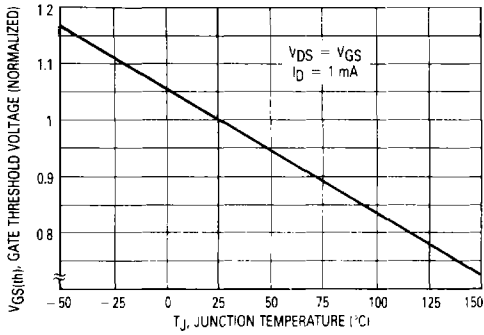


FIGURE 8 — CAPACITANCE VARIATION

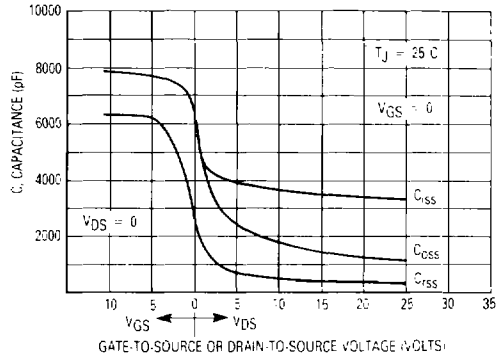


FIGURE 9 — BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

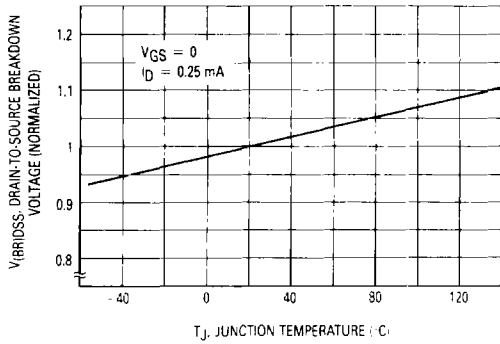


FIGURE 10 — ON-RESISTANCE VARIATION WITH TEMPERATURE

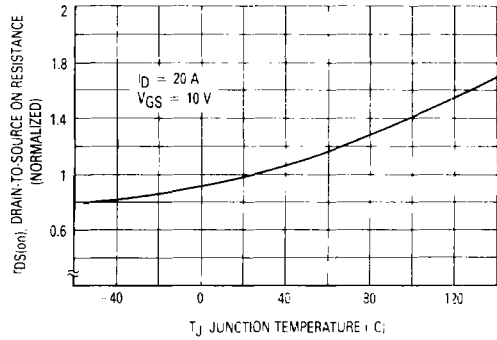
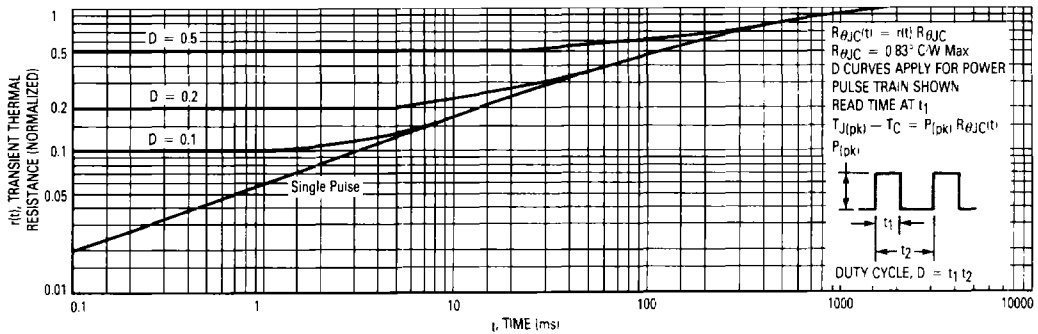


FIGURE 11 — THERMAL RESPONSE



3

# MTH40N08, 10, 05, 06

## SAFE OPERATING AREA INFORMATION

### MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

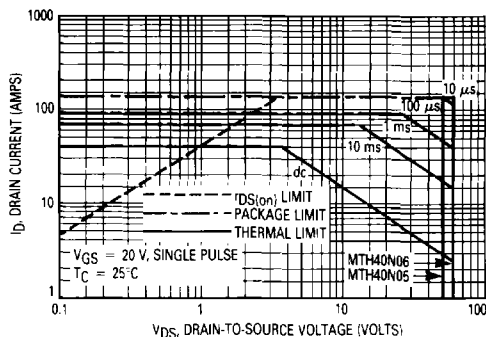
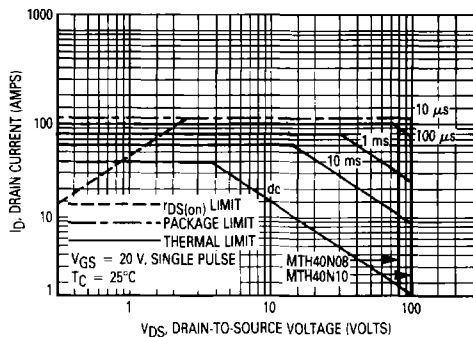


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



### FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

### SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current,  $I_{DM}$  and the breakdown voltage,  $V_{(BR)DSS}$ . The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(\max) - T_C}{R_{\theta JC}}$$

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

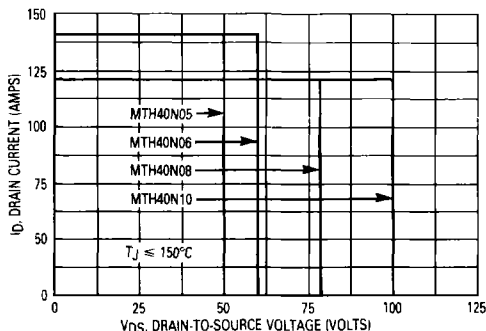


FIGURE 15 — STORED CHARGE versus GATE-TO-SOURCE VOLTAGE

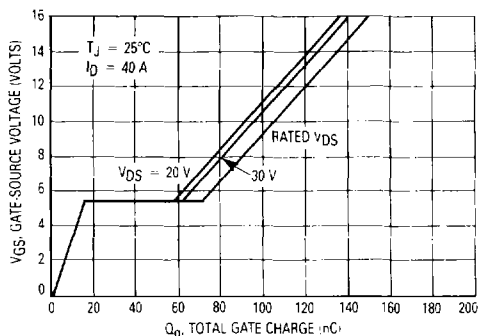


FIGURE 16 — RESISTIVE SWITCHING TIME VARIATION WITH GATE RESISTANCE

