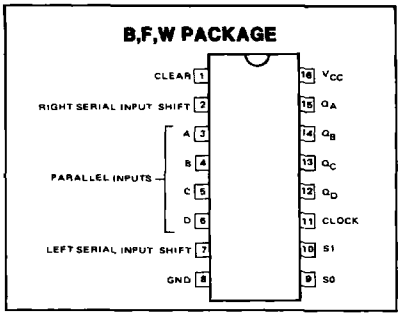
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
54S	F,W	74S	B

PIN CONFIGURATION



DESCRIPTION

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 45 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transistion of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the S54194/N74194 should be changed only while the clock input is high.

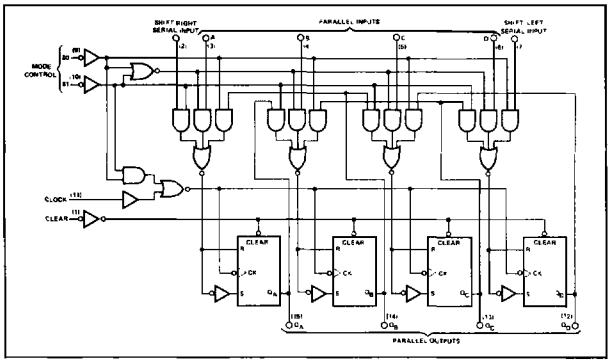
TRUTH TABLE

INPUTS										OUTPUTS			
	MODE			SERIAL		PARALLEL							
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

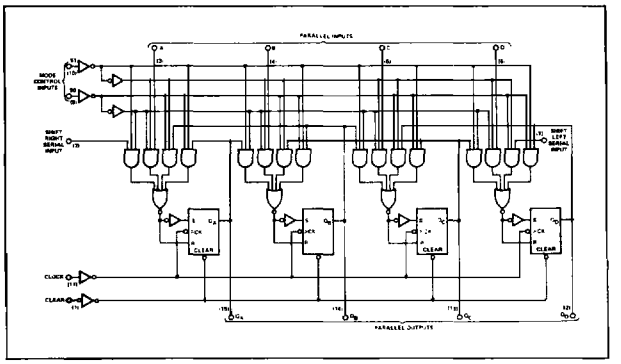
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d, = the level of steady state input at inputs A,B,C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock

LOGIC

BLOCK DIAGRAM (94)



BLOCK DIAGRAM (LS194, S194)



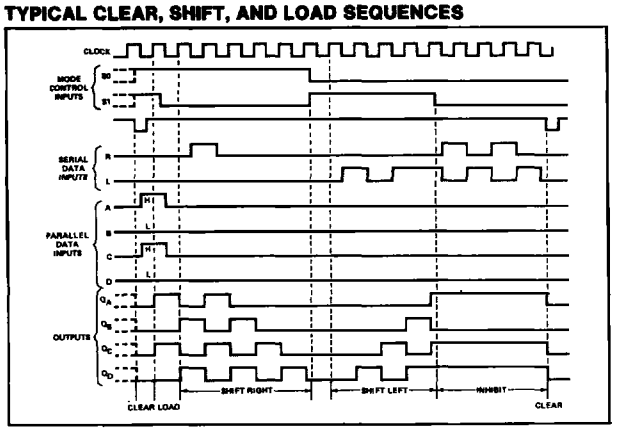
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Clock}	Clock frequency			25	36		25	36		70	105		MHz
t_w	Width of pulse			20			20						ns
	Clock									7			
	Clear									12			
t_{Setup}	Input setup time												
	Mode control			30			30↑			8			ns
	Serial, Parallel			20			20↑			5			
	Clear inactive			25			25↑			9			
t_{Hold}	Input hold time	Any		0			0↑			3			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock		7	14	22		14	22	4	8	12	ns
t_{PHL}	High-to-low			7	17	26		17	22	4	11	16.5	
t_{PHL}	High-to-low	Clear			19	30		19	30		12.5	18.5	

Load circuit and typical waveforms are shown at the front of section.

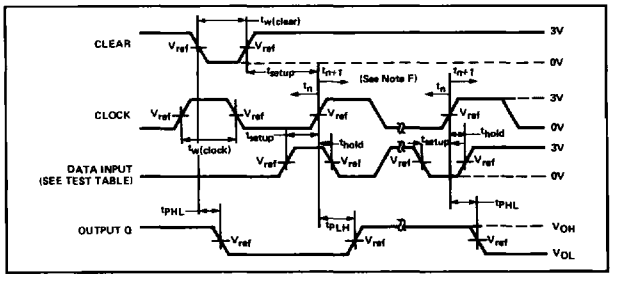
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5V	4.5V	Q_A at t_n+1
B	4.5V	4.5V	Q_B at t_n+1
C	4.5V	4.5V	Q_C at t_n+1
D	4.5V	4.5V	Q_D at t_n+1
L Serial Input	4.5V	0V	Q_A at t_n+4
R Serial Input	0V	4.5V	Q_D at t_n+4



VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ≤ MHz, $t_r \leq 15$ ns and $t_f \leq 6$ ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. A clear pulse is applied prior to each test.
E. $V_{ref} = 1.3V$.
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+4 with a functional test.
G. t_n = bit time before clocking transition.
t_n+1 = bit time after one clocking transition.
t_n+4 = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

LOGIC

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
54S	F,W	74S	B

DESCRIPTION

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

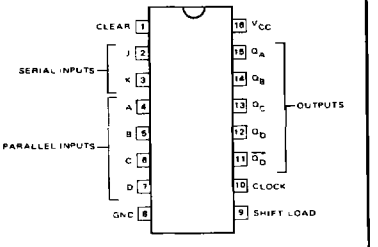
Parallel (Broadside) Load
Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

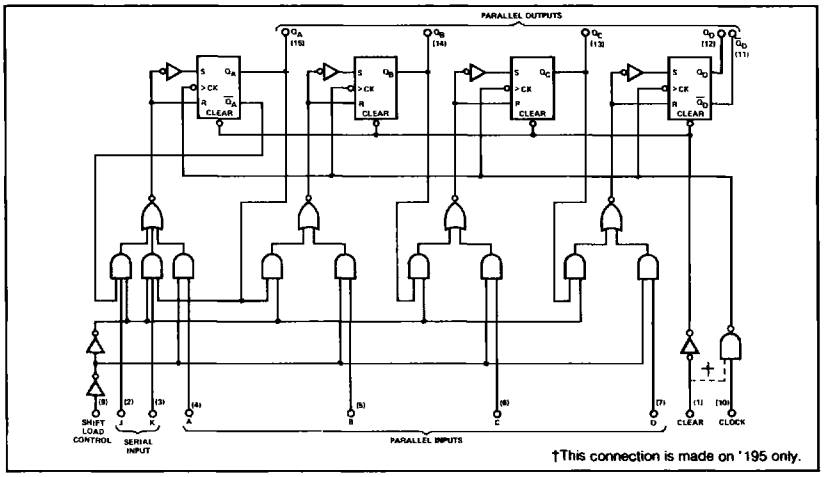
INPUTS									OUTPUTS				
			SERIAL		PARALLEL								
CLEAR	SHIFT/ LOAD	CLOCK	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d = the level of steady-state input at A,B,C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			30	39		30	39		70	105		MHz
$t_{w(Clock)}$	Width of clock input pulse			16			16			7			ns
$t_{w(Clear)}$	Width of clear input pulse			12			12			12			ns
t_{Setup}	Input setup time												
	Shift/Load			25			25↑			8			ns
	Serial/Parallel			15			15↑			5			
	Clear inactive			25			25↑			9			
$t_{Release}$	Shift/Load release time					10			10↑			6	ns
T_{Hold}	Input hold time	Any		0			0↑			3			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock		6	14	22		14	22		8	12	ns
t_{PHL}	High-to-low			7	17	26		17	26		11	16.5	
t_{PHL}	High-to-low	Clear			19	30		19	30		12.5	18.5	

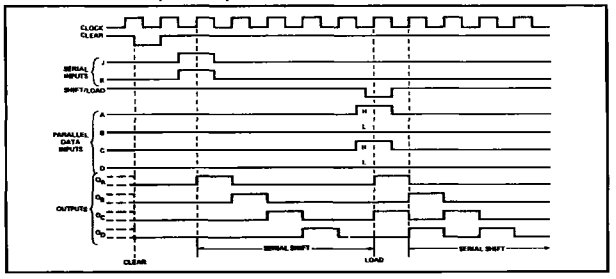
BLOCK DIAGRAM

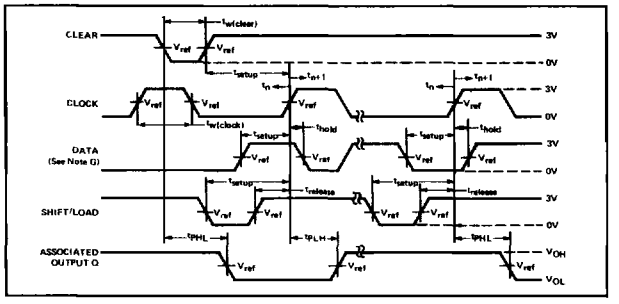


†This connection is made on '195 only.

PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES





VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leq$ 1 MHz
$t_r \leq 15$ ns and $t_f \leq 6$ ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. $V_{ref} \approx 1.3V$.

F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+4 with a functional test.

G. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.

H. t_n = bit time before clocking transition.
t_n+1 = bit time after one clocking transition.
t_n+4 = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES