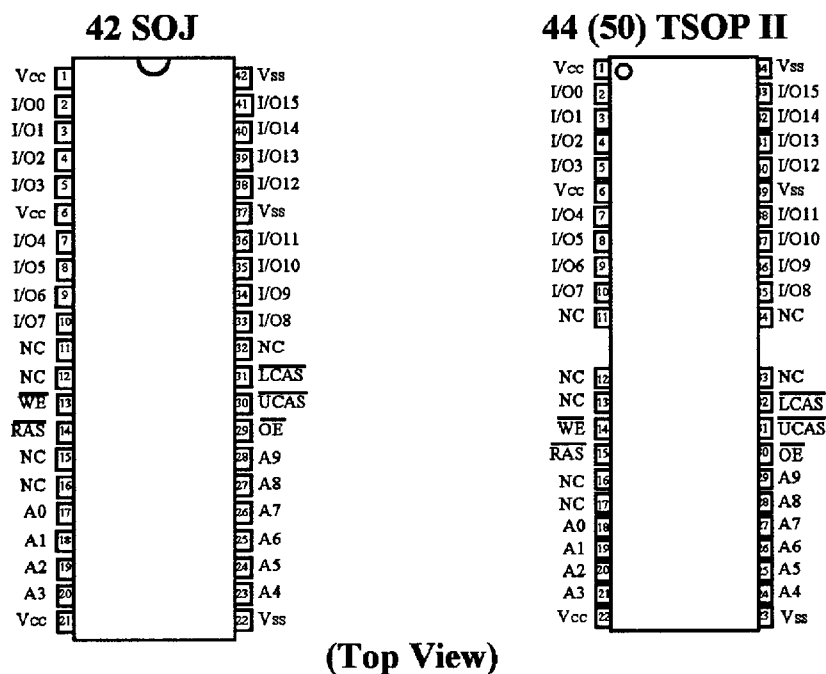


## Description

The GM71V(S)18163A/AL is the new generation dynamic RAM organized 1,048,576 words x 16 bit. GM71V(S)18163A/AL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)18163A/AL offers Extended Data Out (EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)18163A/AL to be packaged in standard 400 mil 42pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 3.3V  $\pm$  0.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

## Pin Configuration



## Features

- 1,048,576 Words x 16 Bit Organization
- Extended Data Out Mode Capability
- Single Power Supply (3.3V  $\pm$  0.3V)
- Fast Access Time & Cycle Time

(Unit: ns)

|                     | t <sub>TRAC</sub> | t <sub>CAC</sub> | t <sub>RC</sub> | t <sub>HPC</sub> |
|---------------------|-------------------|------------------|-----------------|------------------|
| GM71V(S)18163A/AL-7 | 70                | 18               | 124             | 30               |
| GM71V(S)18163A/AL-8 | 80                | 20               | 144             | 35               |

- Low Power  
Active : 540 / 468mW (MAX)  
Standby : 3.6mW (CMOS level : MAX)  
0.54mW (L-version : MAX)
- $\overline{\text{RAS}}$  Only Refresh,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh, Hidden Refresh Capability
- Self Refresh Operation (L-version)
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms
- 1024 Refresh Cycles/128ms (L-version)
- Battery Back Up Operation (L-version)
- 2  $\overline{\text{CAS}}$  byte Control

### Pin Description

| Pin                                | Function               | Pin             | Function          |
|------------------------------------|------------------------|-----------------|-------------------|
| A0-A9                              | Address Inputs         | $\overline{WE}$ | Read/Write Enable |
| A0-A9                              | Refresh Address Inputs | $\overline{OE}$ | Output Enable     |
| I/O0-I/O15                         | Data-In/Out            | V <sub>CC</sub> | Power (+3.3V)     |
| $\overline{RAS}$                   | Row Address Strobe     | V <sub>SS</sub> | Ground            |
| $\overline{UCAS}, \overline{LCAS}$ | Column Address Strobe  | NC              | No Connection     |

### Ordering Information

| Type No.                             | Access Time  | Package                                   |
|--------------------------------------|--------------|-------------------------------------------|
| GM71V18163AJ-7<br>GM71V18163AJ-8     | 70ns<br>80ns | 400 Mil<br>42 Pin<br>Plastic SOJ          |
| GM71V18163AT-7<br>GM71V18163AT-8     | 70ns<br>80ns | 400 Mil<br>44 (50) Pin<br>Plastic TSOP II |
| GM71VS18163ALJ-7<br>GM71VS18163ALJ-8 | 70ns<br>80ns | 400 Mil<br>42 Pin<br>Plastic SOJ          |
| GM71VS18163ALT-7<br>GM71VS18163ALT-8 | 70ns<br>80ns | 400 Mil<br>44 (50) Pin<br>Plastic TSOP II |

### Absolute Maximum Ratings\*

| Symbol               | Parameter                                              | Rating                                      | Unit |
|----------------------|--------------------------------------------------------|---------------------------------------------|------|
| T <sub>A</sub>       | Ambient Temperature under Bias                         | 0 ~ 70                                      | °C   |
| T <sub>STG</sub>     | Storage Temperature (Plastic)                          | -55 ~ 125                                   | °C   |
| V <sub>IN/VOUT</sub> | Voltage on any Pin Relative to V <sub>SS</sub>         | -0.5 ~ V <sub>CC</sub> +0.5<br>(≤4.6V(max)) | V    |
| V <sub>CC</sub>      | Voltage on V <sub>CC</sub> Relative to V <sub>SS</sub> | -0.5 ~ +4.6                                 | V    |
| I <sub>OUT</sub>     | Short Circuit Output Current                           | 50                                          | mA   |
| P <sub>D</sub>       | Power Dissipation                                      | 1.0                                         | W    |

\*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**Recommended DC Operating Conditions ( $T_A = 0 \sim 70^\circ\text{C}$ )**

| Symbol   | Parameter          | Min  | Typ | Max            | Unit |
|----------|--------------------|------|-----|----------------|------|
| $V_{CC}$ | Supply Voltage     | 3.0  | 3.3 | 3.6            | V    |
| $V_{IH}$ | Input High Voltage | 2.0  | -   | $V_{CC} + 0.3$ | V    |
| $V_{IL}$ | Input Low Voltage  | -0.3 | -   | 0.8            | V    |

\*Note: All voltage referred to  $V_{SS}$ .

The supply voltage with all  $V_{CC}$  pins must be on the same level. The supply voltage with all  $V_{SS}$  pins must be on the same level.

**Truth Table**

| $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | Output    | Operation                    |                                         | Notes |
|------------------|-------------------|-------------------|-----------------|-----------------|-----------|------------------------------|-----------------------------------------|-------|
| H                | D                 | D                 | D               | D               | Open      | Standby                      |                                         | 1,3   |
| L                | L                 | H                 | H               | L               | Valid     | Lower byte                   | Read cycle                              | 1,3   |
| L                | H                 | L                 | H               | L               | Valid     | Upper byte                   |                                         |       |
| L                | L                 | L                 | H               | L               | Valid     | Word                         |                                         |       |
| L                | L                 | H                 | L               | D               | Open      | Lower byte                   | Early write cycle                       | 1,2,3 |
| L                | H                 | L                 | L               | D               | Open      | Upper byte                   |                                         |       |
| L                | L                 | L                 | L               | D               | Open      | Word                         |                                         |       |
| L                | L                 | H                 | L               | H               | Undefined | Lower byte                   | Delayed Write cycle                     | 1,2,3 |
| L                | H                 | L                 | L               | H               | Undefined | Upper byte                   |                                         |       |
| L                | L                 | L                 | L               | H               | Undefined | Word                         |                                         |       |
| L                | L                 | H                 | H to L          | L to H          | Valid     | Lower byte                   | Read-modify-write cycle                 | 1,3   |
| L                | H                 | L                 | H to L          | L to H          | Valid     | Upper byte                   |                                         |       |
| L                | L                 | L                 | H to L          | L to H          | Valid     | Word                         |                                         |       |
| H to L           | H                 | L                 | D               | D               | Open      | Word                         | CBR Refresh or Self Refresh (L-version) | 1,3   |
| H to L           | L                 | H                 | D               | D               | Open      | Word                         |                                         |       |
| H to L           | L                 | L                 | D               | D               | Open      | Word                         |                                         |       |
| L                | H                 | H                 | D               | D               | Open      | Word                         | $\overline{RAS}$ -only Refresh cycle    | 1,3   |
| L                | L                 | L                 | H               | H               | Open      | Read cycle (Output disabled) |                                         | 1,3   |

\*Note : 1. H : High(inactive), L : Low(active), D : H or L

2.  $t_{wCS} \geq 0\text{ns}$  : Early write cycle,  $t_{wCS} \leq 0\text{ns}$  : Delayed write cycle

3. Mode is determined by the OR function of the  $\overline{UCAS}$  and  $\overline{LCAS}$ . ( Mode is set by the earliest of  $\overline{UCAS}$  and  $\overline{LCAS}$  active edge and reset by the latest of  $\overline{UCAS}$  and  $\overline{LCAS}$  inactive edge.)

However write OPERATION and output High-Z control are done independently by each  $\overline{UCAS}$ ,  $\overline{LCAS}$ . ex) if  $\overline{RAS}$ =H to L,  $\overline{LCAS}$ =L,  $\overline{UCAS}$ =H, then  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle is selected.

**DC Electrical Characteristics** ( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 0 \sim 70^\circ C$ )

| Symbol    | Parameter                                                                                                                                                       | Min   | Max      | Unit    | Note       |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|----------|---------|------------|
| $V_{OH}$  | Output Level<br>Output "H" Level Voltage ( $I_{OUT} = -2mA$ )                                                                                                   | 2.4   | $V_{CC}$ | V       |            |
| $V_{OL}$  | Output Level<br>Output "L" Level Voltage ( $I_{OUT} = 2mA$ )                                                                                                    | 0     | 0.4      | V       |            |
| $I_{CC1}$ | Operating Current<br>Average Power Supply Operating Current<br>( $\overline{RAS}$ , $\overline{UCAS}$ or $\overline{LCAS}$ Cycling: $t_{RC} = t_{RC\ min}$ )    | 70 ns | -        | 150     | mA<br>1, 2 |
|           |                                                                                                                                                                 | 80 ns | -        | 130     |            |
| $I_{CC2}$ | Standby Current (TTL)<br>Power Supply Standby Current<br>( $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS} = V_{IH}$ , $D_{OUT} = High-Z$ )             | -     | 2        | mA      |            |
| $I_{CC3}$ | $\overline{RAS}$ Only Refresh Current<br>Average Power Supply Current<br>$\overline{RAS}$ Only Refresh Mode<br>( $t_{RC} = t_{RC\ min}$ )                       | 70 ns | -        | 150     | mA<br>2    |
|           |                                                                                                                                                                 | 80 ns | -        | 130     |            |
| $I_{CC4}$ | Extended Data Out Mode Current<br>Average Power Supply Current<br>EDO Mode<br>( $t_{RDC} = t_{RDC\ min}$ )                                                      | 70 ns | -        | 165     | mA<br>1, 3 |
|           |                                                                                                                                                                 | 80 ns | -        | 150     |            |
| $I_{CC5}$ | Standby Current (CMOS)<br>Power Supply Standby Current<br>( $\overline{RAS}$ , $\overline{UCAS}$ or $\overline{LCAS} \geq V_{CC} - 0.2V$ , $D_{OUT} = High-Z$ ) | -     | 1        | mA      | 4          |
|           |                                                                                                                                                                 | -     | 150      | $\mu A$ |            |
| $I_{CC6}$ | $\overline{CAS}$ -before- $\overline{RAS}$ Refresh Current<br>( $t_{RC} = t_{RC\ min}$ )                                                                        | 70 ns | -        | 150     | mA         |
|           |                                                                                                                                                                 | 80 ns | -        | 130     |            |
| $I_{CC7}$ | Battery Back Up Operating Current<br>(Standby with CBR Refresh)<br>( $t_{RC} = 125\ \mu s$ , $t_{RAS} \leq 0.3\ \mu s$ , $D_{OUT} = High-Z$ )                   | -     | 400      | $\mu A$ | 4, 5       |
| $I_{CC8}$ | Standby Current $\overline{RAS} = V_{IH}$<br>$\overline{UCAS}$ , $\overline{LCAS} = V_{IL}$<br>$D_{OUT} = Enable$                                               | -     | 5        | mA      | 1          |
| $I_{CC9}$ | Self-Refresh Mode Current<br>( $\overline{RAS}$ , $\overline{UCAS}$ or $\overline{LCAS} \leq 0.2V$ , $D_{OUT} = High-Z$ )                                       | -     | 250      | $\mu A$ | 5          |
| $I_{IL}$  | Input Leakage Current<br>Any Input ( $0V \leq V_{IN} \leq 4.6V$ )                                                                                               | -10   | 10       | $\mu A$ |            |
| $I_{OL}$  | Output Leakage Current<br>( $D_{OUT}$ is Disabled, $0V \leq V_{OUT} \leq 4.6V$ )                                                                                | -10   | 10       | $\mu A$ |            |

Note: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC(max)}$  is specified at the output open condition.

2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{LCAS}$  and  $\overline{UCAS} = V_{IH}$ .

4.  $V_{IH} \geq V_{CC} - 0.2V$ ,  $0V \leq V_{IL} \leq 0.2V$ .

5. L-version.

**Capacitance** ( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 25^\circ C$ )

| Symbol    | Parameter                        | Min | Max | Unit | Note |
|-----------|----------------------------------|-----|-----|------|------|
| $C_{I1}$  | Input Capacitance (Address)      | -   | 5   | pF   | 1    |
| $C_{I2}$  | Input Capacitance (Clocks)       | -   | 7   | pF   | 1    |
| $C_{I/O}$ | Output Capacitance (Data-In/Out) | -   | 7   | pF   | 1, 2 |

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. LCAS and UCAS =  $V_{IH}$  to disable Dour.

**AC Characteristics** ( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 0 \sim 70^\circ C$ , Notes 1, 2, 19)

**Test Conditions**

Input rise and fall times : 2 ns

Input levels :  $V_{IL} = 0V$ ,  $V_{IH} = 3V$

Input timing reference levels : 0.8V, 2.0V

Output timing reference levels : 0.8V, 2.0V

Output load : 1TTL gate +  $C_L$  (100 pF)

(Including scope and jig)

**Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)**

| Symbol    | Parameter                                           | GM71V(S)18163<br>A/AL-7 |        | GM71V(S)18163<br>A/AL-8 |        | Unit | Note |
|-----------|-----------------------------------------------------|-------------------------|--------|-------------------------|--------|------|------|
|           |                                                     | Min                     | Max    | Min                     | Max    |      |      |
| $t_{RC}$  | Random Read or Write Cycle Time                     | 124                     | -      | 144                     | -      | ns   |      |
| $t_{RP}$  | $\overline{RAS}$ Precharge Time                     | 50                      | -      | 60                      | -      | ns   |      |
| $t_{CP}$  | $\overline{CAS}$ Precharge Time                     | 13                      | -      | 15                      | -      | ns   |      |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width                        | 70                      | 10,000 | 80                      | 10,000 | ns   |      |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width                        | 13                      | 10,000 | 15                      | 10,000 | ns   |      |
| $t_{ASR}$ | Row Address Set up Time                             | 0                       | -      | 0                       | -      | ns   |      |
| $t_{RAH}$ | Row Address Hold Time                               | 10                      | -      | 10                      | -      | ns   |      |
| $t_{ASC}$ | Column Address Set-up Time                          | 0                       | -      | 0                       | -      | ns   | 21   |
| $t_{CAH}$ | Column Address Hold Time                            | 13                      | -      | 15                      | -      | ns   | 21   |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time     | 20                      | 52     | 20                      | 60     | ns   | 3    |
| $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time       | 15                      | 35     | 15                      | 40     | ns   | 4    |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time                          | 18                      | -      | 20                      | -      | ns   |      |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time                          | 58                      | -      | 68                      | -      | ns   | 23   |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5                       | -      | 5                       | -      | ns   | 22   |
| $t_{ODD}$ | $\overline{OE}$ to $D_{IN}$ Delay Time              | 18                      | -      | 20                      | -      | ns   | 5    |
| $t_{DZO}$ | $\overline{OE}$ Delay Time from $D_{IN}$            | 0                       | -      | 0                       | -      | ns   | 6    |
| $t_{DZC}$ | $\overline{CAS}$ Delay Time from $D_{IN}$           | 0                       | -      | 0                       | -      | ns   | 6    |
| $t_T$     | Transition Time (Rise and Fall)                     | 2                       | 50     | 2                       | 50     | ns   | 7    |
| $t_{REF}$ | Refresh Period                                      | -                       | 16     | -                       | 16     | ms   |      |
|           | Refresh Period (L-version)                          | -                       | 128    | -                       | 128    | ms   |      |

## Read Cycle

| Symbol            | Parameter                                              | GM71V(S)18163<br>A/AL-7 |     | GM71V(S)18163<br>A/AL-8 |     | Unit | Note    |
|-------------------|--------------------------------------------------------|-------------------------|-----|-------------------------|-----|------|---------|
|                   |                                                        | Min                     | Max | Min                     | Max |      |         |
| t <sub>RAC</sub>  | Access Time from $\overline{\text{RAS}}$               | -                       | 70  | -                       | 80  | ns   | 8,9     |
| t <sub>CAC</sub>  | Access Time from $\overline{\text{CAS}}$               | -                       | 18  | -                       | 20  | ns   | 9,10,17 |
| t <sub>AA</sub>   | Access Time from Address                               | -                       | 35  | -                       | 40  | ns   | 9,11,17 |
| t <sub>OAC</sub>  | Access Time from $\overline{\text{OE}}$                | -                       | 18  | -                       | 20  | ns   | 9       |
| t <sub>RCS</sub>  | Read Command Setup Time                                | 0                       | -   | 0                       | -   | ns   | 21      |
| t <sub>RCH</sub>  | Read Command Hold Time to $\overline{\text{CAS}}$      | 0                       | -   | 0                       | -   | ns   | 12,22   |
| t <sub>RCHR</sub> | Read Command Hold Time from $\overline{\text{RAS}}$    | 70                      | -   | 80                      | -   | ns   |         |
| t <sub>RRH</sub>  | Read Command Hold Time to $\overline{\text{RAS}}$      | 5                       | -   | 5                       | -   | ns   | 12      |
| t <sub>RAL</sub>  | Column Address to $\overline{\text{RAS}}$ Lead Time    | 35                      | -   | 40                      | -   | ns   |         |
| t <sub>CAL</sub>  | Column Address to $\overline{\text{CAS}}$ Lead Time    | 23                      | -   | 28                      | -   | ns   |         |
| t <sub>CLZ</sub>  | $\overline{\text{CAS}}$ to Output in Low-Z             | 0                       | -   | 0                       | -   | ns   |         |
| t <sub>OH</sub>   | Output Data Hold Time                                  | 3                       | -   | 3                       | -   | ns   | 27      |
| t <sub>OH0</sub>  | Output Data Hold Time from $\overline{\text{OE}}$      | 3                       | -   | 3                       | -   | ns   |         |
| t <sub>OFF</sub>  | Output Buffer Turn-off Time                            | -                       | 15  | -                       | 15  | ns   | 13,27   |
| t <sub>OEZ</sub>  | Output Buffer Turn-off Time to $\overline{\text{OE}}$  | -                       | 15  | -                       | 15  | ns   | 13      |
| t <sub>CDD</sub>  | $\overline{\text{CAS}}$ to D <sub>IN</sub> Delay Time  | 18                      | -   | 20                      | -   | ns   | 5       |
| t <sub>OHR</sub>  | Output Data Hold Time from $\overline{\text{RAS}}$     | 3                       | -   | 3                       | -   | ns   | 27      |
| t <sub>OFR</sub>  | Output Buffer Turn-off Time to $\overline{\text{RAS}}$ | -                       | 15  | -                       | 15  | ns   | 27      |
| t <sub>WEZ</sub>  | Output Buffer Turn-off Time to $\overline{\text{WE}}$  | -                       | 15  | -                       | 15  | ns   |         |
| t <sub>WDD</sub>  | $\overline{\text{WE}}$ to D <sub>IN</sub> Delay Time   | 18                      | -   | 20                      | -   | ns   |         |
| t <sub>RDD</sub>  | $\overline{\text{RAS}}$ to D <sub>IN</sub> Delay Time  | 18                      | -   | 20                      | -   | ns   |         |

### Write Cycle

| Symbol           | Parameter                                          | GM71V(S)18163<br>A/AL-7 |     | GM71V(S)18163<br>A/AL-8 |     | Unit | Note  |
|------------------|----------------------------------------------------|-------------------------|-----|-------------------------|-----|------|-------|
|                  |                                                    | Min                     | Max | Min                     | Max |      |       |
| t <sub>WCS</sub> | Write Command Setup Time                           | 0                       | -   | 0                       | -   | ns   | 14,21 |
| t <sub>WCH</sub> | Write Command Hold Time                            | 13                      | -   | 15                      | -   | ns   | 21    |
| t <sub>WP</sub>  | Write Command Pulse Width                          | 10                      | -   | 10                      | -   | ns   |       |
| t <sub>RWL</sub> | Write Command to $\overline{\text{RAS}}$ Lead Time | 13                      | -   | 15                      | -   | ns   |       |
| t <sub>CWL</sub> | Write Command to $\overline{\text{CAS}}$ Lead Time | 13                      | -   | 15                      | -   | ns   | 23    |
| t <sub>DS</sub>  | Data-in Setup Time                                 | 0                       | -   | 0                       | -   | ns   | 15,23 |
| t <sub>DH</sub>  | Data-in Hold Time                                  | 13                      | -   | 15                      | -   | ns   | 15,23 |

### Read-Modify-Write Cycle

| Symbol           | Parameter                                                    | GM71V(S)18163<br>A/AL-7 |     | GM71V(S)18163<br>A/AL-8 |     | Unit | Note |
|------------------|--------------------------------------------------------------|-------------------------|-----|-------------------------|-----|------|------|
|                  |                                                              | Min                     | Max | Min                     | Max |      |      |
| t <sub>RWC</sub> | Read-Modify-Write Cycle Time                                 | 175                     | -   | 199                     | -   | ns   |      |
| t <sub>RWD</sub> | $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time | 92                      | -   | 104                     | -   | ns   | 14   |
| t <sub>CWD</sub> | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time | 40                      | -   | 44                      | -   | ns   | 14   |
| t <sub>AWD</sub> | Column Address to $\overline{\text{WE}}$ Delay Time          | 57                      | -   | 64                      | -   | ns   | 14   |
| t <sub>OEH</sub> | $\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ | 18                      | -   | 20                      | -   | ns   |      |

### Refresh Cycle

| Symbol           | Parameter                                                                                                       | GM71V(S)18163<br>A/AL-7 |     | GM71V(S)18163<br>A/AL-8 |     | Unit | Note |
|------------------|-----------------------------------------------------------------------------------------------------------------|-------------------------|-----|-------------------------|-----|------|------|
|                  |                                                                                                                 | Min                     | Max | Min                     | Max |      |      |
| t <sub>CSR</sub> | $\overline{\text{CAS}}$ Setup Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle) | 5                       | -   | 5                       | -   | ns   | 21   |
| t <sub>CHR</sub> | $\overline{\text{CAS}}$ Hold Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)  | 10                      | -   | 10                      | -   | ns   | 22   |
| t <sub>RPC</sub> | $\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time                                          | 0                       | -   | 0                       | -   | ns   | 21   |

### EDO Mode Cycle

| Symbol            | Parameter                                                                | GM71V(S)18163<br>A/AL-7 |         | GM71V(S)18163<br>A/AL-8 |         | Unit | Note    |
|-------------------|--------------------------------------------------------------------------|-------------------------|---------|-------------------------|---------|------|---------|
|                   |                                                                          | Min                     | Max     | Min                     | Max     |      |         |
| t <sub>HPC</sub>  | EDO Mode Cycle Time                                                      | 30                      | -       | 35                      | -       | ns   | 25      |
| t <sub>RASP</sub> | EDO Mode $\overline{\text{RAS}}$ Pulse Width                             | -                       | 100,000 | -                       | 100,000 | ns   | 16      |
| t <sub>ACP</sub>  | Access Time from $\overline{\text{CAS}}$ Precharge                       | -                       | 40      | -                       | 45      | ns   | 9,17,22 |
| t <sub>RHCP</sub> | $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | 40                      | -       | 45                      | -       | ns   |         |
| t <sub>DOH</sub>  | Output Data Hold Time from $\overline{\text{CAS}}$ Low                   | 5                       | -       | 5                       | -       | ns   | 9       |
| t <sub>COL</sub>  | $\overline{\text{CAS}}$ Hold Time Referred $\overline{\text{OE}}$        | 13                      | -       | 15                      | -       | ns   |         |
| t <sub>COP</sub>  | $\overline{\text{CAS}}$ to $\overline{\text{OE}}$ Setup Time             | 5                       | -       | 5                       | -       | ns   |         |
| t <sub>RCHP</sub> | Read command hold Time from $\overline{\text{CAS}}$ precharge            | 40                      | -       | 45                      | -       | ns   |         |

### EDO Read-Modify-Write Cycle

| Symbol             | Parameter                                                                | GM71V(S)18163<br>A/AL-7 |     | GM71V(S)18163<br>A/AL-8 |     | Unit | Note |
|--------------------|--------------------------------------------------------------------------|-------------------------|-----|-------------------------|-----|------|------|
|                    |                                                                          | Min                     | Max | Min                     | Max |      |      |
| t <sub>HPRWC</sub> | EDO Mode Read-Modify-Write Cycle Time                                    | 90                      | -   | 99                      | -   | ns   |      |
| t <sub>CPW</sub>   | $\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge | 62                      | -   | 69                      | -   | ns   | 14   |

### Self Refresh Mode (L-Version)

| Symbol            | Parameter                                             | GM71VS18163<br>AL-7 |     | GM71VS18163<br>AL-8 |     | Unit | Note |
|-------------------|-------------------------------------------------------|---------------------|-----|---------------------|-----|------|------|
|                   |                                                       | Min                 | Max | Min                 | Max |      |      |
| t <sub>RASS</sub> | $\overline{\text{RAS}}$ Pulse Width (Self-Refresh)    | 100                 | -   | 100                 | -   | us   | 29   |
| t <sub>RPS</sub>  | $\overline{\text{RAS}}$ Precharge Time (Self-Refresh) | 130                 | -   | 150                 | -   | ns   |      |
| t <sub>CHS</sub>  | $\overline{\text{CAS}}$ Hold Time (Self-Refresh)      | -50                 | -   | -50                 | -   | ns   |      |



**Notes :**

1. AC measurements assume  $t_r = 2 \text{ ns}$ .
2. An initial pause of  $200 \mu\text{s}$  is required after power followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh).
3. Operation with the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
4. Operation with the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
5. Either  $t_{\text{ODD}}$  or  $t_{\text{CDD}}$  must be satisfied.
6. Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
7.  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$ .
8. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and 100pF.
10. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ .
11. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ .
12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
13.  $t_{\text{OFF}}(\text{max})$  and  $t_{\text{OEZ}}(\text{max})$  define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , or  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$   $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in delayed write or read-modify-write cycles.
16.  $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in EDO mode cycles.
17. Access time is determined by the longer of  $t_{\text{AA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{ACP}}$ .
18. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device. After  $\overline{\text{RAS}}$  is reset, if  $t_{\text{OEH}} \geq t_{\text{CWL}}$ , the I/O pin will remain open circuit (high impedance); if  $t_{\text{OEH}} \leq t_{\text{CWL}}$ , invalid data will be out at each I/O.
19. When both  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  go low at the same time, all 16-bits data are written into the device.  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  cannot be staggered within the same write/read cycles.
20. All the  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins shall be supplied with the same voltages.
21.  $t_{\text{ASC}}$ ,  $t_{\text{CAH}}$ ,  $t_{\text{RCS}}$ ,  $t_{\text{WCS}}$ ,  $t_{\text{WCH}}$ ,  $t_{\text{CSR}}$  and  $t_{\text{RPC}}$  are determined by the earlier falling edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
22.  $t_{\text{CRP}}$ ,  $t_{\text{CHR}}$ ,  $t_{\text{RCH}}$ ,  $t_{\text{ACP}}$  and  $t_{\text{CPW}}$  are determined by the later rising edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
23.  $t_{\text{CWL}}$ ,  $t_{\text{DH}}$ ,  $t_{\text{DS}}$  and  $t_{\text{CHS}}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
24.  $t_{\text{CP}}$  is determined by the time that both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  are high.

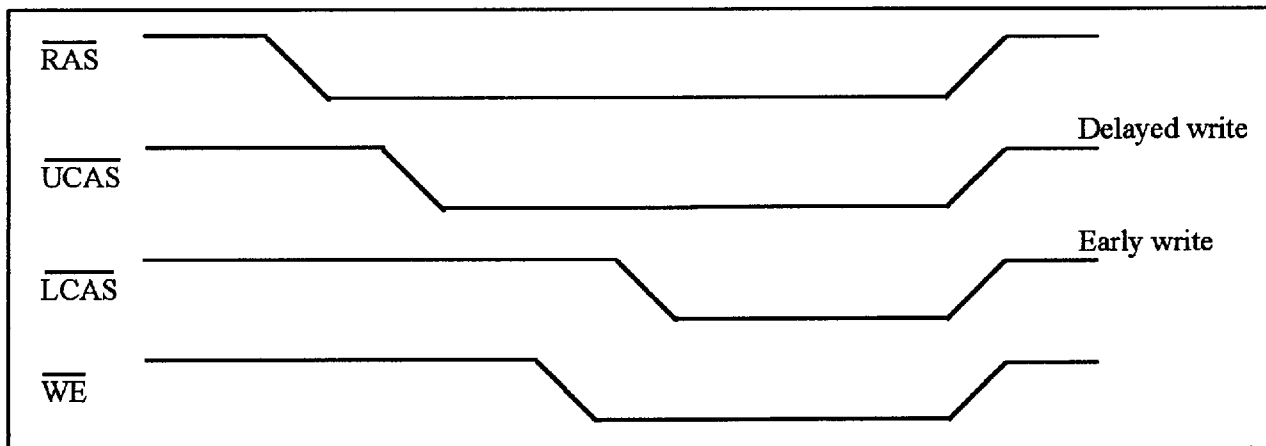


25.  $t_{HPC}(\min)$  can be achieved during a series of EDO page made write cycles or EDO mode write cycles. If both write and read operation are mixed in a EDO mode  $\overline{RAS}$  cycle (EDO mode mix cycle (1),(2)) minimum Value of  $\overline{CAS}$  cycle ( $t_{CAS}+t_{CP}+2t_T$ ) becomes greater than the specified  $t_{HPC}(\min)$  value. The value of  $\overline{CAS}$  cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).
26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH\min}/V_{IL\max}$  level.
27. Data output turns off and becomes high impedance from later rising edge of  $\overline{RAS}$  and  $\overline{CAS}$ . Hold time and turn off time are specified by the timing specification of later rising edge of  $\overline{RAS}$  and  $\overline{CAS}$  between  $t_{OHR}$  and  $t_{OH}$ , and between  $t_{OFF}$  and  $t_{OFF}$ .
28. EDO Hi-Z control by  $\overline{OE}$  or  $\overline{WE}$ .  $\overline{OE}$  rising edge disables data outputs. When  $\overline{OE}$  goes high during  $\overline{CAS}$  high, the data will not come out until next  $\overline{CAS}$  access. When  $\overline{WE}$  goes low during  $\overline{CAS}$  high, the data will not come out until next  $\overline{CAS}$  access.
29. Please do not use  $t_{RASS}$  timing,  $10\mu s \leq t_{RASS} \leq 100\mu s$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} \geq 100\mu s$ , then  $RAS$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .
30.  H or L (H :  $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ , L :  $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$ )

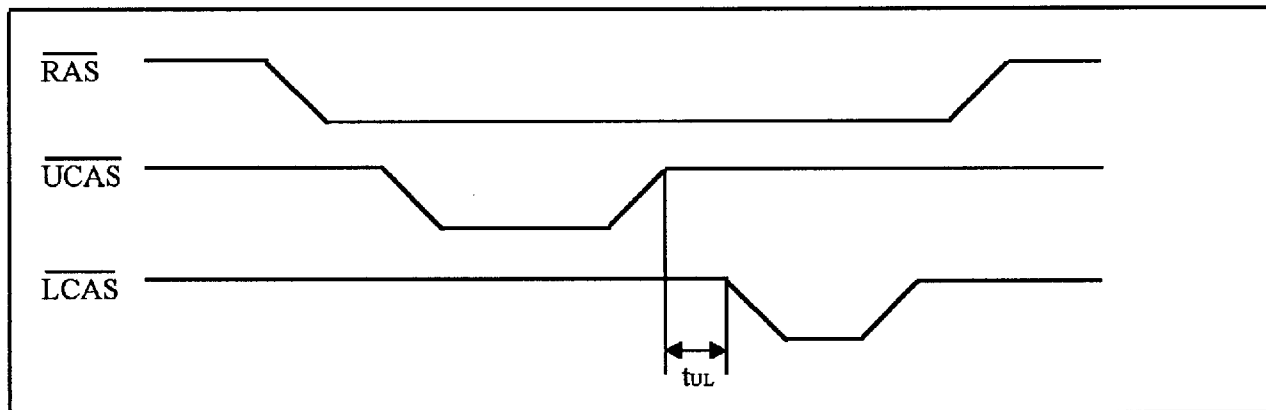
## Notes concerning $\overline{2CAS}$ control

Please do not separate the  $\overline{UCAS}/\overline{LCAS}$  operation timing intentionally. However skew between  $\overline{UCAS}/\overline{LCAS}$  are allowed under the following conditions.

- (1) Each of the  $\overline{UCAS}/\overline{LCAS}$  should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.

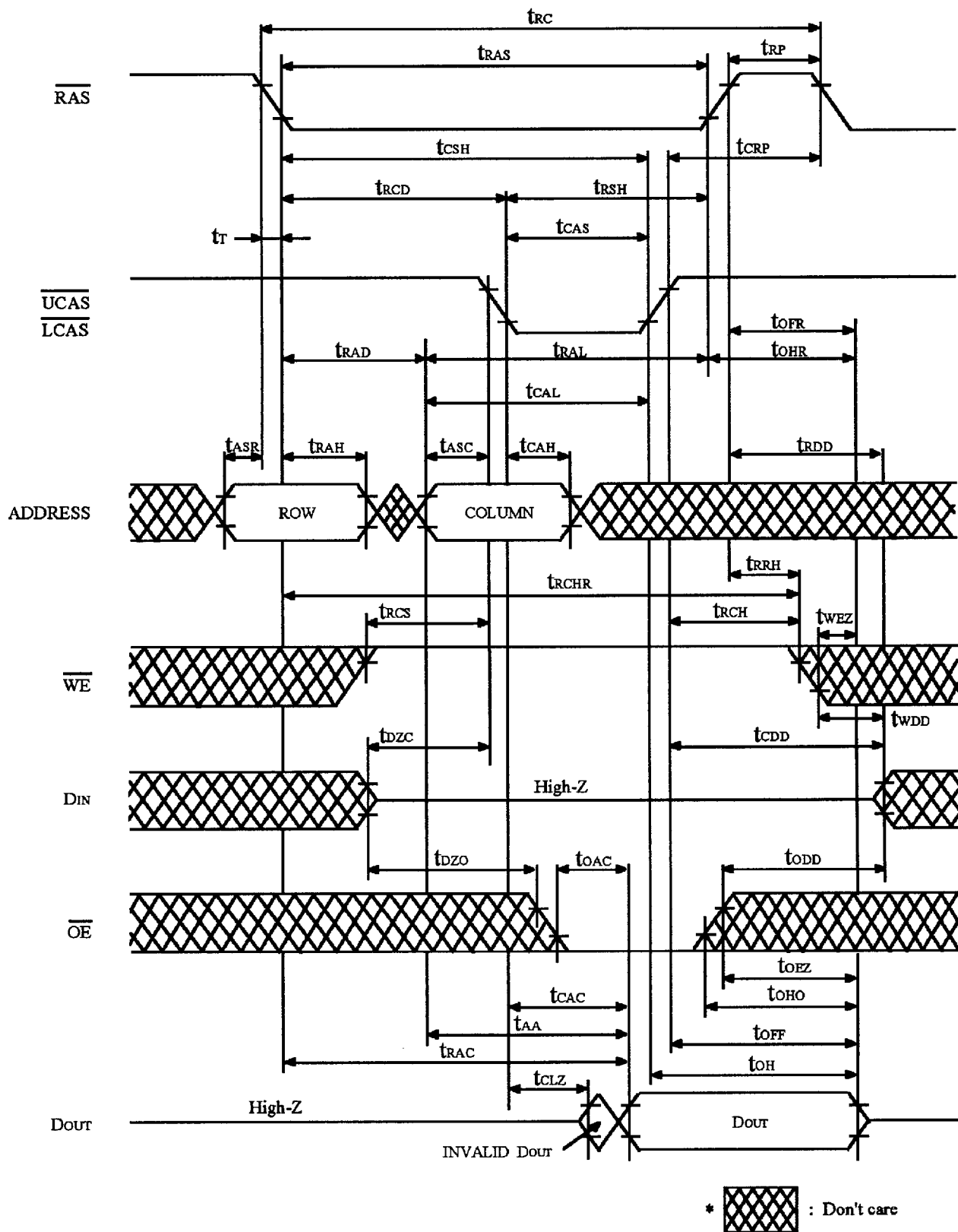


- (3) Closely separated upper/lower byte control is not allowed. However when the condition ( $t_{cp} \leq t_{ul}$ ) is satisfied, EDO page mode can be performed.

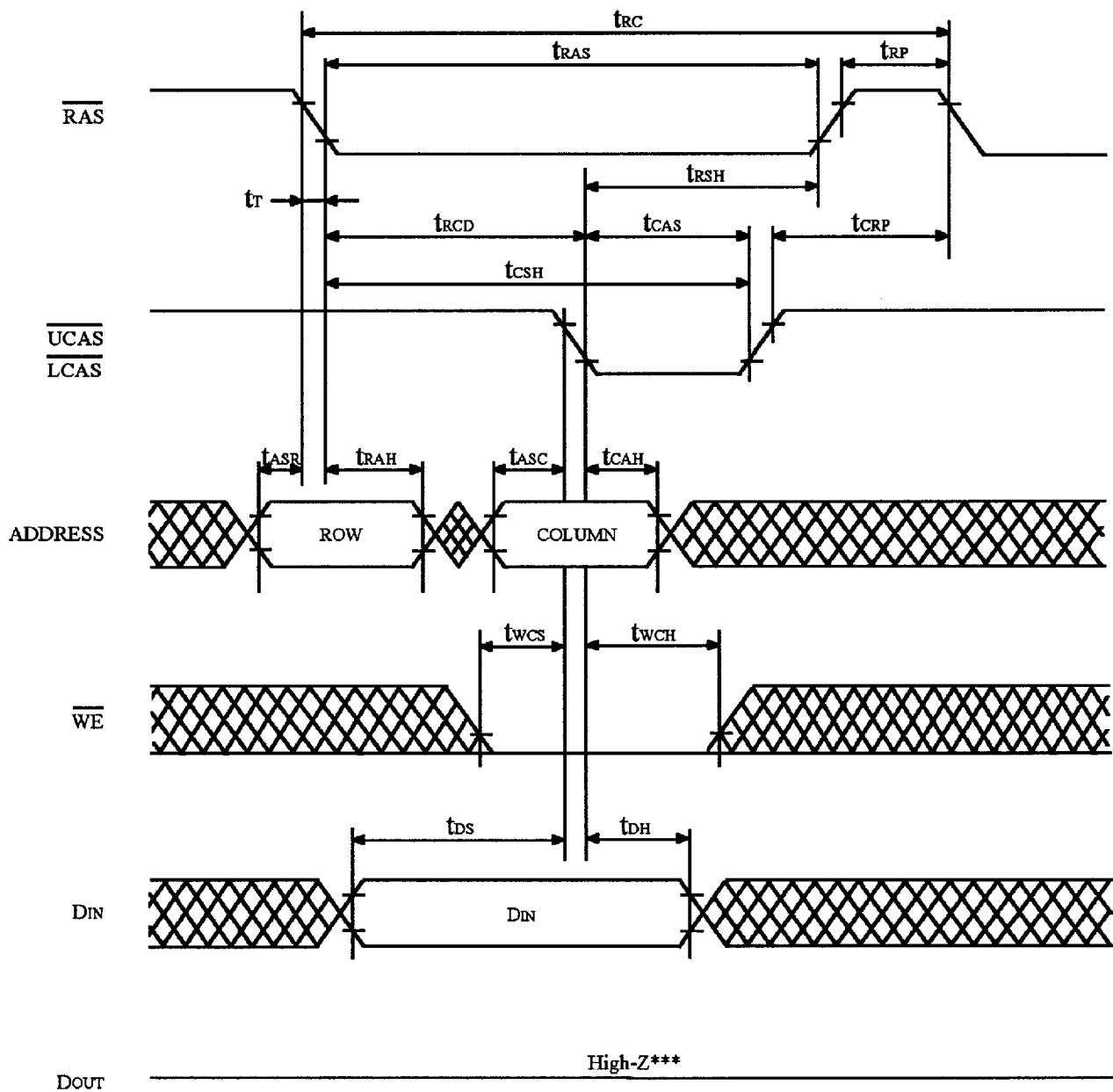


- (4) Byte control operation by remaining  $\overline{LCAS}$  or  $\overline{UCAS}$  high is guaranteed.

## Timing Waveforms<sup>\*30</sup>



### FIGURE 1. READ CYCLE



\*  : Don't care

\*\*  $\overline{OE}$  : Don't care

\*\*\*  $t_{WCS} \geq t_{WCS}(\min)$

FIGURE 2. EARLY WRITE CYCLE

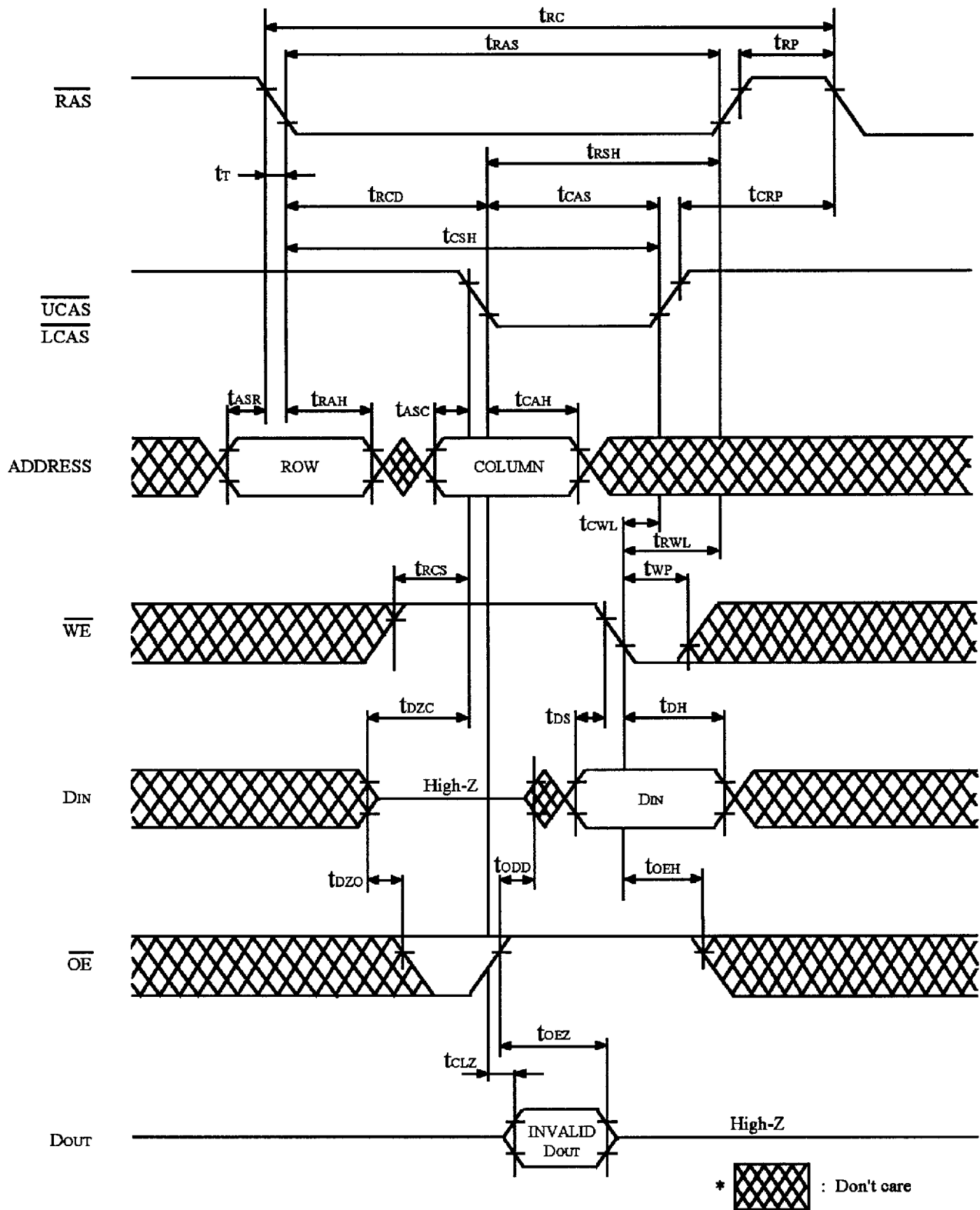


FIGURE 3. DELAYED WRITE CYCLE <sup>\*18</sup>

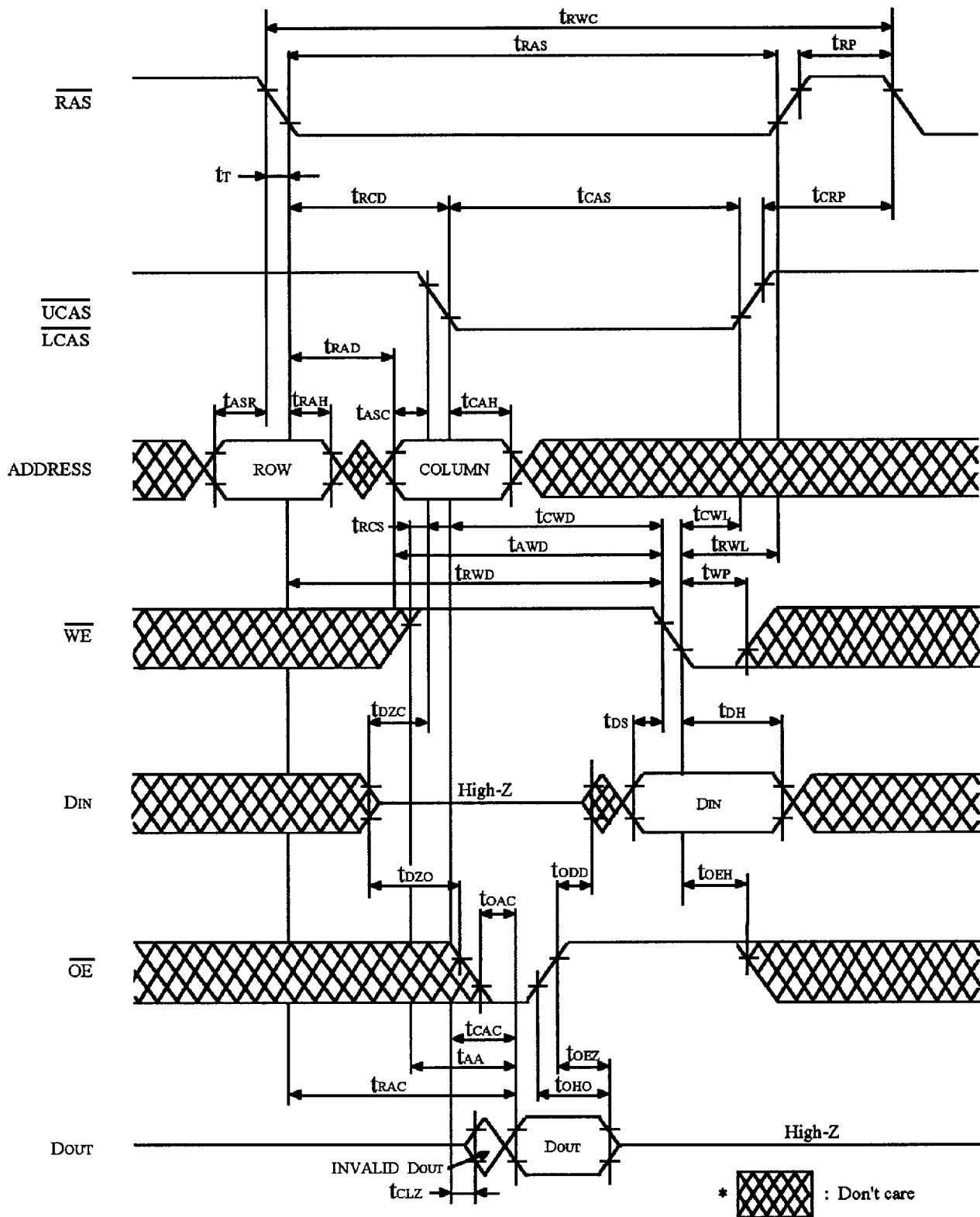
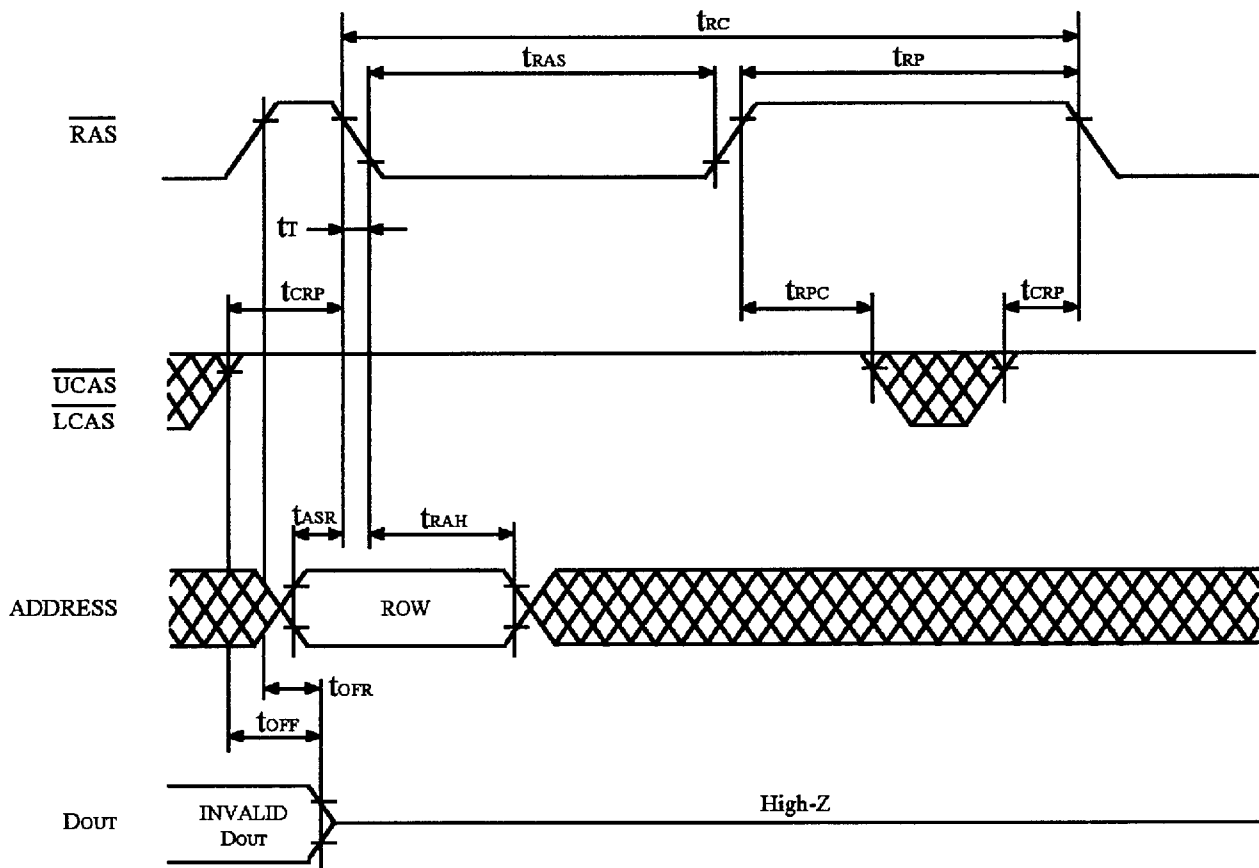


FIGURE 4. READ MODIFY WRITE CYCLE<sup>\*18</sup>



\*  : Don't care

\*\*  $\overline{\text{OE}}$ ,  $\overline{\text{WE}}$  : Don't care

\*\*\* Refresh Address:  
A0-A9 (RA0-RA9)

FIGURE 5.  $\overline{\text{RAS}}$  ONLY REFRESH CYCLE



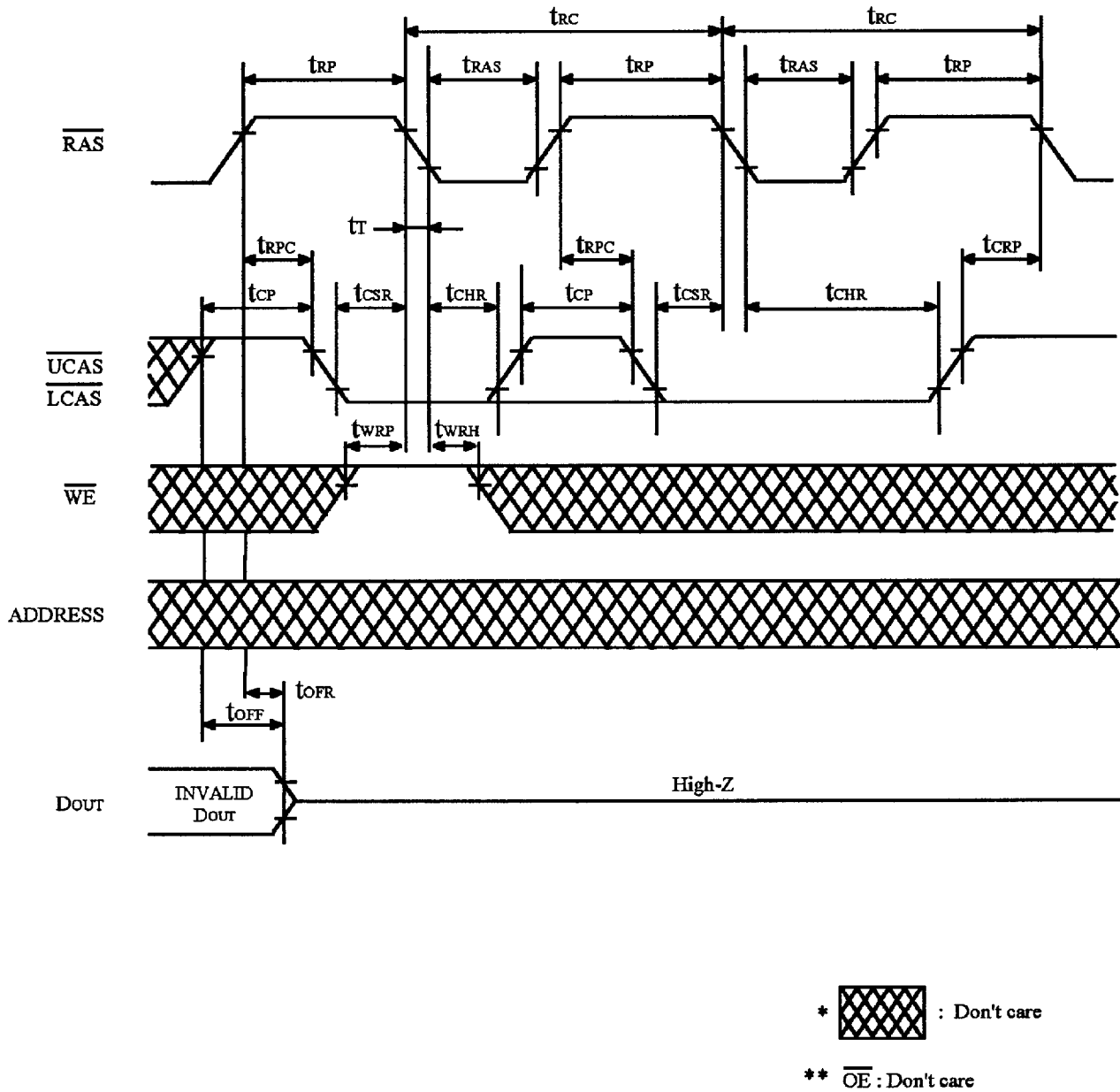


FIGURE 6.  $\overline{CAS}$  BEFORE  $\overline{RAS}$  REFRESH CYCLE

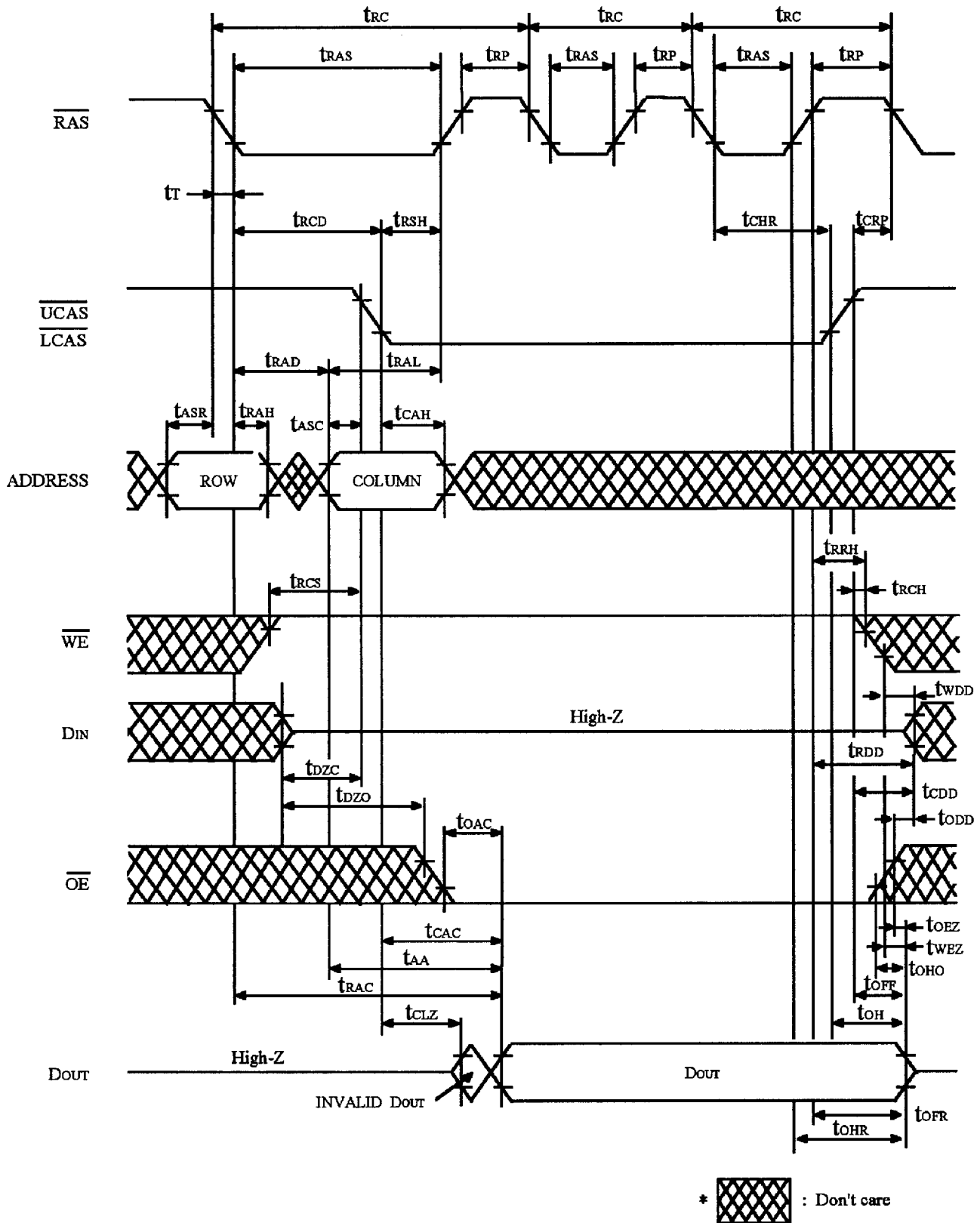


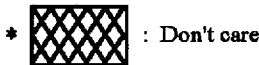
FIGURE 7. HIDDEN REFRESH CYCLE



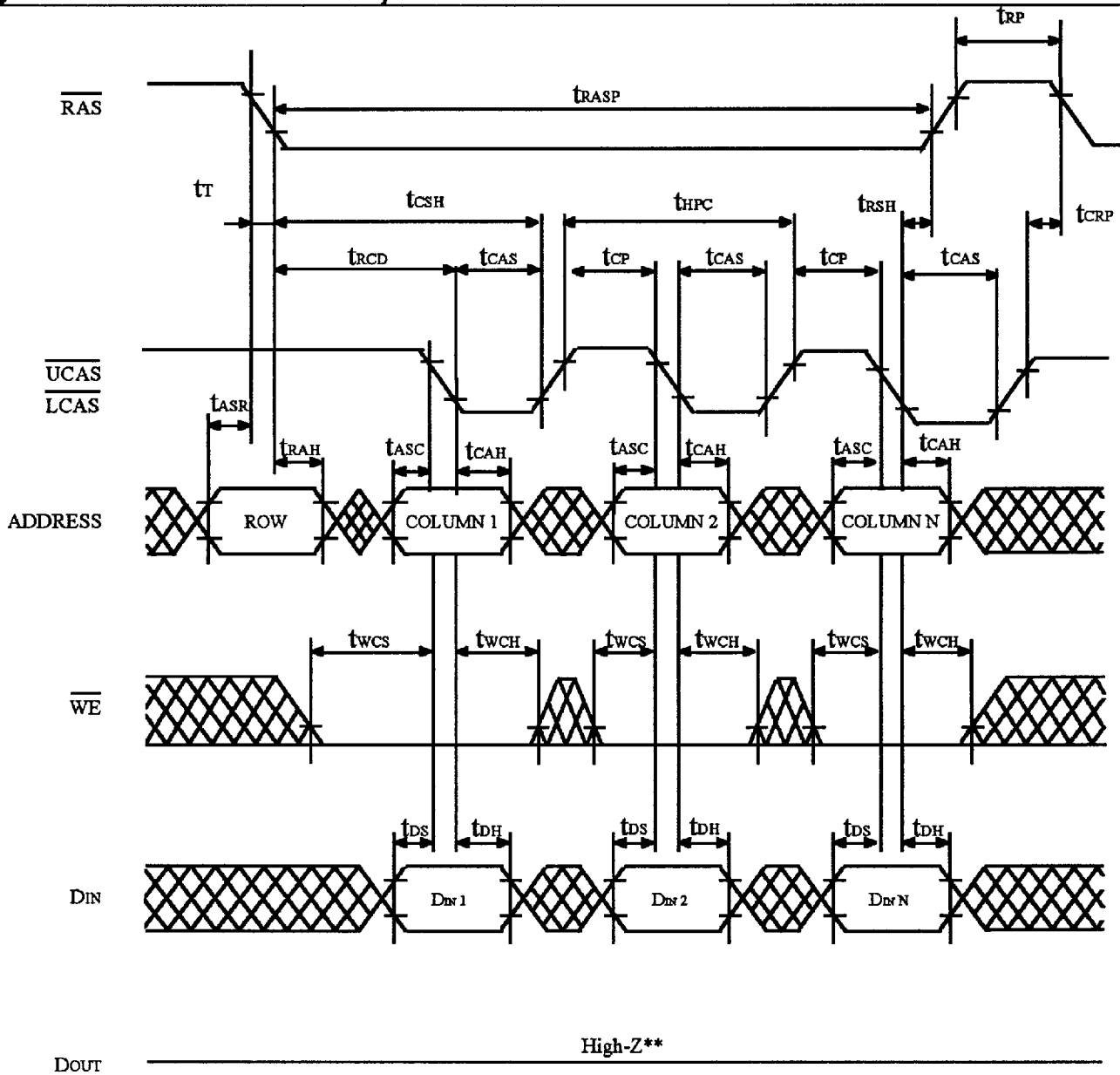
19



**\*28**



**FIGURE 10. EXTENDED DATA OUT MODE READ CYCLE ( $\overline{2C\overline{AS}}$  TYPE)**

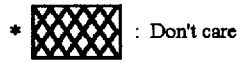


\*  $\overline{\text{OE}}$  : Don't care

\*\*  $t_{\text{wcs}} \geq t_{\text{wcs}}(\text{min})$

\*\*\*  : Don't care

FIGURE 11. EXTENDED DATA OUT MODE EARLY WRITE CYCLE



**\*18**