ADE-XXX-XXX (Z)

HD153061RTF

130-Mbps PRML Data Channel Processor

HITACHI

Under Development
1st. Edition
December 1995

Description

The HD153061RTF is a fully integrated single-chip data channel processor for high performance magnetic disk drives. Functions include automatic gain control (AGC), programmable active filter, A/D converter, FIR transversal filter, Viterbi qualifier, 8/9 ENDEC, data synchronizer, 4-burst servo demodulator, write PLL, and programmable write precompensation. The HD153061RTF is capable of 40 Mbits/s to 130 Mbits/s data rates and supports single zone and Multi Zone Recording(MZR).

The HD153061RTF is fabricated in HITACHI 0.7 µm Hi-BiCMOS process technology which provides high performance with low power consumption. Built-in programmable power management reduces power dissipation to 10 mW when in sleep mode.

Features :

- Sampled data channel with Viterbi qualification.
- 40 to 130 Mbits/s data transfer rate.
- Serial port for register access.
- 5-tap analog FIR transversal filter for adaptive PR4 equalization.
- Data Scrambler and Descrambler function. (0, 4/4) 8/9 code ENDEC
- Programmable 5th order equiripple filter for Data.
- Programmable 3rd order equiripple filter for Servo.
- Programmable write precompensation.
- Power consumption 1.0 W (Typ) at 130 Mbps.
- Power Management system.
  (Servo = 400 mW, Idle = 50 mW, Sleep = 10 mW)
- Selectable 2, 4 or 8-bit parallel NRZ interface.
- Operates from a single 5 V supply.
- Low profile (1.2 mm) package.
- 64 pin TQFP package with copper lead frame.

A/D Converter :

- 5-bit flash A/D converter.
- Integral linearity is guaranteed to ±1.0 LSB.
- Differential linearity is guaranteed to ±1.0 LSB.
- Built-in DC offset adjustment (32 settings).

Encoder/Decoder :

- (0, 4/4) 8/9 Group Code Recording.
- Programmable 2, 4 or 8-bit parallel NRZ interface.
- Encoder bypass function.
- Write data can be selected as differential pseudo-ECL for high speed transfer and minimum timing error.
- On chip programmable write precompensation.
- Data Scrambler/Descrambler reduce fixed pattern effects.

Read Pulse Detector & Servo :

- Built-in AGC amplifier for stable operation to adjust to varying media and head characteristics.
- AGC amplifier gain can be set to zero during write.
- Fast AGC attack can be accomplished by supplying an internal RX signal which is automatically generated on the rising and falling edges of SRV/RD signals.
- AGC input low-Z duration can be controlled by a register.
- 4-burst servo circuit (peak-hold type) with on-chip hold capacitors and buffer amplifiers.
- Servo reference voltage is provided.
- Servo charge speed is programmable.

Write PLL :

- On-chip frequency synthesizer generates write clock.
- Independent M and N divide by registers.
- Unlock detect function.
- VCO center frequency matched to data synchronizer.
- VCO center frequency accuracy is better than ±5%.

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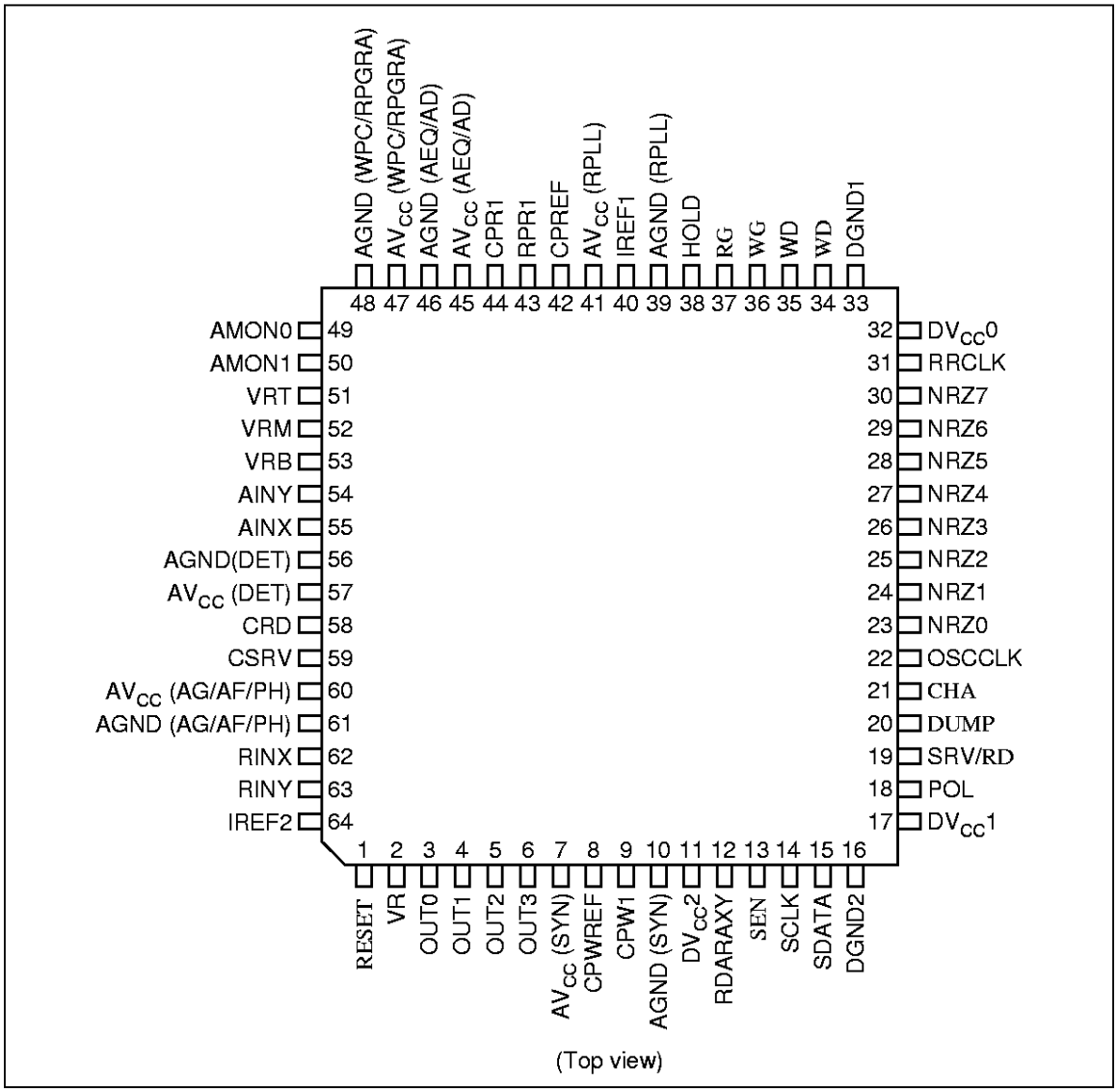
Programmable Active Filter and Transversal Filter :

- 5th order equiripple analog filter with ±10 % asymmetric phase equalization capability for Data mode.
- Cut off frequency is programmable from 9 to 40 MHz for Data and 5 to 16 MHz for Servo mode.
- fc accuracy is guaranteed to ±10 %.
- Group delay variation (0.2 fc to fc) is guaranteed to 3 %.
- 5-tap analog FIR transversal filter for PR4 adaptive equalization.

Data Synchronizer :

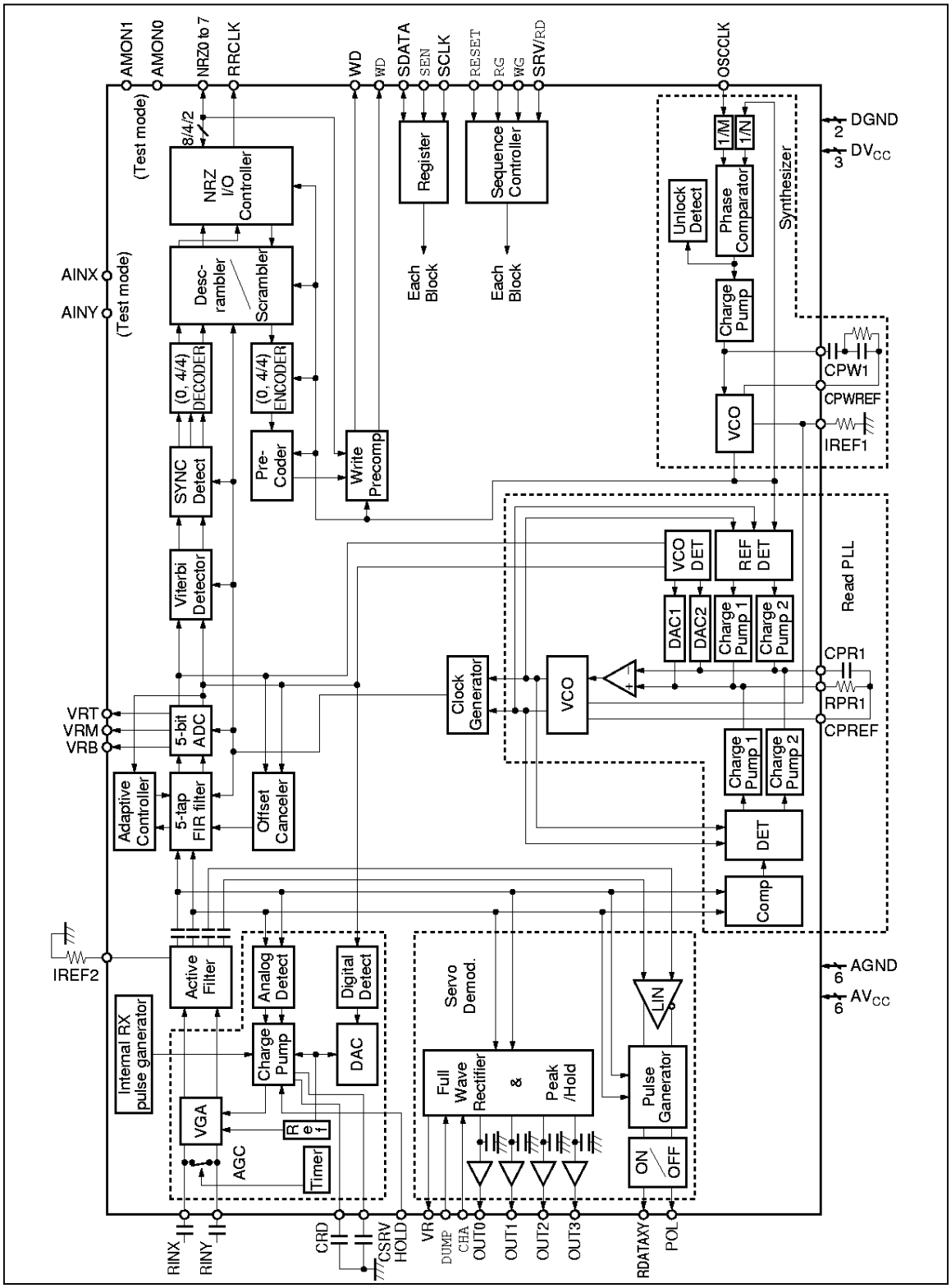
- Programmable VCO center frequency (256 settings).
- Consistant high speed acquisition can be accomplished by switching between normal and high gain modes, and by switching loop filter constants.(typical acquisition time is 15 bytes)
- Dual-mode phase detector compares both phase and frequency to ensure a wide capture range.
- VCO center frequency accuracy is better than ±5 %.

Pin Arrangement



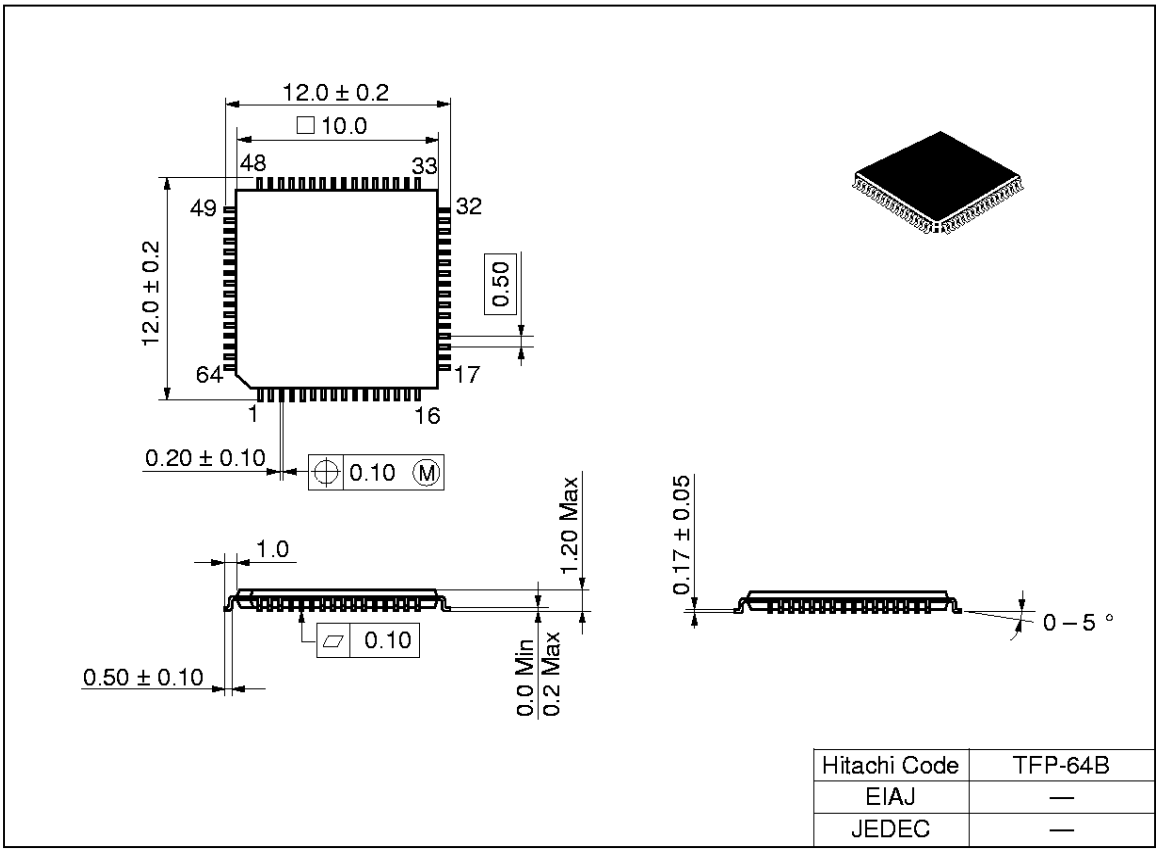
(Top view)

Block Diagram



Package Dimensions

Unit: mm



Hitachi Code	TFP-64B
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JEDEC	—