Sept. 1995
Edition 4.0a

FUJITSU

DATA SHEET

MB501LV/504LV

LOW VOLTAGE/LOW POWER TWO MODULUS PRESCALERS

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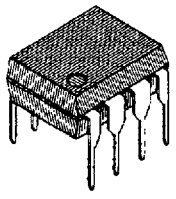
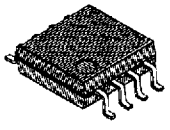
The Fujitsu MB501LV/504LV are low power and low voltage versions of MB501/504, two modulus prescalers used with a frequency synthesizer to make a Phase Locked Loop (PLL). They will divide the input frequency by the modulus of 64/65 or 128/129 for the MB501LV, and 32/33 or 64/65 for the MB504LV. The output level is 1.1V peak to peak on ECL level.

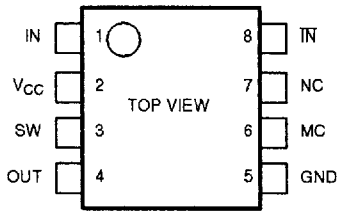
- Wide Low Voltage Operation 3.0V typ., +2.7 to 4.5V
- High Frequency Operation, Low Power Operation (V_{IN} = −12dBm min.)
  1.1 GHz at 36mW typ. (MB501LV)
  520MHz at 18mW typ. (MB504LV)
- Pulse Swallow Function
- Wide Operation Temperature T_A = −40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.1Vp-p typ.
- Built-in a termination resistor
  Stable output amplitude is obtained up to output load capacitance of 8pF.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package



PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01



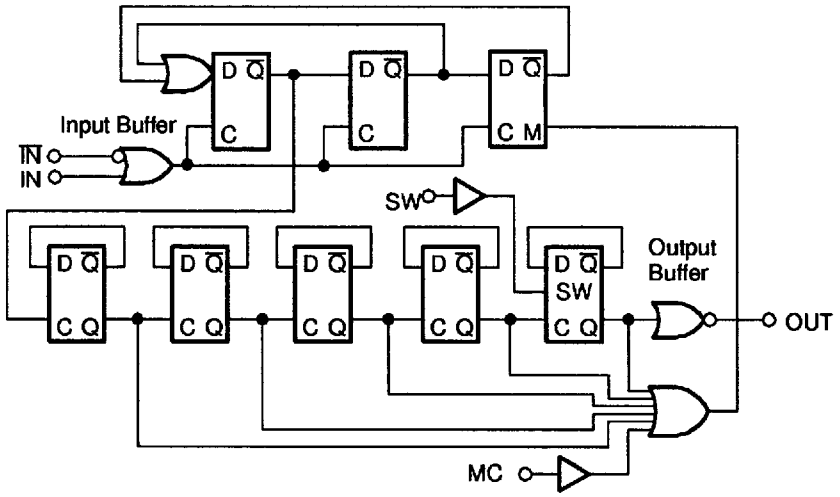
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to + V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	− 55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

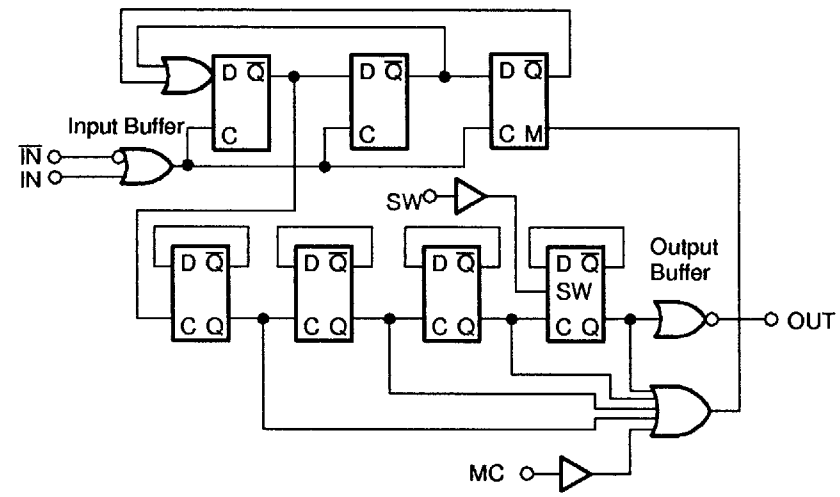
a) MB501LV



SW	MC	Divide Ratio
H	H	1/64
H	L	1/65
L	H	1/128
L	L	1/129

Note: SW: H = V_{CC}, L = OPEN
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{HIM} = {}^1/_2\ V_{CC} + 0.3V$

b) MB504LV



SW	MC	Divide Ratio
H	H	1/32
H	L	1/33
L	H	1/64
L	L	1/65

Note: SW: H = V_{CC}, L = OPEN
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{HIM} = {}^1/_2\ V_{CC} + 0.3V$

Figure 1. Block Diagrams

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	2.7	3.0	4.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			8	pF

ELECTRICAL CHARACTERISTICS

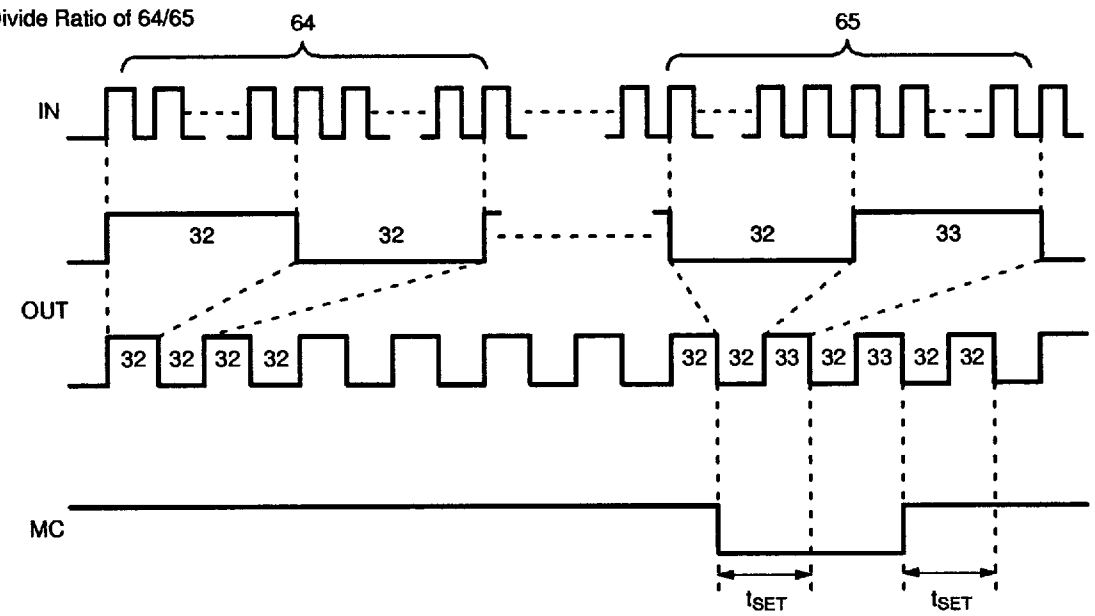
(Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power Supply Current	MB501LV	I_{CC}	V_{CC} = 3.0V		12		mA
	MB504LV				6		mA
Output Amplitude		V_O		0.8	1.1		V_{P-P}
Input Frequency	MB501LV	f_{IN}	With input coupling capacitor 1000pF	10		1100	MHz
	MB504LV			10		520	MHz
Input Signal Amplitude		P_{IN}		-12		5.5	dBm
High Level Input Voltage for MC Input		V_{IHM}	$V_{IHM} = {}^1/_2 V_{CC} + 0.3$	V_{IHM}			V
Low Level Input Voltage for MC Input		V_{ILM}				0.8	V
High Level Input Voltage for SW Input		V_{IHS}*		V_{CC} -0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW Input		V_{ILS}		OPEN			V
High Level Input Current for MC Input		I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input		I_{ILM}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT	MB501LV	t_{SET}			16	26	ns
	MB504LV				18	28	ns

Note: * Design Guarantee

MB501LV TIMING CHART (2 MODULUS)

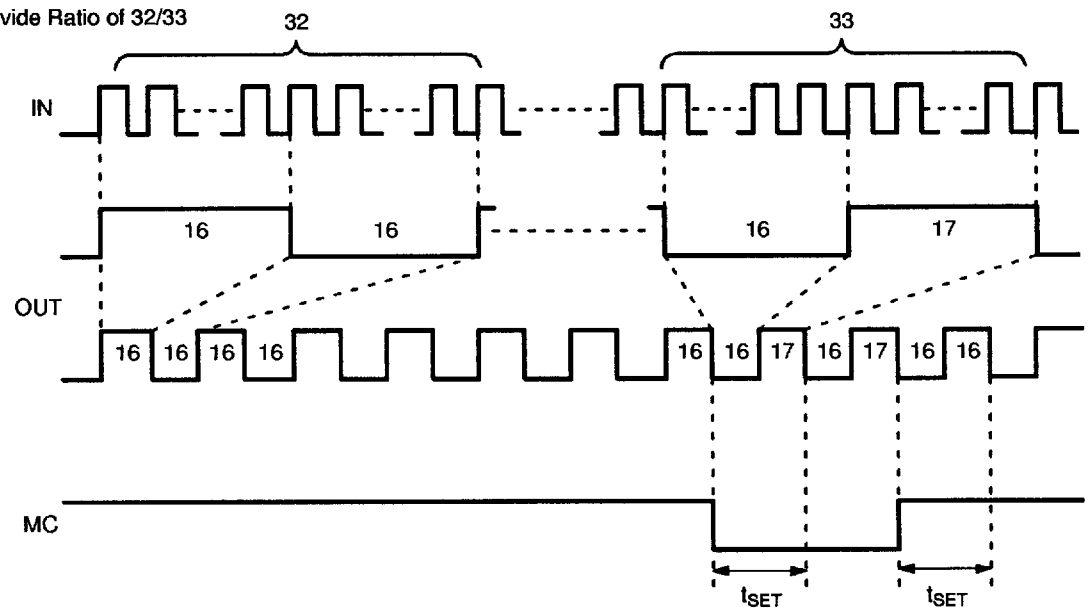
Example: Divide Ratio of 64/65



Notes:
When divide ratio of 65 is selected, positive pulse is added by one to 33.
The typical set up time is 16ns from MC signal input to the timing of change of prescaler divide ratio.

MB504LV TIMING CHART (2 MODULUS)

Example: Divide Ratio of 32/33



Notes:
When divide of 33 is selected, positive pulse is added by one to 17.
The typical set up time is 18ns from MC signal input to the timing of change of prescaler divide ratio.

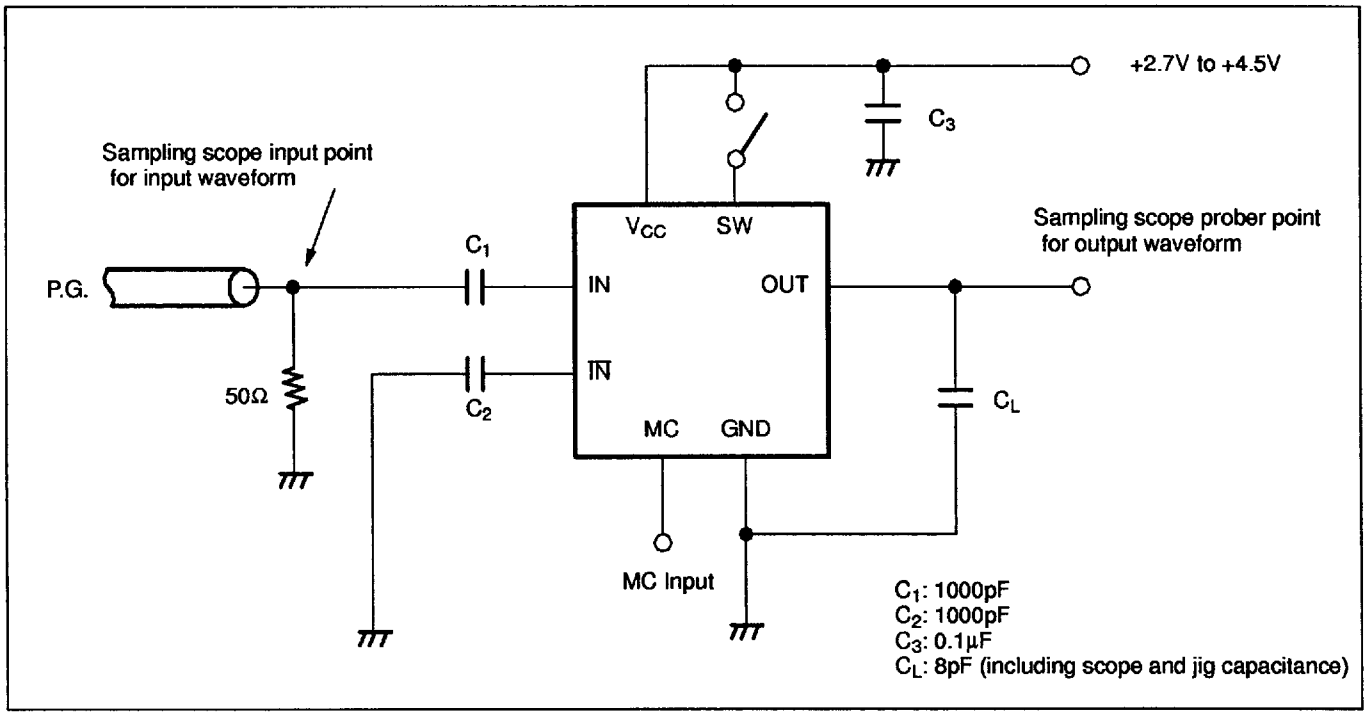


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS CURVES

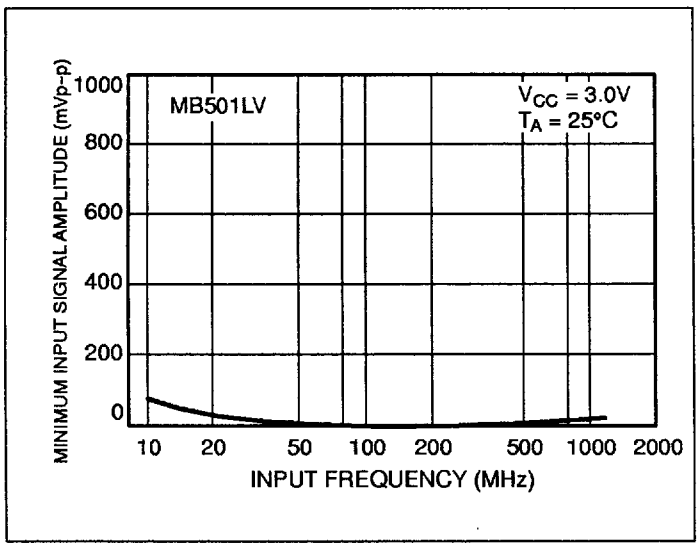


Figure 3. Input Signal Amplitude vs. Input Frequency

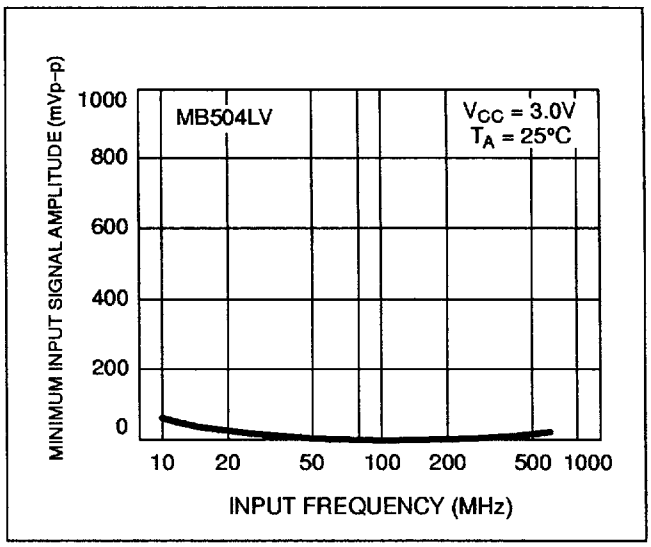


Figure 4. Input Signal Amplitude vs. Input Frequency

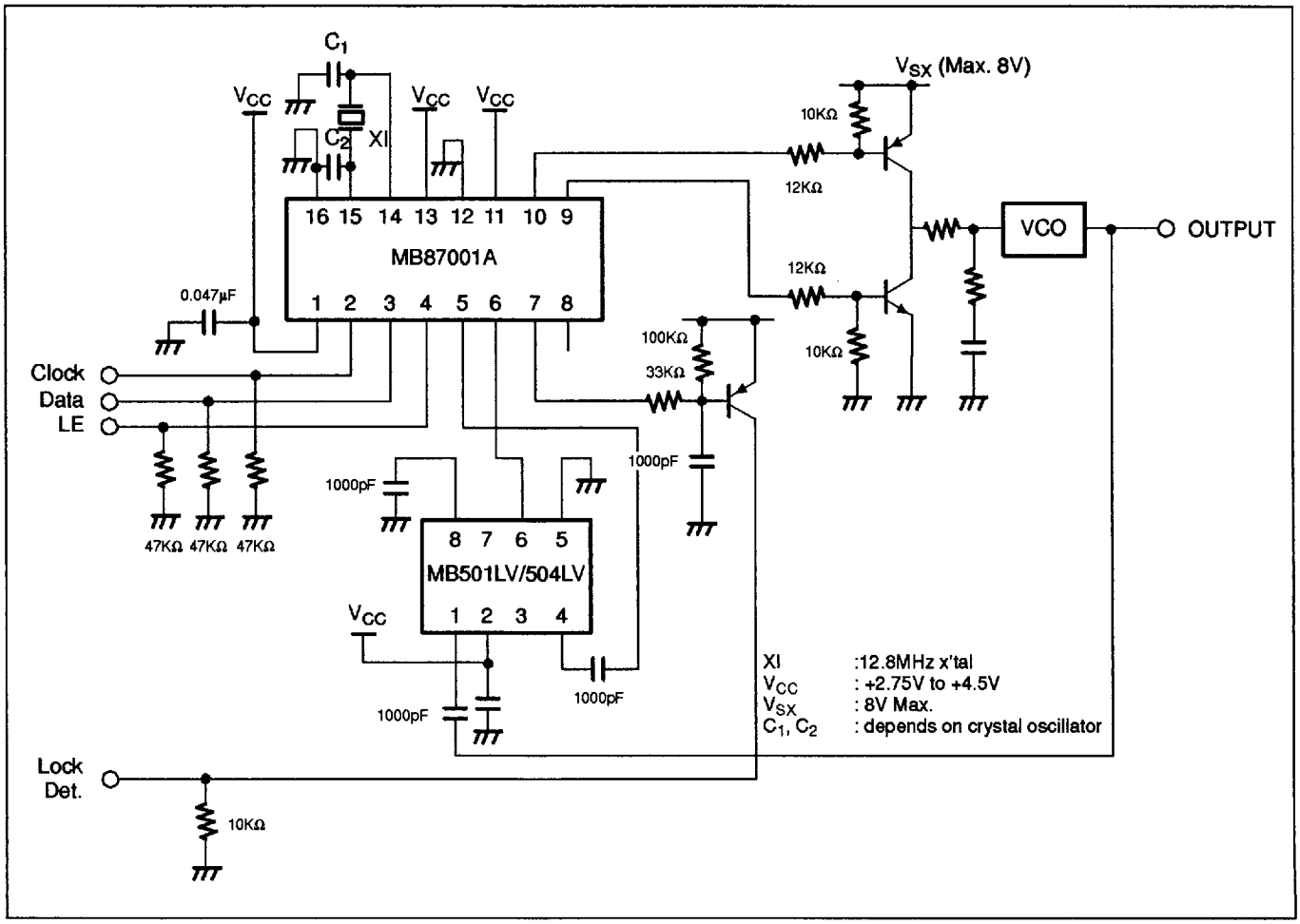
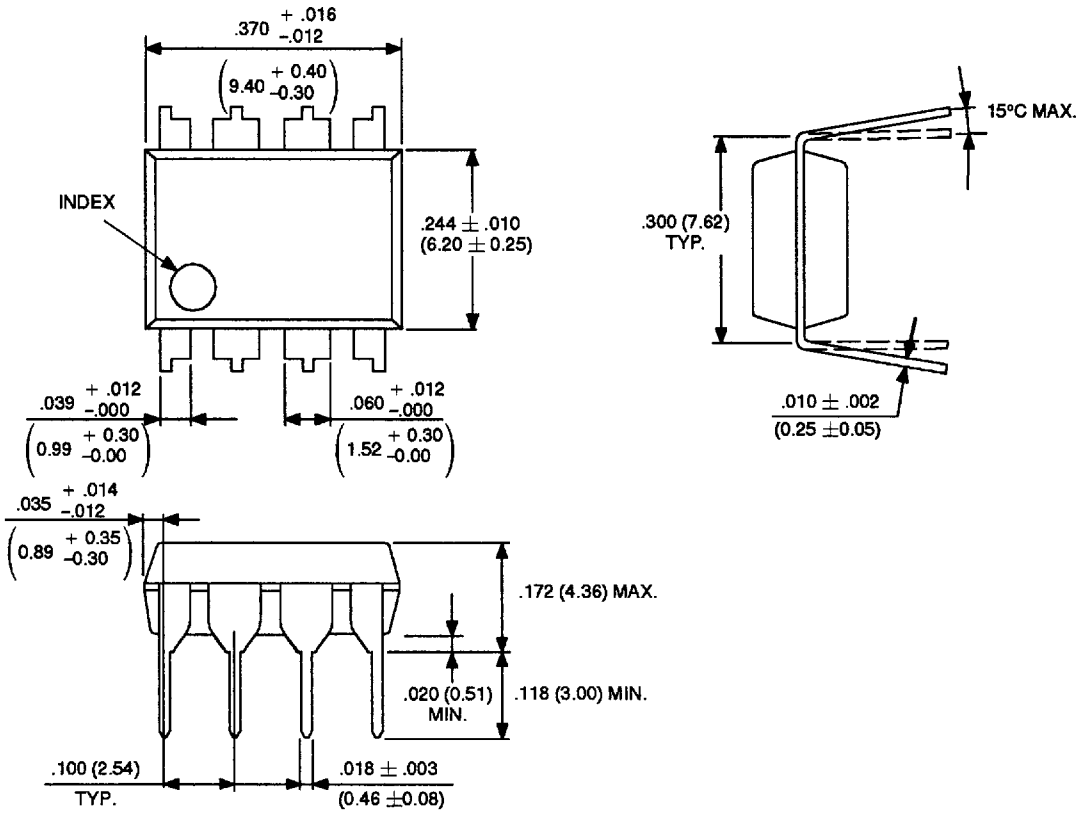


Figure 5. Typical Application Example

PACKAGE DIMENSIONS

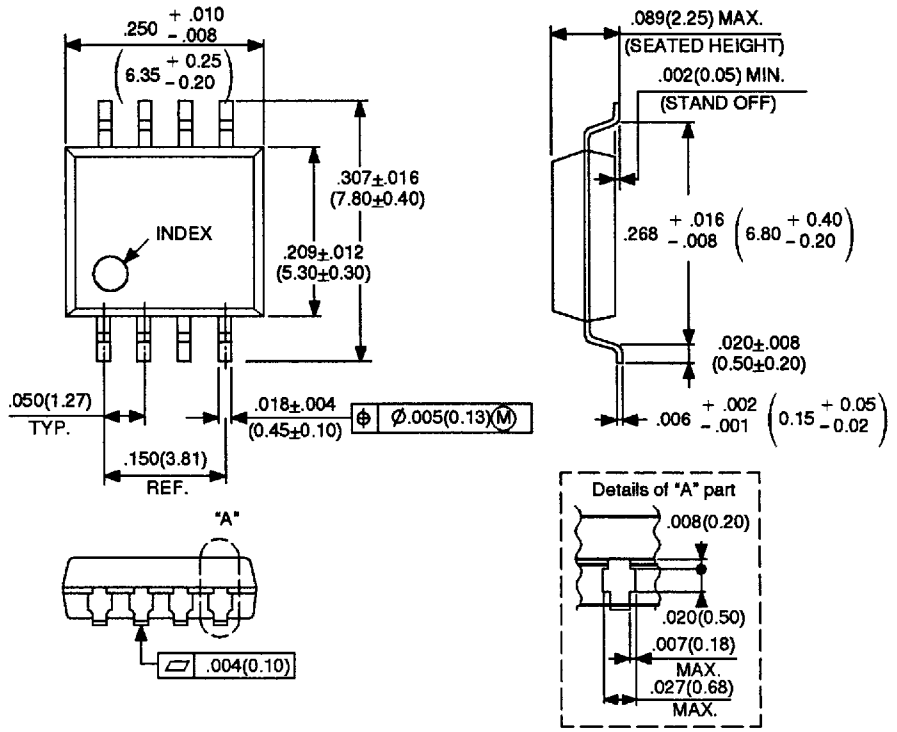
8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters).

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in inches (millimeters).