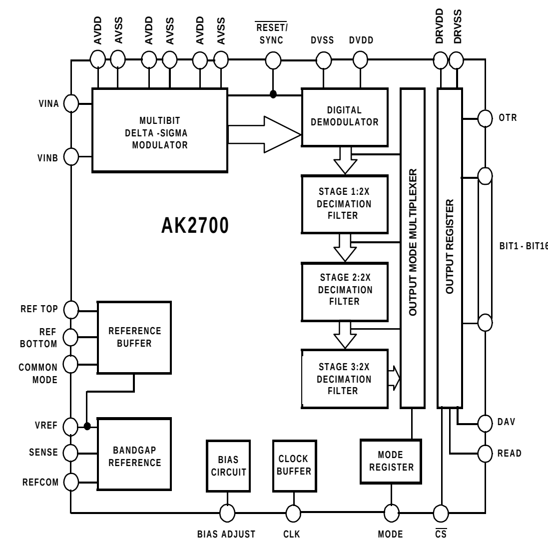
AK2700

High Precision, High Speed ADC:16-Bits, 2.5MSPS

Features

- Monolithic 16-Bit, Oversampled A/D Convertor
- 8 x Oversampling Mode, 20 MHz Clock
- 2.5 MHz output Word Rate
- AC Specifications
  - 1.01 MHz Signal Passband
  - Signal-to-Noise: 90dB
  - Total Harmonic Distortion: -96dB
  - Spurious Free Dynamic range: 100dB
- Digital Filter
  - Stopband Attentuation: 85 dB
  - Passband Ripple: 0.004dB
  - Linear Phase
- Low Power Dissipation: 315 mW
- Power Supply
  - Analog Supply +5 V
  - Digital Supply +3 V/ +5 V
- Twos-Complement Output Data
- 44-Lead LQFP

Block Diagram



Description

The AK2700 is a 16-bit, high speed oversampled analog-to-digital converter (ADC) that offers a high dynamic range over a wideband of 1.01MHz. The AK2700 is manufactured on an advanced submicron analog CMOS process. High dynamic range is achieved with an oversampling of 8x through the use of proprietary multi bit delta sigma techniques.

The AK2700 is a switched-capacitor ADC with a nominal full scale input range of4V. It offers a differential input with 60dB of common-mode rejection. The signal range of each differential input is +/- 1V centered on a 2.5 V common-mode level.

The on-chip decimation filter consists of three half-band FIR filter stages that provide 8x decimation filtering with 85dB of stopband attenuation and 0.004 dB of passband ripple. An integrated digital multiplexer allows users to access data from the 2nd and 3rd stages of the decimation filter.

The on-chip reference and reference buffer amplifier are configured for maximum accuracy and flexibility.

The AK2700 operates on a single +5V analog supply, and +3 V digital supply typically consuming 425 mW of power. For low power applications, the power dissipation can be reduced to 315mW.

The AK2700 is available in a 44-lead LQFP package and is specified to operate in the range of -40 to 85C.

PERFORMANCE SPECIFICATION

DC SPECIFICATION

VA = 5.0V, VD = 3.0V, AGND = DGND = 0V, f_{CLOCK} = 20 MSPS, VCM = 2.5V, Input CML = 2.5V T_{MAX}=85C, T_{MIN}=-40C
Rbias = 3.9k ohms

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Resolution		16			Bits
Input Referred Noise (Typical)					
2.5 V Reference			0.69		LSB rms
Accuracy					
Integral Nonlinearity (INL)	Note 1		$\pm$0.75		LSB
Differential Nonlinearity (DNL)	Note 1		$\pm$0.50		LSB
No Missing Codes	Bits Guaranteed[2]	16			Bits
Offset Error	Note 2		0.09	0.5	% FSR
Gain Error	Note 2,3,4		0.4	1.5	% FSR
Temperature Drift					
Offset Error			1.1		ppm/C
Gain Error			38		ppm/C
Power Supply Rejection					
DC Supply Rejection			0.064		% FSR/V
AC Supply Rejection	50mV (p-p) 100kHz		-61.5		dB
Analog Input					
Input Span	V_{REF} = 2.0V			4.0	V_{p-p} Diff
Input Range		0.5		AVDD-0.5	V
Common Mode Rejection	100kHz, 1.2Vp-p input		-61.5		dB
Input Capacitance			10		pF
Internal Voltage Reference					
Output Voltage (VCM)	Note 2	2.350	2.500	2.650	V
Power Supplies					
AVDD & SVDD		4.75	5	5.25	V
DVDD		2.7	3	AVDD	V
Low Power Bias (Rbias = 6.3k ohms)					
I(AVDD + SVDD)	500kHz Input, -0.5dBFS		53		mA
I(DVDD + RVDD)			17.5		mA
Power Consumption			317.5		mW
High Performance Bias (Rbias = 3.9k ohms)					
I(AVDD + SVDD)	500kHz Input, -0.5dBFS[2]		75		mA
I(DVDD + RVDD)			17.5		mA
Power Consumption			427.5	452.5	mW

PERFORMANCE SPECIFICATION (continued)

AC SPECIFICATION (8x Mode)

AVDD = +5V, DVDD= +3V, f_{CLOCK} = 20 MSPS, Input CML = 2.5V, Input Amplitude: -0.5dBFS, T_{MAX}=85C, T_{MIN}=-40C, Rbias=3.9k unless specified otherwise

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
DYNAMIC PERFORMANCE					
Input Test Frequency: 100 KHz					
Signal to Noise (SNR)	Note 2	86.5	89.5		dB
	-6 dBFS input		84.5		dB
	Low Power Bias[5]	86.5	89.5		dB
SNR + Distortion (SINAD)	Note 2	84	88.5		dB
	-6 dBFS input		84.5		dB
	Low Power Bias[5]	81	88		dB
Total Harmonic Distortion (THD)	Note 2		-98	-88	dB
	-6 dBFS input		-101		dB
	Low Power Bias[5]		-96.5	-81.5	dB
Spurious Free Dynamic Range (SFDR)		90	100		dB
	-6 dBFS input		106		dB
	Low Power Bias[5]	85	100		dB
Input Test Frequency: 500 KHz					
Signal to Noise (SNR)			89.5		dB
	-6 dBFS input		85		dB
	Low Power Bias		89.5		
SNR + Distortion (SINAD)			89		dB
	-6 dBFS input		85		dB
	Low Power Bias		89		dB
Total Harmonic Distortion (THD)			-106		dB
	-6 dBFS input		-102		dB
	Low Power Bias		-100		dB
Spurious Free Dynamic Range (SFDR)			106		dB
	-6 dBFS input		102		dB
	Low Power Bias		100		dB
Input Test Frequency: 1 MHz					
Signal to Noise (SNR)			89		dB
	-6 dBFS input		84.5		dB
	Low Power Bias		89		dB
Spurious Free Dynamic Range (SFDR)			102		dB
	-6 dBFS input		102		dB
	Low Power Bias		100		dB
INTERMODULATION DISTORTION					
f_{IN1} = 452 kHz, f_{IN2} = 500 kHz	-6.5 dBFS inputs		102.5		dBFS
f_{IN1} = 905 kHz, f_{IN2} = 1 MHz	-6.5 dBFS inputs		98		dBFS

PERFORMANCE SPECIFICATION (continued)

DYNAMIC CHARACTERISTICS					
Full Power Bandwidth	-3 dB point		160		MHz
Small Signal Bandwidth (AIN = -20 dBFS)	-3 dB point		160		MHz

AC SPECIFICATION (4 X Mode)

AVDD = +5V, DVDD= +3V, f_{CLOCK} = 20 MSPS, Input CML = 2.5V, T_{MAX}=85C, T_{MIN}=-40C Input Amplitude = -0.5dBFS, Rbias=3.9k unless specified otherwise.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
DYNAMIC PERFORMANCE					
Input Test Frequency: 100 KHz					
Signal to Noise (SNR)			82		dB
	-6 dBFS input		77		dB
	Low Power Bias		82		dB
SNR + Distortion (SINAD)			81.5		dB
	-6 dBFS input		77		dB
	Low Power Bias		81.5		dB
Total Harmonic Distortion (THD)			-98		dB
	-6 dBFS input		-99		dB
	Low Power Bias		-97		dB
Spurious Free Dynamic Range (SFDR)			100		dB
	-6 dBFS input		97		dB
	Low Power Bias		99.5		dB
Input Test Frequency: 1 MHz					
Signal to Noise (SNR)			80.5		dB
	-6 dBFS input		77		dB
	Low Power Bias		80.5		dB
SNR + Distortion (SINAD)			80		dB
	-6 dBFS input		76		dB
	Low Power Bias		80		dB
Total Harmonic Distortion (THD)	-0.5 dBFS input		-90		dB
	-6 dBFS input		-90		dB
	Low Power Bias		-90.5		dB
Spurious Free Dynamic Range (SFDR)	-0.5 dBFS input		90		dB
	-6 dBFS input		89.5		dB
	Low Power Bias		90.5		dB

PERFORMANCE SPECIFICATION (continued)

DIGITAL FILTER CHARACTERISTICS

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
ADC Digital Filter (8 X Decimation)					
Passband		0		1.01	MHz
Stopband		1.49		19.51	MHz
Passband Ripple				±0.004	dB
Stopband Attenuation		85.5			dB
Group Delay			11		µs
Group Delay Variation			0		µs
Settling Time (to ± 0.0007%)			17		µs
ADC Digital Filter (4 X Decimation)					
Passband		0		2.02	MHz
Stopband		2.98		39.02	MHz
Passband Ripple				±0.004	dB
Stopband Attenuation		85.5			dB
Group Delay			3.95		µs
Group Delay Variation			0		µs
Settling Time (to ± 0.0007%)			6.35		µs

DIGITAL SPECIFICATION

AVDD = +5V, DVDD = +3V, T_{MAX}=85C, T_{MIN}=-40C

Parameter		Conditions/Comments	Min.	Typical	Max	Units
VIH	High Level Input Voltage	Clock Pin	0.7*SVDD			V
VIL	Low Level Input Voltage	Clock Pin			0.3*SVDD	V
VIH	High Level Input Voltage	Read, CSB, & RSTB Pins	0.7*DVDD			V
VIL	Low Level Input Voltage	Read, CSB, & RSTB Pins			0.3*DVDD	
VIH	High Level Input Voltage	Mode Pin	0.35*AVDD		0.5*AVDD	V
VIL	Low Level Input Voltage	Mode Pin			0.1*AVDD	
VOH	High Level Output Voltage	Iout = 90 uA	RVDD-0.4			V
VOL	Low Level Output Voltage	Iout = 90 uA			0.4	V
I_{IL}	Input Leakage Current				±0.1	uA

Notes

1. Conventional INL and DNL measurements do not really apply to delta sigma converters: the DNL looks continually better if longer data records are taken. The AK2700, INL and DNL numbers are given as representative.The code density test produces a histogram of the digital output codes of an ADC sampling a known input. The code density can be intepreted to compute the differential and integral non-linearities, gain error, offset error and internal noise. A 100 kHz , -0.55dBFS tone is used as an input.
2. 100% production tested at 85C and sample tested at other specified temperature.
3. The specification excludes the variation in the voltage reference.
4. The AK2700 has a maximum code of 7FBD and a minimum code of 8042, introducing a gain error of ±0.4% FSR. The gain error is measured using the "code density test" with a 100 kHz input at -0.55 dBFS.
5. Low Power Bias minimum and maximum specifications are guaranteed by test corelation. In this mode the second harmonic has a stronger dependence on temperature resulting in a greater spread of THD and SFDR specifications.

Absolute Maximum Ratings

AVSS, SVSS,RVSS and DVSS = 0V. All voltages are with respect to ground.

Parameter		Min.	Max.	Units
Power Supplies				
VA	Analog Power Supply	-0.3	6.0	V
VD	Digital Power Supply	-0.3	6.0	V
GND	Difference between AVSS, SVSS, RVSS and DVSS		0.3	V
IIN	Input Current—All pins except supply pins		±10	mA
VINA	Analog Input Voltage	-0.3	VA + 0.3	V
VIND	Digital Input Voltage	-0.3	VD + 0.3	V
Temperature				
Ta	Ambient Operating Temperature (Power Applied)	-40	80	°C
Tstg	Storage Temperature	-65	150	°C

Recommended Operation Conditions

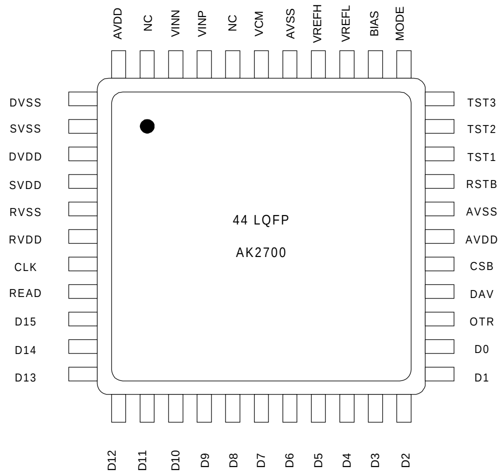
AVSS, SVSS, RVSS, and DVSS = 0V. All voltages are with respect to ground.

Parameter		Min.	Typ.	Max.	Units
Power Supplies[1]					
VA	Analog Power Supply (AVDD & SVDD)	4.75	5.0	5.25	V
VD	Digital Power Supply (DVDD & RVDD)	2.7	3.0	VA	V

PIN DESCRIPTION

No.	Pin Name	I/O	Pin Function and Description
1	DVSS		**Digital Ground,** DGND=0V
2	SVSS		**5V Digital Ground.** SGND=0V
3	DVDD		**Digital Power Supply.** DVDD = 3/5V
4	SVDD		**Digital Power Supply.** SVDD = 5V
5	RVSS		**Digital Output Ground.** RGND=0V
6	RVDD		**Digital Output Supply** RVDD=3/5V
7	CLK	I	**Master Clock.** Referenced to AVDD
8	READ	I	**Output Enable** - Active high
9-24	D15-D0	O	**Data Output** (LSB = Pin9 and MSB = Pin 24)
25	OTR	O	**Data Out of Range Flag -** Set when converter or filter overflows
26	DAV	O	**Data Valid Flag** - Data Available
27	CSB	I	**Chip Select** - Active Low
28	AVDD		**Analog Supply.** AVDD = 5V
29	AVSS		**Analog Ground.** AGND = 0V
30	RSTB	I	**Reset -** Active Low
31	TST1	I	**Connected to 0V - AGND**
32	TST2	I	**Connected to 0V - AGND**
33	TST3	I	**Connected to 0V. -AGND**
34	MODE	I	**Selects Decimation Ratio**
35	BIAS	O	**Bias Resistance - 3.9 K ohms (High Performance Mode) & 6.3 kohms (Low Power Mode)**
36	VREFL	O	**Negative Reference Pin**
37	VREFH	O	**Positive Reference Pin**
38	AVSS		**Analog Ground.** AGND = 0V
39	VCM	O	**Common Mode Reference Pin**
40	NC		**No Connect**
41	VINP	I	**Positive Analog Input**
42	VINN	I	**Negative Analog Input**
43	NC		**No Connect**
44	AVDD		**Analog Supply.** AVDD = 5V

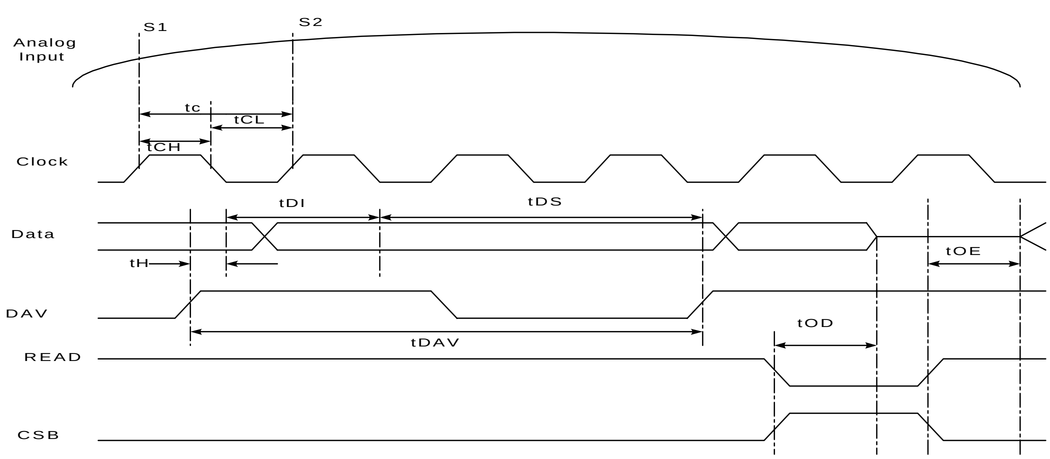
PINOUT



DIGITAL SWITCHING CHARACTERISTICS

AVDD = +5V, DVDD=3V, CL=20pF, T_{MAX}=85C, T_{MIN}=-40C

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
tCLK	Clock Period		50			ns
tDAV	Data Available Period		tc x MODE			ns
tDI	Data Invalid				0.43 x tDA	ns
tDS	Data Setup time	tDAV-tH-tDI	235			ns
tCH	Clock Pulse Width High		22.5			ns
tCL	Clock Pulse Width Low		22.5			ns
tH	Data Hold Time		8.5			ns
tOD	Three-State Output Disable Time			6.2	15.2	ns
tOE	Three-State Output Enable Time			6	12	ns



THEORY OF OPERATION

The AK2700 is a 16 bit, 2.5MSPS Analog to Digital converter intended for high speed instrumentation, medical imaging and high resolution, high speed data acquisition. A novel delta-sigma modulator operating at 20Mhz employing multibit quantization and dynamic element matching techniques achieves 89dB signal to noise performance, with a 100dB of spurious free dynamic range and a low power dissipation of 315mW.

The on-chip decimation filter provides excellent stop-band rejection to suppress any stray signal between 1.49MHz and 18.51Mhz, substantially easing the requirements of any anti-aliasing filter for the analog input path.

The AK2700 features READ and CSB pins to allow for easy interfacing. A digital supply of 5.25 to 2.7V can be used, though a 3V supply is recommended to minimize digital noise on the board. A Data available pin (DAV) allows the user to easily synchronize to the converter's decimated output data rate. The OTR pin indicates an overflow condition within the modulator and the digital filters. The RSTB pin is provided to synchronize the converter's decimated data and clear any overflo conditions.

An on-chip reference and reference buffer provides a 2.5V reference for a 4V pk-pk differential input full scale.

Analog Input and Reference Overview

The value of VCM defines the maximum input voltage to the AK2700. An internal reference buffer scales the VCM of 2.5V to create VREFH and VREFL. The scale factor for these buffers is 0.8. Thus the maximum input voltage to the A/D is defined to be +0.8 x VCM = +2V to -0.8 x VCM = -2V.

INPUT SPAN

The AK2700 is implemented with a differential input structure. This allows the common mode of the input voltage to be varied independent of the input span of the converter. The input to the A/D core is the difference of the voltages applied at the VINA and VINB input pins. This difference must be less than 4V pk-pk.

INPUT RANGE

The analog input structure bounds the valid operating range of operation to AVSS + 0.5 < VIN < AVDD - 0.5V, where AVSS is 0V and AVDD is nominally +5V.

INPUT DRIVER CONSIDERATION

The optimum noise and distortion performance of the AK2700 is achieved when the device is driven differentially with a 4V input span. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. This is best realized using a differential op amp driver

SINGLE-ENDED TO DIFFERENTIAL OP AMP DRIVER

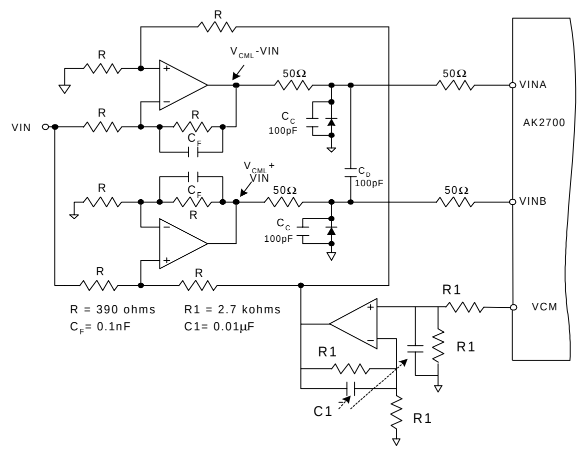


Figure 2: DC Coupled Differential Driver with Level Shifting

There are two particular single-ended-to-differential op amp driver circuits useful for driving the AK2700. The first circuit is shown in figure 2 is optimized for dc coupling applications requiring optimum distortion performance. This circuit converts and level shifts a 2 Vp-p single-ended, ground referenced signal to a 4Vp-p differential signal centered at the common-mode level of the AK2700. The circuit is based on two op amps which are configured as matched unity gain difference amplifiers. The single ended input signal is applied to opposing inputs of the difference amplifiers, thus providing differential outputs. The common mode offset voltage is applied to the non-inverting resistor leg of each difference amplifier, thus providing differential outputs. The offset voltage is derived from the VCM pin on the AK2700 via a low output impedance buffer amplifier capable of driving a 1uF capacitive load

To protect the AK2700 from an undervoltage fault condition from the op amps specified for ± 5V operation, two 50 ohm series resistors and a diode to AGND are inserted between each op amp output and the AK2700 inputs. The AK2700 will be inherently protected against an over voltage conditions if the op amps share the same positive power supply as the AK2700.

The gain accuracy and common mode rejection of each of the difference amplifiers can be enhanced by using a matched thin-film resistor network for the op amps. These values should be less than 500 ohms to maintain the lowest possible noise. The noise gain can be reduced by adding a shunt capacitor, across each op amp's feedback resistor. This will essentially establish a low pass filter that will reduce the noise gain to one beyond the cutoff while simultaneously band limiting the input signal. For the lowest possible noise performance while maintaining excellent distortion performance, the unity gain OPA642 should be considered.

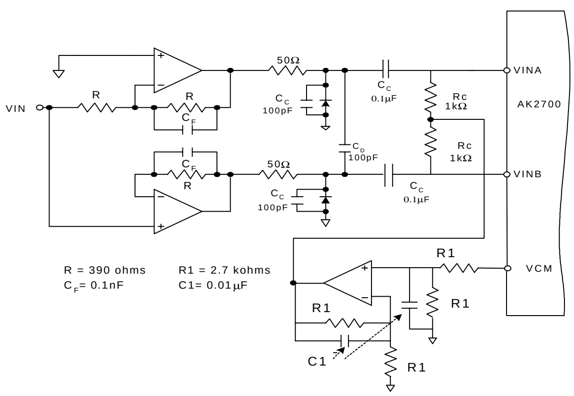


Figure3: AC Coupled Low Noise Differential Driver

The lowest possible noise and distortion performance can be achieved using an ac coupled circuit, shown in figure. The circuit consists of two low noise, high speed op amps configured as an inverting gain of one and a unity gain buffer. In this configuration, the noise performance is dominated by the inverting op amp topology due to it' noise gain of two. Excellent distortion is achieved as the op amps are centered around AGND. The outputs of each op amp are ac coupled via a small series resistor and capacitor to the respective inputs of the AK2700. Further out of band noise reduction can be realized with an addition of 100pF single ended and differential capacitors. The lower cutoff frequency of this ac coupled circuit is determined by Rc and Cc. The OP642 provides a low overall noise and distortion performance.

The VCM pin is an internal analog bias point used internally by the AK2700. This pin must be decoupled to analog ground with atleast a 0.1 uF and 10uF capacitor. This voltage (2.5V) should be buffered if it is to be used for any external biasing.

REFERENCE OPERATION

The AK2700 contains an integrated bandgap reference and a internal reference buffer amplifier. This reference generates a 2.5V. The actual voltages used by the internal circuitry of the AK2700 appear on the VREFH and VREFL pins. For proper operation, it is necessary to add a capacitive network to decoupled the pins. All digital switching lines must be drawn away from these pins.

DIGITAL INPUTS AND OUTPUTS

DATA OUTPUT

The AK2700 output data is presented in a two's complement format.

CSB AND READ PIN

These pins control the state of the output data pins on the AK2700. The CSB pin is active low and the READ pin is active high. When both the pins are active the ADC data is driven on the output data pins, otherwise the output data pins are in a high impedance (Hi-Z) state.

DAV PIN

The DAV pin indicates when the output data is valid. Digital output data is updated on the rising edge of DAV The duty cycle of DAV is approximately 50% and it remains independent of CSB and READ

RSTB PIN

The RSTB pin is an asynchronous digital input that is active low. On assertion, the clocks in the decimation filter are disabled, theDAV pin goes low and the data on the output pins is invalid. In addition, the analog modulator clocks are also reset as long as RSTB is maintained low. The RSTB must remain low for at least a clock period to ensure all the dividers and modulators are reset.

The RSTB may be used to synchronized multiple AK2700 clocked with the same clock. In order to synchronize it is necessary that the clock dividers in each AK2700s are all reset at the same state. On the third rising edge of CLK following the rising edge of RSTB, the input is sampled synchronously.

OTR PIN

The OTR pin is a synchronous output that is updated each CLK period. It indicates that an overrange conditions has occur within the AK2700. Ideally, OTR should be latched to the falling edge of CLK to ensure proper setup and hold time. OTR typically remains high for more than one clock cycle

The AK2700 can be used in systems that incorporate automatic gain control. The OTR signal may be used to indicate that the signal amplitude should be reduced.

MODE PIN

The Mode pin allows the user to use the 4x mode of the decimator. When connected between 0 to 0.5V or ground the AK2700 is in the 8x mode of operation. When connected to 1.75 to 3.25V or VCM, the 4x mode is selected. A voltage higher than 0.9 timesAVDD puts the device in test mode.

BIAS PIN

The pin is connected to a 3.9k ohms in the high performance mode. The AK2700 can also be operated in the low power mode by connecting the bias resistor to 6.3k ohms. This resistor sets up the bias currents to all the analog circuitry. Minimization of capacitance to this pin is recommended in order to prevent instability of the bias pin amplifier.

DIGITAL OUTPUT CONSIDERATION

The AK2700 output drivers can be configured to interface with +5V or 3V logic families by setting RVDD to +5V or 3V. A large drive currents tend to cause glitches on the RVDD power rail. This may effect the SINAD performance. Applications requiring the AK2700 to drive large loads or large fannout may require additional decoupling capacitors on RVDD. The addition of external buffers or latches can reduce output loading while providing effective isolation.

CLOCK INPUT CONSIDERATION

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AK2700. The CLK input buffer is powered by a 5V analog supply and requires high and low levels of 3.5V and 1V respectively. Supplies of the clock buffers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock source

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Multi layer printed circuit boards (PCBs) are recommended to provide for optimal grounding and power schemes. The use of ground and power planes results in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While AK2700 features separate analog and digital pins, it should be treated as an analog component.

Analog and Digital Supply Decoupling

The analog and digital supplies should be decoupled as close to the chip as physically possible. A combination of 0.1uF and 10uF should be connected between each pair of power supplies: AVDD and AVSS, DVDD and DVSS, SVDD and SVSS, and RVDD and RVSS. An external decoupling and bias network is shown in figure 4.

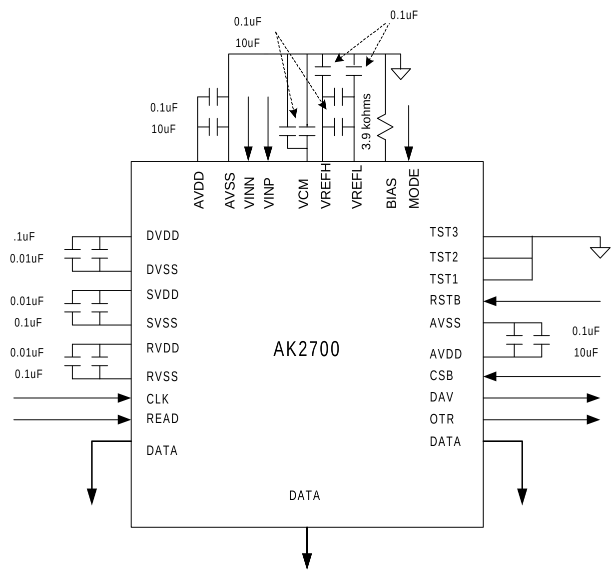
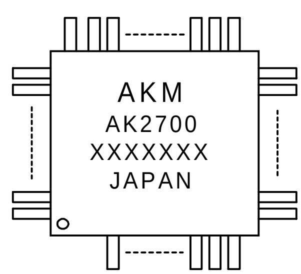


Figure4: Decoupling and Bias Connection for AK2700

Marking Spec



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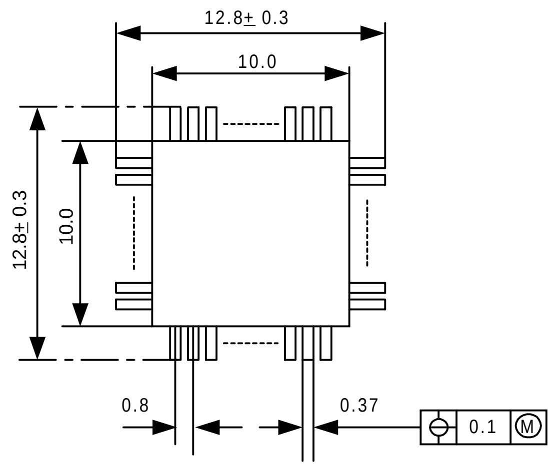
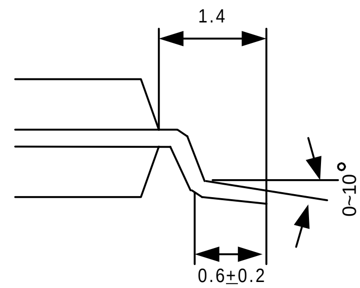
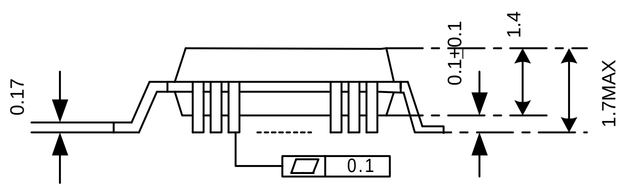
OUTLINE DIMENSION







44-Lead LQFP

Dimensions shown in millimeters

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