# SuperH RISC Engine Family High-Performance 32-Bit RISC Microcomputers with Large-Capacity On-Chip Flash Memory

## SH7044F, SH7045F

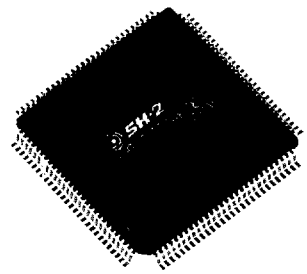
**Main Uses**

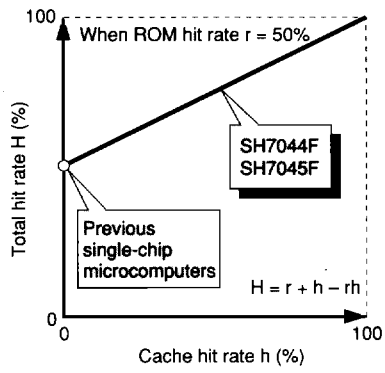
**• Digital video cameras, digital still cameras, Internet TVs, DVD players, various multimedia products, HDDs, printers, fax machines, PPCs, motor control, electric vehicles, etc.**

- Large 256-kbyte on-chip flash memory
- Easy-to-use single-power-supply flash memory
- Large-capacity ROM and cache memory included on-chip, enabling single-cycle execution of most programs
- High-speed processing: 28–33 MIPS (28–33 MHz/5 V)
- Powerful on-chip supporting functions, including DMAC, timers, serial I/O, and A/D converter
- Direct interfacing to various kinds of external memory (SRAM, DRAM)

Recent years have seen a growing demand, in both consumer and industrial fields, for field programmability, offering the ability to change parameters or adjust control data while equipment is operating, and to modify microprograms at any stage—from development through trial production, initial mass production, and final mass production—in order to shorten the product development time or improve product specifications. In response to this demand, Hitachi developed its range of F-ZTAT™*1 microcomputers, featuring on-chip flash memory. These products have made significant inroads into the microcomputer market.

Hitachi is now releasing two models in the SH7040 Series—the SH7044F and SH7045F. These 32-bit single-chip RISC microcomputers, featuring large-capacity on-chip flash memory which can be programmed using a single power supply, are designed for application fields requiring high-speed, high-precision control. They have up to 256 kbytes of flash memory and are capable of single-cycle access operation at a maximum operating frequency of 28 to 33 MHz (5 V). In other words, each instruction in a program located in the on-chip flash memory can be executed in one cycle, giving a high instruction execution performance figure of 28 to






The proportion of instructions that can be fetched in one cycle (total hit rate) H is shown on the left for different values of cache hit rate h, assuming that the proportion of instructions executed in on-chip ROM (ROM hit rate) r is 50%.
The graph illustrates the improvement in overall performance compared with previous microcomputers with on-chip ROM alone.

**Fig. 1 Single-Cycle Program Execution Performance**

33 MIPS (28 to 33 MHz/5 V). This series also features on-chip cache, enabling high-speed single-cycle execution, when cache hits are made, of external programs that exceed the capacity of the on-chip ROM. Single-cycle execution can thus be achieved for most programs, improving overall system processing performance. This makes these new microcomputers ideal for use in multimedia products that require processing of enormous quantities of mixed (e.g. image and voice) data, and in high-performance industrial equipment in areas such as high-speed, high-precision servo control.

A comprehensive range of on-chip supporting functions are also provided, including a DMAC, timers, serial I/O, A/D converter, and a facility for direct connection of external memory (SRAM or DRAM), enabling a compact end-product to be created while keeping system costs down.

Some earlier devices required a separate power supply (12 V, for example) for programming and erasing on-chip flash memory. However, these new SH7040 Series models include a built-in step-up circuit that eliminates the need for a separate external power supply, simplifying the design of the end-product power supply.

As with previous F-ZTAT™ microcomputers, a convenient block-erase function is supported in addition to total-memory erasing. The flash memory is divided into twelve large and small blocks, and erasing can be specified for only those blocks requiring it. This feature is useful for adjusting application system control data, for example.

## Features

**■ 33 MIPS/5 V SH-2 core**

- 33 MIPS performance at 33 MHz
- 28 MIPS performance at 28 MHz

**■ Single-power-supply, 256-kbyte on-chip flash memory**

- On-board microprogram and control data modifications can be made at any stage, from development through trial production, initial mass production, and final mass production.
- The provision of an on-chip step-up circuit eliminates the need for a separate power supply (e.g. 12 V) for data programming and erasing, simplifying end-product power supply design.

**■ 1-kbyte on-chip cache**

- With a large on-chip ROM capacity of 256 kbytes, most programs requiring high-speed processing can be executed at a fast single-cycle rate within the sys-

**Table 1 SH7040 Series Specifications**

| Item | SH7044F (HD64F7044) | SH7045F (HD64F7045) |
|---|---|---|
| Power supply | 5 V | 3.3 V |
| Operating frequency | 33 MHz/28.7 MHz | 16.7 MHz |
| Processing speed | 33 MIPS/28.7 MIPS | 16.7 MIPS |
| CPU core | 32-bit original RISC SH-2 core | |
| CPU instructions | 62 kinds (all 16-bit fixed-length instructions) | |
| DSP functions | 32 bits × 32 bits → 64 bits: 2–4 cycles<br>32 bits × 32 bits + 64 bits → 64 bits: 2–4 cycles<br>16 bits × 16 bits → 32 bits: 1–3 cycles<br>16 bits × 16 bits + 64 bits → 64 bits: 2–3 cycles | |
| On-chip flash memory | 256-kbyte F-ZTAT™ version (32-bit single-cycle access capability)<br>Single-power-supply programming/erasing | |
| On-chip RAM | 4 kbytes (32-bit single-cycle access capability) | |
| On-chip cache | 1-kbyte instruction cache (direct mapping)<br>Doubles as 2 kbytes of on-chip RAM<br>(1 kbyte for address array, 1 kbyte for data array) | |
| External memory | Direct connection of SRAM/DRAM possible by means of bus state controller<br>Four 4-Mbyte SRAM areas, one 16-Mbyte DRAM area<br>Provision for idle cycle insertion to prevent bus collisions<br>Data bus width: SH7044F: external 16-bit; SH7045F: external 32-bit | |
| On-chip supporting functions | Four DMAC channels<br>Data transfer controller (DTC): 34-channel simple DMAC<br>Multifunction timer pulse unit (MTU): 5-channel high-functionality timer<br>Eight 10-bit-resolution A/D converter channels<br>Two serial communication interface (SCI) channels<br>Two compare match timer channels<br>Interrupt controller (INTC)<br>User break controller (UBC)<br>Parallel I/O port<br>Watchdog timer (WDT)<br>Clock pulse generator (CPG): built-in multiplying PLL | |
| Packages | QFP112 (0.65 mm pitch, 20 mm × 20 mm) | QFP144 (0.5 mm pitch, 20 mm × 20 mm) |
| Power consumption | 600 mW (typ.) at 5 V, 33 MHz; 300 mW (typ.) at 3.3 V, 16.7 MHz | |
| Process | 0.6 µm 2-layer aluminum CMOS process | |

tem. The provision of on-chip cache also enables high-speed single-cycle execution, when cache hits are made, of external programs that exceed the capacity of the on-chip ROM. This allows almost all program instructions to be executed in a single cycle.

■ **External memory interface**

• Various kinds of memory devices, including SRAM and DRAM, can be directly connected

■ **Four DMAC channels**

■ **34 DTC channels**

• Simple DMAC capable of data transfer in response to requests from on-chip supporting modules

■ **Two SCI channels**

■ **Five MTU channels**

• Six-phase non-overlap waveforms for inverter drive can be output without program intervention.

■ **Two CMT channels**

• Generation of interval interrupts for use as realtime OS time base

■ **A/D converter**

• Eight 10-bit-resolution channels

■ **Interrupt controller**

■ **User break controller**

• Interrupts can be generated in the specified bus cycles.

• Enables construction of an on-chip debugger.

■ **Parallel I/O port**

■ **Watchdog timer**

■ **Packages**

• SH7044F: QFP112

• SH7045F: QFP144

■ **Operating voltage, operating frequency (performance)**

• 5 V, 33 MHz (33 MIPS)

• 5 V, 28.7 MHz (28.7 MIPS)

• 3.3 V, 16.7 MHz (16.7 MIPS)

■ **Process**

• 0.6 µm Al 2-layer CMOS

## From Our Engineer

Future plans for the SH7040 Series include phased development of higher-performance (33 MHz/33 MIPS) versions of current 128-kbyte-ROM ZTAT™*2 mask products SH7042 and SH7043, and products with mask implementation of the present ROM, plus SH7040 and SH7041 mask ROM versions with a 64-kbyte ROM capacity. There are also plans for ongoing extension of the range of single-chip microcomputers for embedded applications in the SuperH™*3 microcomputer family, with a lineup featuring a higher operating frequency and expansion of on-chip memory and on-chip supporting functions.

*1: F-ZTAT is a trademark of Hitachi, Ltd.
*2: ZTAT is a trademark of Hitachi, Ltd.
*3: SuperH is a trademark of Hitachi, Ltd.

**Table 2 SH7040 Series Product Lineup**

| Type | Name | On-Chip ROM | External Bus Width | Package | Operating Temperature | Frequency | Voltage | Development Status |
|---|---|---|---|---|---|---|---|---|
| ZTAT | SH7042* | 128 kbytes | 16 bits | QFP2020-112 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Ok<br>Ok |
| | SH7043 | 128 kbytes | 32 bits | QFP2020-144 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Ok<br>Ok |
| FLASH | SH7044 | 256 kbytes | 16 bits | QFP2020-112 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Under development<br>Under development |
| | SH7045 | 256 kbytes | 32 bits | QFP2020-144 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Under development<br>Under development |
| MASK | SH7040 | 64 kbytes | 16 bits | QFP2020-112 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Under development<br>Under development |
| | SH7041 | 64 kbytes | 32 bits | QFP2020-144 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Under development<br>Under development |
| | SH7042* | 128 kbytes | 16 bits | QFP2020-112 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Ok<br>Ok |
| | SH7043* | 128 kbytes | 32 bits | QFP2020-144<br>LQFP2020-144** | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Ok<br>Ok |
| | SH7044 | 256 kbytes | 16 bits | QFP2020-112 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Ok<br>Under development |
| | SH7045 | 256 kbytes | 32 bits | QFP2020-144 | –20 to 75°C | 33 MHz<br>28 MHz<br>16 MHz | 5 V<br>5 V<br>3.3 V | Planned<br>Ok<br>Under development |

*: These products are available in a number of mask versions with different specifications. For details, contact your Hitachi sales representative.
**: Under development