Product Brief
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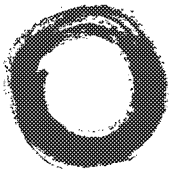

Lucent Technologies
Bell Labs Innovations

TTSI2K32T
2048-Channel, 32-Highway Time-Slot Interchanger

Features

- Thirty-two full-duplex, serial time-division multiplexed (TDM) highways.
- Full availability, nonblocking 2048-channel time/space switch.
- 2.048 Mbits/s (32 time slots), 4.096 Mbits/s (64 time slots), or 8.192 Mbits/s (128 time slots) data rates, independently programmable per highway.
- 64 kbits/s granularity with optional 32 kbits/s (4-bit) and 16 kbits/s (2-bit) subrate switching, selectable per highway.
- Low-latency mode for voice channels.
- Frame integrity for wideband data applications.
- Concentration highway interface (CHI) compatible with the IOM2, GCI, K2, SLD, *MVIP**, ST-Bus, SC-Bus, and H.100.
- Single highway clock and frame synchronization input.
- Independently programmable bit and byte offsets with 1/4 bit resolution for all highways.
- Capable of broadcasting data to the transmit highways from a variety of sources including host data.
- High-impedance control per time slot.
- Software compatible family of 1K, 2K, and 4K time-slot interchangers.
- Thirty-two independent high-impedance indicators (output enables) for transmit highways, allowing external drivers.
- Direct access to device registers, connection store, and data store via microprocessor interface.
- *IEEE*† 1149.1 boundary scan (JTAG).
- Test-pattern generation and checking for on-line system testing (PRBS, QRSS, or user-defined byte).
- User-accessible BIST for data and connection stores.
- 3.3 V power supply with 5 V tolerant I/O.
- Low-power high-density CMOS technology, and TTL compatible switching thresholds.
- 217-pin PBGA package.
- –40 °C to +85 °C operating temperature range.

* *MVIP* is a registered trademark of Natural Microsystems Corporation.

† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Applications

- Small and medium digital switch matrices.
- Computer telephony integration (CTI).
- Access concentrators.
- PABX.
- Cellular infrastructure.
- ISP modem banks.
- T1/E1 multiplexers.
- Digital cross connects.
- Digital loop carriers.
- Multiport DS1/E1 service cards.
- LAN/WAN gateways.
- TDM highway data rate adaptation.

Description

The TTSI2K32T Time-Slot Interchanger (TSI) switches data between 32 full-duplex, serial time-division multiplexed highways. The TTSI2K32T can make any connection between 2048 input and output time slots.

Each of the 32 transmit and 32 receive highways can be independently programmed for data rate (2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s) and offset. The offset can range from 0 bits to 127 bytes and 7 3/4 bits on an 8.192 Mbits/s highway. The TTSI2K32T can perform rate adaptation between varying speed highways as well.

The TTSI2K32T is configured via a microprocessor interface with a demultiplexed address and data bus. In addition to accessing the registers and connection store, this interface can also be used to read received time slots and specify user data for transmission.

The TTSI2K32T ensures that interchanged time slots retain their frame integrity. Frame integrity is required for applications that switch wideband data (i.e., ISDN H-channels). For voice applications where low delay is important, a low-latency mode can be selected.

Functional Description

The TTSI2K32T is a 2048 time-slot switch that can be used in a variety of ways, with some or all of the highways active and running at different data rates. The table below lists a few of the possible combinations of switch size and data rates. By selecting different rates for receive and transmit highways, rate adaptation can be performed also. Each one of the 64 (32 transmit and 32 receive) highways can be independently programmed for data rate (2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s) as well as a full range of bit (0—7.75) and byte (0—127) offsets.

Table 1. Data Rate and Switch Size Examples

Number of Receive Highways Used	Receive Highway Data Rates (Mbit/s)	Receive Time Slots per Frame	Total Switch Size	Number of Transmit Highways Used	Transmit Highway Data Rates (Mbits/s)	Transmit Time Slots per Frame
32	4.096	64	2048	32	4.096	64
16	8.192	128	2048	16	8.192	128
16	8.192	128	2048	32	4.096	64
16 and 8	4.096 8.192	64 128	2048	10 and 11	4.096 8.192	64 128

This device uses a single clock (CK) and frame synchronization (FSYNC) signal for all highways. The CK rate can be 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz, and this speed is indicated to the device via the CKSPD [0—2] strap pins. A pulse is expected on the FSYNC pin once every 125 μs.

Each one of the 2048 time slots can be independently programmed in any one of the data modes listed below:

- Low latency
- Frame integrity
- Host data substitution
- Idle code substitution
- Test-pattern substitution (PRBS, QRSS, or a fixed byte)
- High impedance

The low-latency mode causes a receive highway time slot to be transmitted as soon as possible, which is dependent on the relative offset of the input and output time slots. This mode is useful for voice channels where it is important to keep the transmission delay to a minimum.

The frame-integrity mode will guarantee that all selected time slots received in a common frame will be transmitted together in a common frame. This mode is useful for wideband data (e.g., ISDN H-channels) where multiple time slots received in a single frame cannot be split across two transmit frames.

The TTSI2K32T is a nonblocking DS0 (64 kbits/s channel) switch where a time slot is 8 bits. Since each Rx and Tx highway data rate can be individually selected, the TTSI2K32T can also be used to switch time slots that are smaller than 8 bits.

- 32 kbits/s channels (4-bit time slots) such as in compressed voice (ADPCM) applications. The TTSI2K32T will be configured to sample the data at twice the data rate for highways carrying traffic at 2.048 Mbits/s or 4.096 Mbits/s.
- 16 kbits/s channels (2-bit time slots) such as in cellular (GSM) applications. The TTSI2K32T will be set to sample the data at four times the data rate on a 2.048 Mbits/s highway carrying such traffic.
- 8 kbits/s channels (1-bit time slots) such as in half-rate GSM applications. This can be done by looping the data through the TSI multiple times, thus oversampling the same data multiple times. However, in this configuration the total switching capacity of the device will drop and the latency will go up.

The TTSI2K32T is one in a family of 1K, 2K, and 4K TSIs. The high-impedance control per time-slot feature allows four of the 4K devices to be connected to make an 8K time-slot switch.

If external drivers are needed on the transmit highway pins, support for 32 output enables, corresponding to the 32 transmit highway, is provided.

Functional Description (continued)

The device capabilities include several test features for board and device diagnostics.

- Test-pattern checking on input time slots (PRBS, QRSS, or a fixed byte).
- Test-pattern generation on output time slots (PRBS, QRSS, or a fixed byte).
- JTAG on all I/O.
- Software-controlled BIST of data store and connection store memory.
- $\overline{\text{TEST}}$ pin for isolating the TTSI2K32T during board test.

The microprocessor interface supports two modes of operation, synchronous and asynchronous. These modes are selected based on the MM input pin. Both modes provide an 8-bit demultiplexed address and data bus. Fifteen address pins allow direct access to the 32K byte address space. This interface provides direct access to the control registers, data store and connection store memories.

The TTSI2K32T is fabricated using a low-power, high-density, CMOS process that nominally operates at 3.3 V with TTL switching thresholds and 5 V tolerance on the inputs and outputs. A basic block diagram of the architecture is shown in Figure 1.

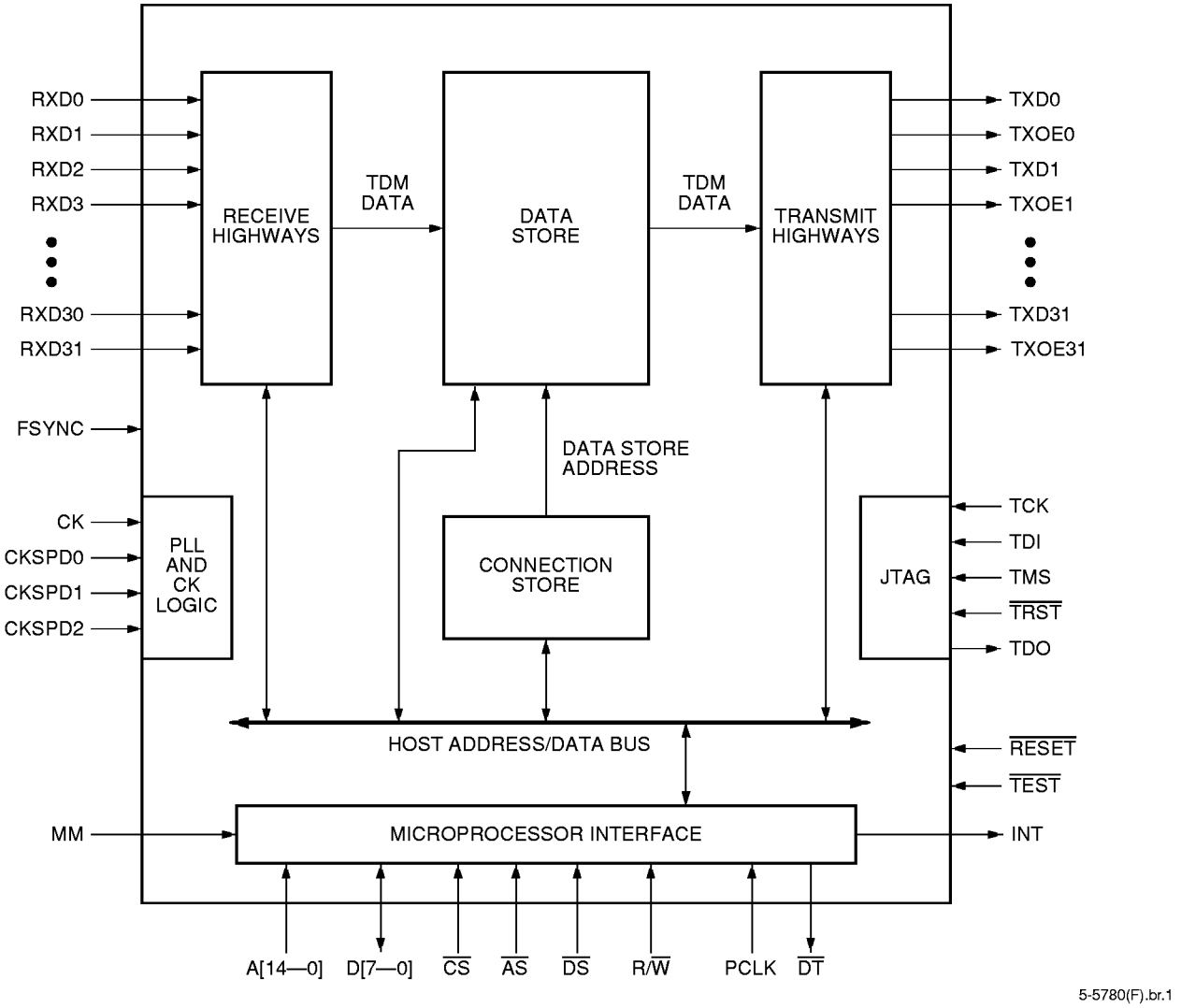

Figure 1. Block Diagram of the TTSI2K32T

Typical TSI Application

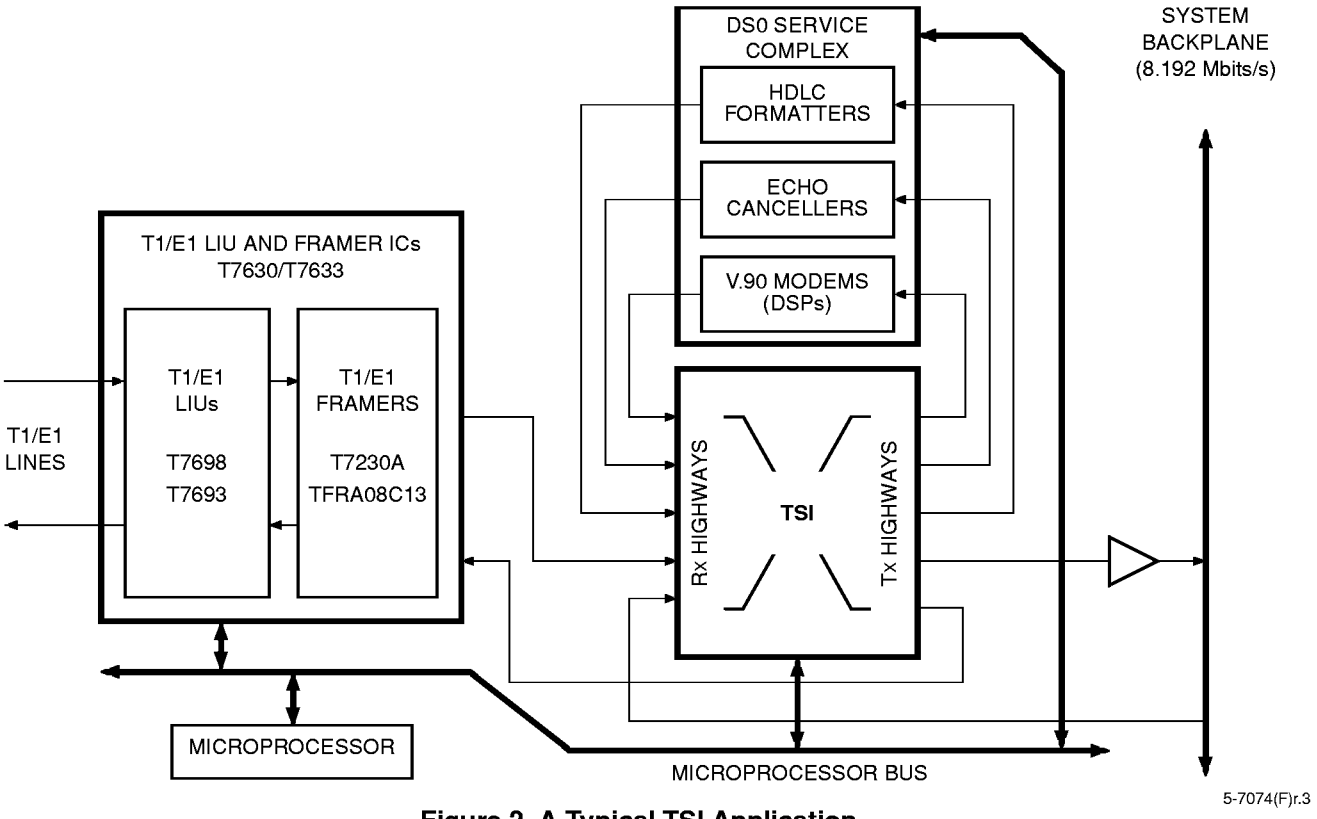

Figure 2. A Typical TSI Application

A typical application that requires a TSI is where TDM highways that are carrying different types of data in 8-bit time slots (64 kbits/s channels) need to be switched and sent to different destinations. For example, TDM highways may contain time slots that are carrying voice, Internet traffic, signaling information, etc.

The TSI could be programmed to select all the time slots, carrying Internet data from different Rx highways to be put on a another Tx highway that is connected to a bank of V.90 modems. Return data from these modems would be sent via another set of Rx highways back to the TSI, which could send the data back out over a Tx highway and to a T1 line via a T1 framer and LIU.

Similarly, time slots containing signaling information which is HDLC formatted can be sent to a bank of HDLC formatters. Voice channels that have echo on them, could be selectively sent to echo cancellers. Data that needs to be sent to another card in the system could be put on the system backplane via optional bus drivers.

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