# TM4416KU8
# 16,384 BY 8-BIT DYNAMIC RAM MODULE

SEPTEMBER 1985 — REVISED NOVEMBER 1985

- 16,384 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Two 16K X 4 Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

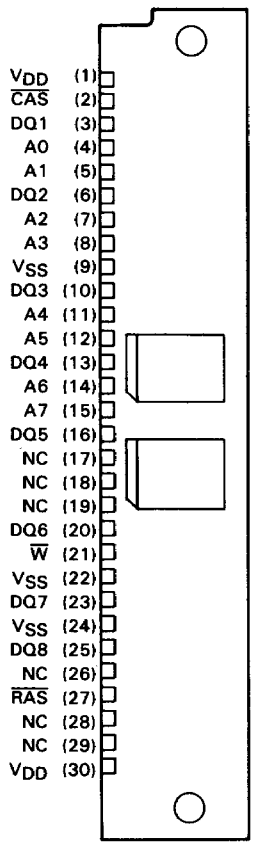
| | ACCESS TIME ROW ADDRESS (MAX) | ACCESS TIME COLUMN ADDRESS (MAX) | READ OR WRITE CYCLE (MIN) |
|---|---|---|---|
| TM4416KU8-12 | 120 ns | 70 ns | 230 ns |
| TM4416KU8-15 | 150 ns | 80 ns | 260 ns |

- Low Power Dissipation:

| | OPERATING (TYP) | STANDBY (TYP) |
|---|---|---|
| TM4416KU8-12 | 400 mW | 30 mW |
| TM4416KU8-15 | 350 mW | 30 mW |

- Operating Free-Air Temperature . . . 0°C to 70°C

U SINGLE-IN-LINE PACKAGE
(TOP VIEW)




## description

The TM4416KU8 is a 128K, dynamic random-access memory module organized as 16,384 × 8 bits in a 30-pin single-in-line package comprising two TMS4416FPL, 16,384 x 4 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with two 0.2 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance.

| PIN NOMENCLATURE | |
|---|---|
| A0-A7 | Address Inputs |
| $\overline{CAS}$ | Column-Address Strobe |
| DQ1-DQ8 | Data In/Data Out |
| NC | No Connection |
| $\overline{RAS}$ | Row-Address Strobe |
| $V_{DD}$ | 5-V Supply |
| $V_{SS}$ | Ground |
| $\overline{W}$ | Write Enable |

## operation

### address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the

chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

**write enable ($\overline{W}$)**

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The grounded output-enable ($\overline{G}$) dictates the use of early write cycles to prevent contention on DQ. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

**data in (DQ1-DQ8)**

Data is written during a write cycle. The falling edge of $\overline{CAS}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

**data out (DQ1-DQ8)**

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the grounded output enable.

**refresh**

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

**page mode**

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

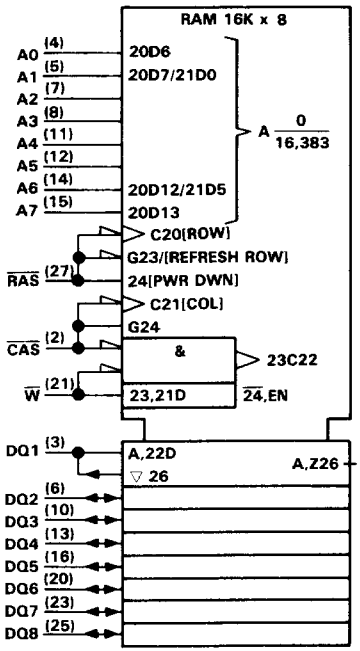
**power up**

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 $\mu$s immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

**single-in-line package and components**

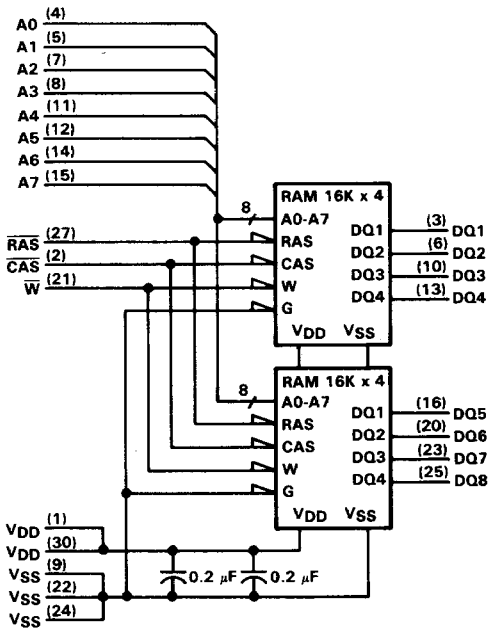
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitor: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate on top of copper

**logic symbol†**




†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**functional block diagram**




**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Voltage range for any pin except $V_{DD}$ and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range for $V_{DD}$ supply and data out with respect to $V_{SS}$ . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to $V_{SS}$.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies" in Section 12.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | | | 0 | | V |
| $V_{IH}$ | High-level input voltage | $V_{DD}$ = 4.5 V | 2.4 | | 4.8 | V |
| | | $V_{DD}$ = 5.5 V | 2.4 | | 5.8 | |
| $V_{IL}$ | Low-level input voltage (see Notes 3 and 4) | | −0.6 | 0 | 0.8 | V |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See Application Report entitled "TMS4164A and TMS4416 Input Diode Protection" on page 9-5.

## electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TM4416KU8-12 | | | TM4416KU8-15 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −2 mA | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4.2 mA | | | 0.4 | | | 0.4 | V |
| $I_I$ | Input current (leakage) | $V_I$ = 0 V to 5.8 V, $V_{DD}$ = 5 V, All other pins = 0 V | | | ±10 | | | ±10 | μA |
| $I_O$ | Output current (leakage) | $V_O$ = 0.4 V to 5.5 V, $V_{DD}$ = 5 V, $\overline{CAS}$ high | | | ±10 | | | ±10 | μA |
| $I_{DD1}$ | Average operating current during read or write cycle | $t_c$ = minimum cycle, All outputs open | | | 108 | | | 96 | mA |
| $I_{DD2}$ | Standby current | After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open | | | 10 | | | 10 | mA |
| $I_{DD3}$ | Average refresh current | $t_c$ = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open | | | 92 | | | 80 | mA |
| $I_{DD4}$ | Average page-mode current | $t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open | | | 92 | | | 80 | mA |

†All typical values are at $T_A$ = 25°C and nominal supply voltages.

## capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

| PARAMETER | | MAX | UNIT |
|---|---|---|---|
| $C_{i(A)}$ | Input capacitance, address inputs | 14 | pF |
| $C_{i(RC)}$ | Input capacitance, strobe inputs | 20 | pF |
| $C_{i(W)}$ | Input capacitance, write-enable input | 20 | pF |
| $C_{i/o}$ | Input/output capacitance, data ports | 10 | pF |





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**switching characteristics over recommended supply voltage range and operating free-air temperature range**

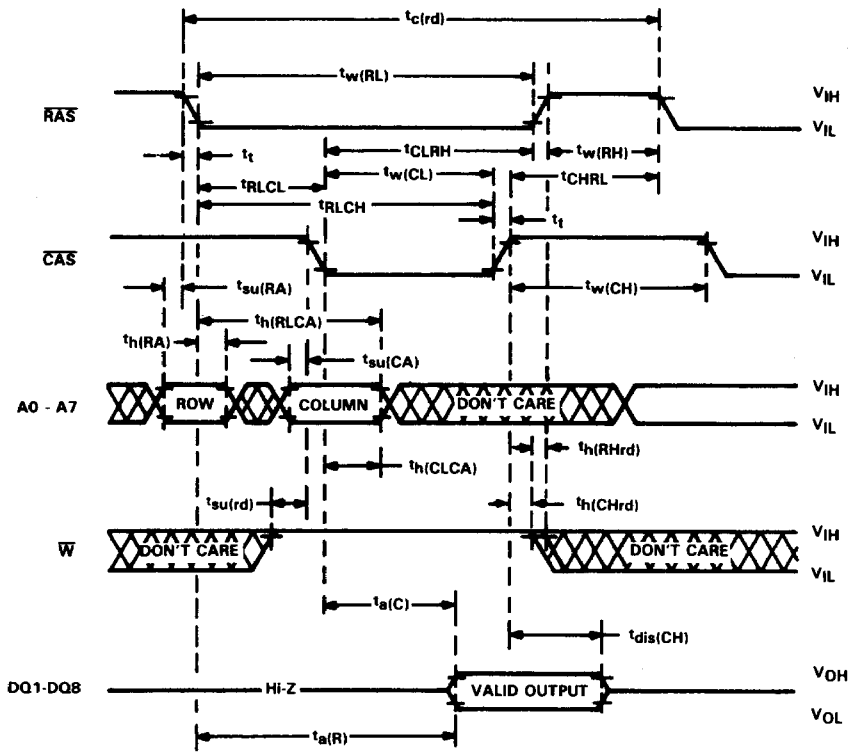
| PARAMETER | | TEST CONDITIONS | ALT. SYMBOL | TM4416KU8-12 | | TM4416KU8-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $t_{a(C)}$ | Access time from $\overline{CAS}$ | $C_L$ = 100 pF, Load = 2 Series 74 TTL gates | $t_{CAC}$ | | 70 | | 80 | ns |
| $t_{a(R)}$ | Access time from $\overline{RAS}$ | $t_{RLCL}$ = MAX, $C_L$ = 100 pF, Load = 2 Series 74 TTL gates | $t_{RAC}$ | | 120 | | 150 | ns |

**timing requirements over recommended supply voltage range and operating free-air temperature range**

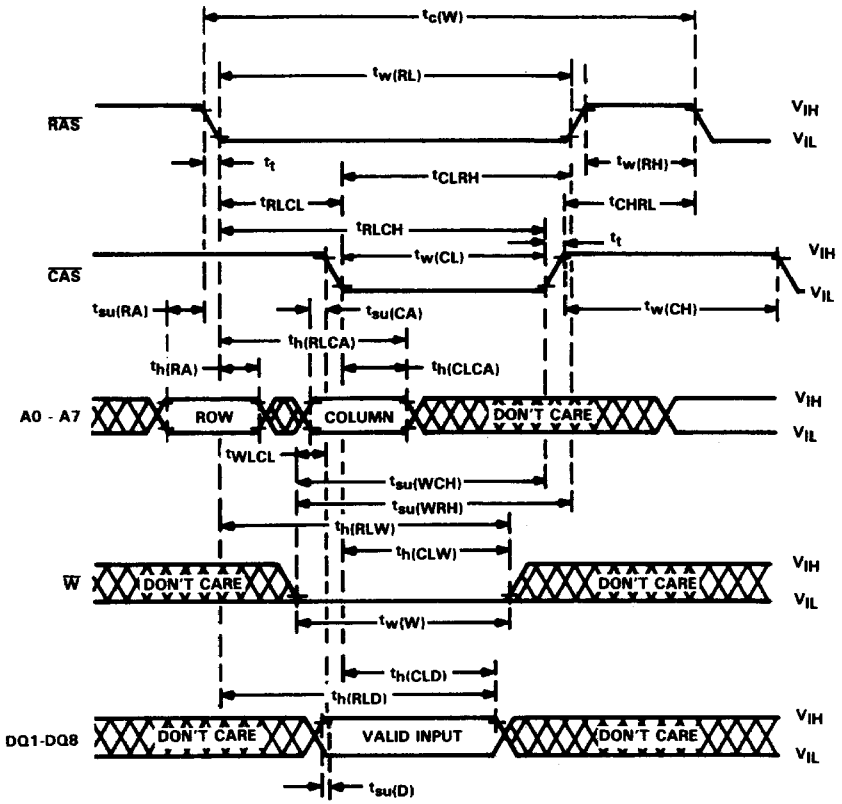
| | | ALT. SYMBOL | TM4416KU8-12 | | TM4416KU8-15 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{c(P)}$ | Page-mode cycle time | $t_{PC}$ | 120 | | 140 | | ns |
| $t_{c(rd)}$ | Read cycle time† | $t_{RC}$ | 230 | | 260 | | ns |
| $t_{c(W)}$ | Write cycle time | $t_{WC}$ | 230 | | 260 | | ns |
| $t_{c(rdW)}$ | Read-write/read-modify-write cycle time | $t_{RWC}$ | 315 | | 365 | | ns |
| $t_{w(CH)}$ | Pulse duration, $\overline{CAS}$ high (precharge time)‡ | $t_{CP}$ | 40 | | 50 | | ns |
| $t_{w(CL)}$ | Pulse duration, $\overline{CAS}$ low | $t_{CAS}$ | 70 | 10,000 | 80 | 10,000 | ns |
| $t_{w(RH)}$ | Pulse duration, $\overline{RAS}$ high (precharge time) | $t_{RP}$ | 80 | | 100 | | ns |
| $t_{w(RL)}$ | Pulse duration, $\overline{RAS}$ low | $t_{RAS}$ | 120 | 10,000 | 150 | 10,000 | ns |
| $t_{w(W)}$ | Write pulse duration | $t_{WP}$ | 30 | | 40 | | ns |
| $t_t$ | Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ | $t_T$ | 3 | 50 | 3 | 50 | ns |
| $t_{su(CA)}$ | Column-address setup time | $t_{ASC}$ | 0 | | 0 | | ns |
| $t_{su(RA)}$ | Row-address setup time | $t_{ASR}$ | 0 | | 0 | | ns |
| $t_{su(D)}$ | Data setup time | $t_{DS}$ | 5 | | 5 | | ns |
| $t_{su(rd)}$ | Read-command setup time | $t_{RCS}$ | 0 | | 0 | | ns |
| $t_{su(WCH)}$ | Write-command setup time before $\overline{CAS}$ high | $t_{CWL}$ | 50 | | 60 | | ns |
| $t_{su(WRH)}$ | Write-command setup time before $\overline{RAS}$ high | $t_{RWL}$ | 50 | | 60 | | ns |
| $t_{h(CLCA)}$ | Column-address hold time after $\overline{CAS}$ low | $t_{CAH}$ | 35 | | 40 | | ns |
| $t_{h(RA)}$ | Row-address hold time | $t_{RAH}$ | 20 | | 30 | | ns |
| $t_{h(RLCA)}$ | Column-address hold time after $\overline{RAS}$ low | $t_{AR}$ | 85 | | 110 | | ns |
| $t_{h(CLD)}$ | Data hold time after $\overline{CAS}$ low | $t_{DH}$ | 40 | | 60 | | ns |
| $t_{h(RLD)}$ | Data hold time after $\overline{RAS}$ low | $t_{DHR}$ | 90 | | 130 | | ns |
| $t_{h(RHrd)}$ | Read-command hold time after $\overline{RAS}$ high | $t_{RRH}$ | 10 | | 10 | | ns |
| $t_{h(CHrd)}$ | Read-command hold time after $\overline{CAS}$ high | $t_{RCH}$ | 0 | | 0 | | ns |
| $t_{h(CLW)}$ | Write-command hold time after $\overline{CAS}$ low | $t_{WCH}$ | 40 | | 60 | | ns |
| $t_{h(RLW)}$ | Write-command hold time after $\overline{RAS}$ low | $t_{WCR}$ | 90 | | 130 | | ns |
| $t_{RLCH}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high | $t_{CSH}$ | 120 | | 150 | | ns |
| $t_{CHRL}$ | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | $t_{CRP}$ | 0 | | 0 | | ns |
| $t_{CLRH}$ | Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high | $t_{RSH}$ | 70 | | 80 | | ns |
| $t_{RLCL}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time) | $t_{RCD}$ | 25 | 50 | 25 | 70 | ns |
| $t_{WLCL}$ | Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle) | $t_{WCS}$ | −5 | | −5 | | ns |
| $t_{rf}$ | Refresh time interval | $t_{REF}$ | | 4 | | 4 | ms |

†All cycle times assume $t_t$ = 5 ns.
‡Page mode only.

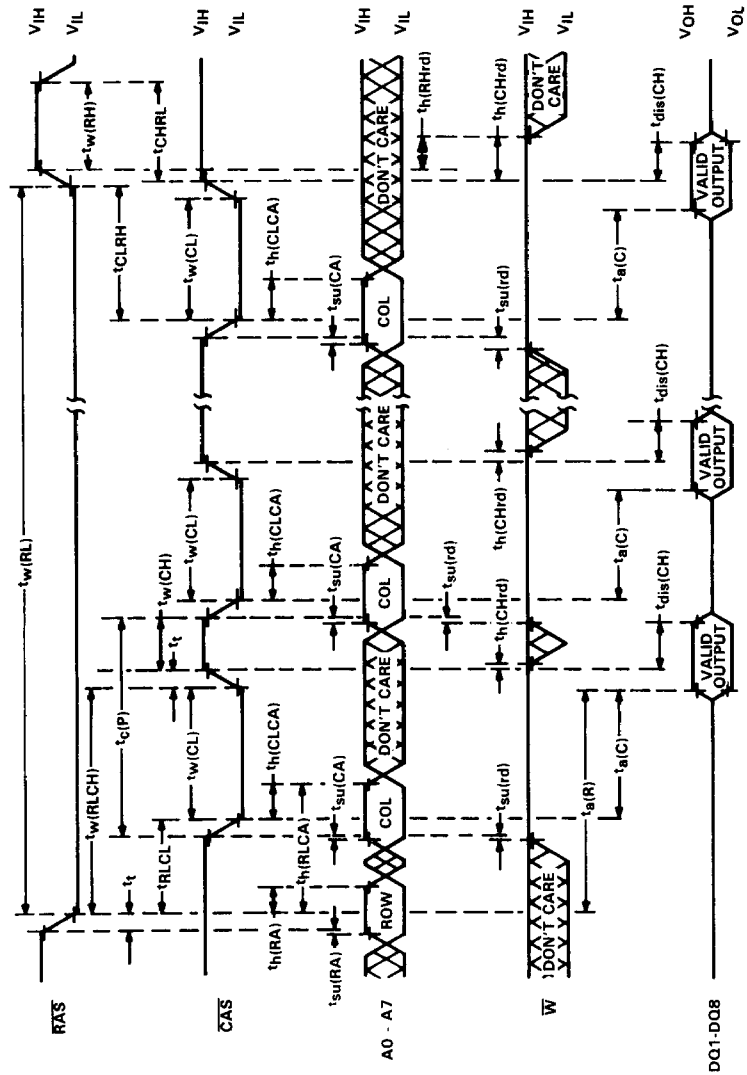
read cycle timing



**early write cycle timing**

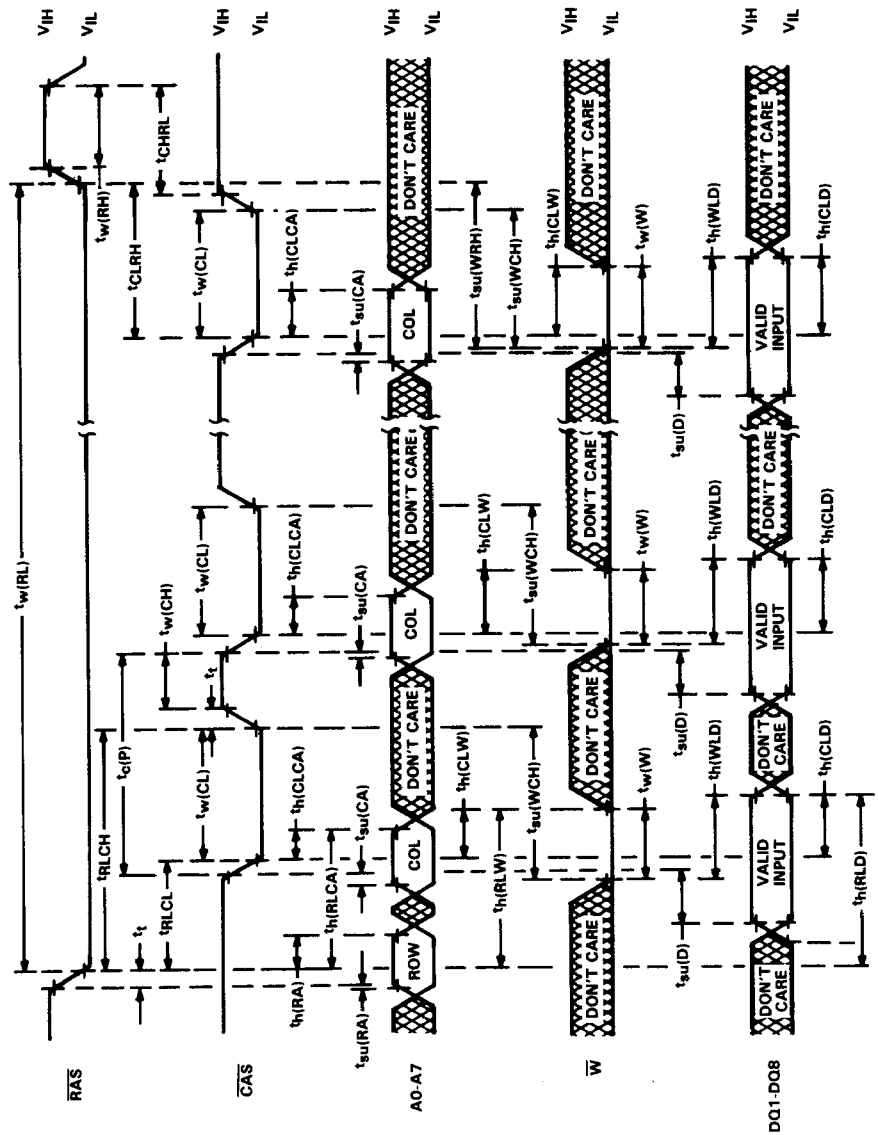


## page-mode read cycle timing



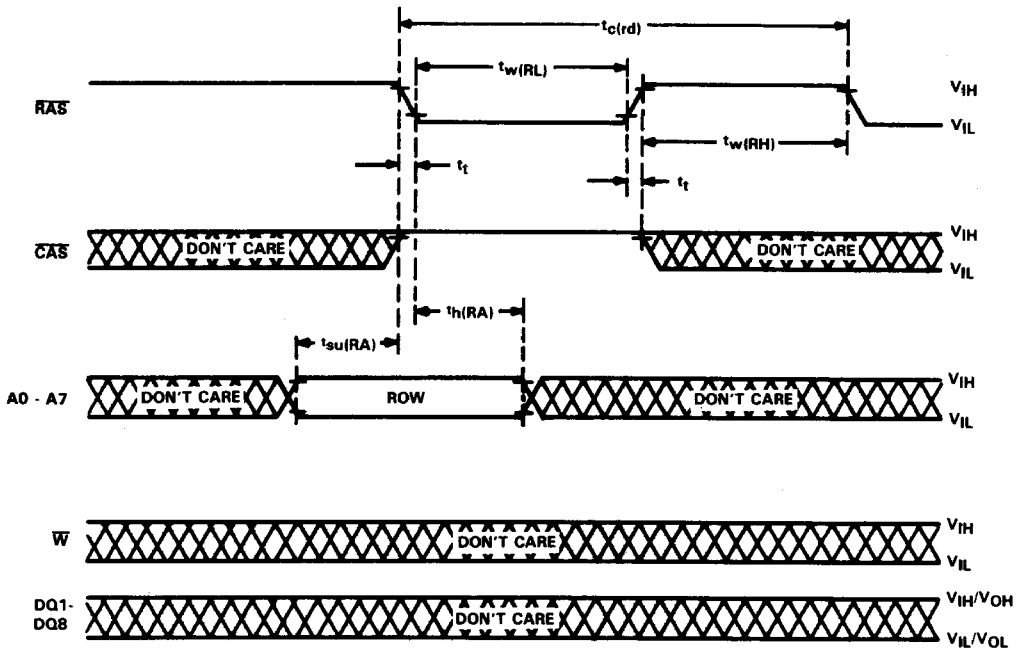

NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

**page-mode write cycle timing**

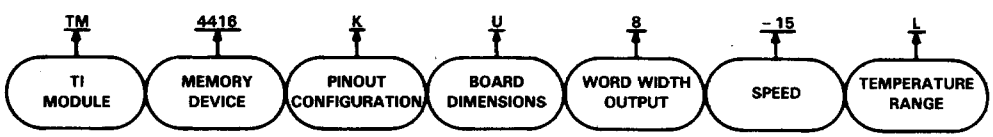



NOTE 6: A read or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

## RAS-only refresh timing




## TI single-in-line package nomenclature




(88,9 x 16,5 mm)
(3.5 x 0.65 inches)

Max Access
-12 120 ns
-15 150 ns

L 0°C to 70°C





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