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POWER MOSFET, N-CHANNEL, RADIATION HARDENED, HIGH RELIABILITY, SPACE USE, DETAIL SPECIFICATION FOR

JAXA R
2SK4048, 2SK4049, 2SK4050
2SK4051, 2SK4052, 2SK4053
2SK4054, 2SK4055, 2SK4056
2SK4214, 2SK4215, 2SK4216

Prepared and Established by Fuji Electric Device Technology Co., Ltd.
Issued by Japan Aerospace Exploration Agency

This specification was originally written and established in the Japanese language. This specification has been translated into English for international users. Note that this document is a working document for international users. Any discrepancies found in this document should be verified against the latest Japanese document before any significant decisions are made.

Revision Log

Rev.	Date	Description
----	20 December 2006	Original
A	29 Feb. 2008	Added the family type part number ▪ Added Part No.: 2SK4214, 2SK4215 and 2SK4216 (V_{DS} 130V Class) Revised to reflect the changes made to JAXA-QTS-2030C. ▪ Revised screening test in compliance with JAXA-QTS-2030C. ▪ Revised qualification test and quality conformance inspection in compliance with JAXA-QTS-2030C.

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1 GENERAL

This specification establishes the detailed requirements for space use, high reliability, N channel power MOSFET (100, 130, 200 and 250V for TO-254 types) used for electronic equipment installed on spacecrafts. The products specified in this specification are as follows.

1.1 Part Number

The part numbers for the products covered by this specification are as follows:

JAXA(1) R(2) 2SK4048
JAXA(1) R(2) 2SK4049
JAXA(1) R(2) 2SK4050
JAXA(1) R(2) 2SK4051
JAXA(1) R(2) 2SK4052
JAXA(1) R(2) 2SK4053
JAXA(1) R(2) 2SK4054
JAXA(1) R(2) 2SK4055
JAXA(1) R(2) 2SK4056
JAXA(1) R(2) 2SK4214
JAXA(1) R(2) 2SK4215
JAXA(1) R(2) 2SK4216

Notes (1) "JAXA" indicates that the parts are for space applications.
(2) "R" indicates that the parts are radiation hardened for space applications.

1.2 Absolute Maximum Ratings

The absolute maximum ratings of the products specified in this specification are as follows. Unless otherwise specified, T_A is +25°C.

Part No.	V_{DS} (V)	I_D (A)	$I_{D(pulse)}$ (A)	V_{GS} (V)	P_D T_C=25°C (W)		P_D T_A=25°C (W)		T_{ch}(1) (°C)	T_{stg} (°C)	$R_{th(ch-c)}$ (°C/W)	$R_{th(ch-a)}$ (°C/W)	SOA
JAXA R 2SK4048	100	42	168	±20	250	Fig.5	2.6	Fig.6	150	-55 to 150	0.5	48.0	Fig.7
JAXA R 2SK4049	100	42	168		125	Fig.8	2.58	Fig.9			1.0	48.5	Fig.10
JAXA R 2SK4050	100	15	60		62.5	Fig.11	2.55	Fig.12			2.0	49.0	Fig.13
JAXA R 2SK4051	200	42	168		250	Fig.14	2.6	Fig.15			0.5	48.0	Fig.16
JAXA R 2SK4052	200	33	132		125	Fig.17	2.58	Fig.18			1.0	48.5	Fig.19
JAXA R 2SK4053	200	14	56		62.5	Fig.20	2.55	Fig.21			2.0	49.0	Fig.22
JAXA R 2SK4054	250	42	168		250	Fig.23	2.6	Fig.24			0.5	48.0	Fig.25
JAXA R 2SK4055	250	27	108		125	Fig.26	2.58	Fig.27			1.0	48.5	Fig.28
JAXA R 2SK4056	250	12	48		62.5	Fig.29	2.55	Fig.30			2.0	49.0	Fig.31
JAXA R 2SK4214	130	42	168		250	Fig.32	2.6	Fig.33			0.5	48.0	Fig.34
JAXA R 2SK4215	130	35	140		125	Fig.35	2.58	Fig.36			1.0	48.5	Fig.37
JAXA R 2SK4216	130	15	60		62.5	Fig.38	2.55	Fig.39			2.0	49.0	Fig.40

Note(1) The channel temperature T_{ch} is given by the following equations:

$$T_{ch}=T_C + R_{th(ch-c)} \times P_D$$

$$T_{ch}=T_A + R_{th(ch-a)} \times P_D$$

Where T_C: Case temperature (°C)

T_A: Ambient temperature (°C)

$R_{th(ch-c)}$: Thermal resistance between junction and case (°C/W)

$R_{th(ch-a)}$: Thermal resistance between channel and ambient (°C/W)

P_D: Power dissipation (W)

1.3 Primary Electrical Characteristics

The primary electrical characteristics of the products specified in this specification are as follows. Unless otherwise specified, T_A is +25°C.

Electrical Characteristics (1/3)

Part No.	$V_{(BR)DSS}$ (V)	I_{DSS} (μA)	I_{GSS} (nA)	$V_{GS(th)}$ (V)	$R_{DS(on)}$([1]) (mΩ)	gfs([1]) (S)	E_{AS} (mJ)
	I_D=1mA V_{GS}=0V	V_{DS}=80% of rated V_{DS} V_{GS}=0V	V_{GS}=±20V V_{DS}=0V	I_D=1mA V_{DS}=V_{GS}	I_D=50% of rated I_D V_{GS}=12V	I_D=50% of rated I_D V_{DS}=25V	Rated I_D V_{DD}=48V, V_{GS}=12V
	Min	Max	Max	Min-Max	Max	Min	Max
JAXA R 2SK4048	100	10	±100	2.5-4.5	18	8	1091
JAXA R 2SK4049	100				33	8	272
JAXA R 2SK4050	100				69	4	191
JAXA R 2SK4051	200				33	8	545
JAXA R 2SK4052	200				69	8	173
JAXA R 2SK4053	200				155	4	102
JAXA R 2SK4054	250				45	8	436
JAXA R 2SK4055	250				98	8	169
JAXA R 2SK4056	250				230	4	95
JAXA R 2SK4214	130				24	8	839
JAXA R 2SK4215	130				46	8	252
JAXA R 2SK4216	130				96	4	147

Note([1]) Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

Electrical Characteristics (2/3)

Part No.	Q_{GS} (nC)	Q_{GD} (nC)	Q_G (nC)	$t_{d(on)}$ (ns)	t_r (ns)	$t_{d(off)}$ (ns)	t_f (ns)
	V_{DS}=50% of rated V_{DS}, I_D= rated I_D, V_{GS}=12V			V_{DD}=50% of rated V_{DS}, I_D= rated I_D, V_{GS}=12V, R_G=10Ω			
	Max	Max	Max	Max	Max	Max	Max
JAXA R 2SK4048	60	70	220	65	30	190	65
JAXA R 2SK4049	30	30	100	40	20	100	30
JAXA R 2SK4050	13	10	50	30	20	65	15
JAXA R 2SK4051	60	70	220	65	30	190	35
JAXA R 2SK4052	30	30	100	40	20	100	20
JAXA R 2SK4053	13	10	50	30	20	65	15
JAXA R 2SK4054	60	70	220	65	30	190	30
JAXA R 2SK4055	30	30	100	40	20	100	15
JAXA R 2SK4056	13	10	50	30	20	65	10
JAXA R 2SK4214	60	70	220	65	30	190	65
JAXA R 2SK4215	30	30	100	40	20	100	30
JAXA R 2SK4216	13	10	50	30	20	65	15

Electrical Characteristics (3/3)

(Body Diode Characteristics)

Part No.	V_{SD}(1) (V)	t_{rr} (ns)	Q_{rr} (□C)
	I_F= rated I_D V_{GS}=0V	I_F= rated I_D, V_{GS}=0V, -di/dt=100A/□s, T_{ch}=25°C	
	Max	Typ	Typ
JAXA R 2SK4048	1.6	450	7.0
JAXA R 2SK4049		500	6.5
JAXA R 2SK4050		350	3.5
JAXA R 2SK4051		690	13.5
JAXA R 2SK4052		800	12.0
JAXA R 2SK4053		620	6.0
JAXA R 2SK4054		1000	19.0
JAXA R 2SK4055		900	12.0
JAXA R 2SK4056		640	6.5
JAXA R 2SK4214		520	11.0
JAXA R 2SK4215		540	9.0
JAXA R 2SK4216		390	5.0

Note(1) Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

1.4 Radiation Hardness

The radiation hardness of the products specified in this specification is as follows.

Symbol	Radiation hardness assurance level
R	1000 Gy(Si) {1×10^5 rad(Si)} (Dose Rate 36Gy(Si)/ h to 360Gy(Si)/ h)

2 APPLICABLE DOCUMENTS

The latest issues of documents listed below at the time of contract award or application form a part of this specification the extent specified herein.

JAXA-QTS-2030	Semiconductor Devices, High Reliability, Space Use, General Specification for
MIL-STD-750	Test Methods Standard for Semiconductor Devices

3 REQUIREMENTS

3.1 Design and Construction

The design and construction of the products shall meet the requirements specified in this paragraph and paragraph 3.3 of JAXA-QTS-2030.

3.1.1 Package Configuration and Lead Connection

The package configuration and lead connection shall meet the requirements specified in Figure 1.

3.1.2 Lead Materials and Finish

The leads shall be made of Fe-Ni (Ni-Au plating) covered OCF (Oxygen-Free Copper) and plated with Au as specified in the paragraph 3.3.7 c) 2) 2.3) or with Pb-Sn solder immersion as specified in paragraph 3.3.7 c) 2) 2.1) of JAXA-QTS-2030. In the case of Pb-Sn solder immersion, unplated lead length shall be less than 2mm from the lead egress on the product's body.

3.1.3 Electrical Characteristics

The electrical characteristics shall meet the requirements specified in Tables 1a and 1b.

3.2 Marking

Marking shall be in accordance with the paragraph 3.4 of JAXA-QTS-2030, and Figure 2.

3.3 Certification

Manufacturers who wish to supply the products specified herein shall be certified by JAXA as specified in paragraph 3.1 of JAXA-QTS-2030.

4 QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

The general requirements shall be in accordance with the paragraph 4.1 of JAXA-QTS-2030.

4.2 Materials Control

The materials control shall be in accordance with the paragraph 4.2 of JAXA-QTS-2030.

4.3 Manufacturing Process Control

The manufacturing process control shall be in accordance with the paragraph 4.3 of JAXA-QTS-2030.

4.4 In-process Inspection

The in-process inspection shall be in accordance with the paragraph 4.5 of JAXA-QTS-2030.

4.5 Screening

The screening shall be in accordance with paragraph 4.7 of JAXA-QTS-2030. The electrical characteristics to be measured, test conditions and delta limits shall be as follows.

4.5.1 Electrical Characteristics to be Measured

The following parameters shall be measured during the interim and final electrical characteristics tests for screening.

(1) Interim electrical characteristic tests T_A=+25°C

Measuring item	$V_{(BR)DSS}$ (V)	I_{DSS} (μA)	I_{GSS} (nA)	$V_{GS(th)}$ (V)	$R_{DS(on)}$([1]) (mΩ)	gfs([1]) (S)	V_{SD}([1]) (V)
MIL-STD-750 Test Method No.	3407	3413	3411	3404	3421	3475	---
Test conditions	Bias Condition C I_D=1mA V_{GS}=0V	Bias Condition C V_{DS}=80% of rated V_{DS} V_{GS}=0V	Bias Condition C V_{GS}=±20V V_{DS}=0V	I_D=1mA V_{DS}=V_{GS}	I_D=50% of rated I_D V_{GS}=12V	I_D=50% of rated I_D V_{DS}=25V	I_F= rated I_D V_{GS}=0V
	Min	Max	Max	Min-Max	Max	Min	Max
JAXA R 2SK4048	100	10	±100	2.5-4.5	18	8	1.6
JAXA R 2SK4049	100				33	8	
JAXA R 2SK4050	100				69	4	
JAXA R 2SK4051	200				33	8	
JAXA R 2SK4052	200				69	8	
JAXA R 2SK4053	200				155	4	
JAXA R 2SK4054	250				45	8	
JAXA R 2SK4055	250				98	8	
JAXA R 2SK4056	250				230	4	
JAXA R 2SK4214	130				24	8	
JAXA R 2SK4215	130				46	8	
JAXA R 2SK4216	130				96	4	

Note([1]) Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

(2) Final electrical characteristics test: As specified in the subgroups 1, 2 and 3 of Tables 1a and 1b.

4.5.2 Test Conditions

The conditions of gate stress test, avalanche energy test, temperature cycling test, reverse bias burn-in test and burn-in test for screening test shall be as follows.
(Gate stress test is performed as part of In-process inspection.)

Gate stress test: V_{GS}=35V, t=1ms, T_A=25°C

Single pulse avalanche energy (E_{AS}) test: $I_{D(pulse)}$ = rated I_D, V_{DD}=48V, V_{GS}=12V

Initial $T_C = +25^{-5}_{+10}$ °C

$$L(mH) = \left[\frac{2E_{AS}}{(I_D)^2}\right]\left[\frac{BV_{DSS} - V_{DD}}{BV_{DSS}}\right] \quad \text{▪ ▪ Equation (1)}$$

Temperature cycling test: Condition G, 20 cycles

Reverse bias burn-in test (GS): T_A=150°C, V_{GS}=16V
V_{DS}=0V, 48hr

Burn-in test (DS): T_A=150°C, V_{DS}=80% of rated V_{DS}
V_{GS}=0V, 240hr

4.5.3 Delta Limits

The delta limits for reverse bias burn-in test and burn-in test shall be as follows.

$\Delta I_{GSS} \leq |20nA|$
$\Delta I_{DSS} \leq |10\mu A|$
$\Delta R_{DS(on)} \leq |20\%|$
$\Delta V_{GS(th)} \leq |20\%|$

4.6 Qualification Test and Quality Conformance Inspection

The qualification test and the quality conformance inspection shall be in accordance with paragraphs 4.6 and 4.8 of JAXA-QTS-2030. External dimensions, electrical characteristics, test conditions and limits shall be as specified in Figure 1, and Tables 1, 2, 3, and 4. Group C tests and Group D tests may be exempted when the qualification test or quality conformance inspection for the Groups C and D tests was performed and the device passed the test within a year. Detailed requirements are specified in Table 6. Group E tests may be exempted in spite of chip size, when the semiconductor devices manufactured from the die of the same wafer lot have passed the Group E tests in the qualification test or the quality conformance inspection.

4.6.1 Electrostatic Discharge Sensitivity Test

Electrostatic discharge sensitivity test in the qualification test shall be performed with the following lead combination:

Gate and Source

4.6.2 Radiation Hardness Test

Radiation test (TID: Total Dose Irradiation) level, electrical characteristics, test conditions and limits in the qualification tests and the quality conformance inspections shall be as specified in Table 5. The bias shall be maintained during the irradiation and post-irradiation electrical characteristics test. The post-irradiation electrical characteristics test shall be performed within 24 hours after the completion of irradiation.

4.7 Change of Tests and Inspections

No change has been made to any test or inspection specified in appendixes A, B or C of JAXA-QTS -2030.

4.8 Long-term Storage

Delivery of the products stored at the manufacturer's site for 24 months or longer shall be in accordance with paragraph 4.9.1 of JAXA-QTS-2030.

5 PREPARATION FOR DELIVERY

Preparation for delivery shall be in accordance with Section 5 of JAXA-QTS-2030.

6 NOTES

6.1 Terms and Definitions

The terms and definitions used herein shall be in accordance with paragraph 1.2 of JAXA-QTS-2030 and as follows.

(1) SEB (Single Event Burnout);

Burnout of the device caused by the incidence of a proton or a heavy ion, when the device is applied to an off-state voltage between drain and source.

(2) SEGR (Single Event Gate Rupture);

Breakdown of MOSFET Gate Oxide film caused by the incidence of a proton or a heavy ion, when the device is applied to a gate bias voltage between gate and source.

6.2 Notice for Acquisition Officers

The precautions to be taken by the purchaser shall be in accordance with paragraph 6.2 of JAXA-QTS-2030 and as follows.

6.2.1 Handling Instructions

The products specified in this specification contain thin oxide films and can be damaged due to electrostatic discharge (ESD). ESD protection measures shall be implemented to avoid ESD between the gate and source and between the gate and drain during transportation and other handling environments.

6.2.2 Beryllium Warning

The products of TO-254 package contain beryllium. Disintegration or chemical processing of the products that may produce dusts or fumes shall be prohibited. Disposition of the products shall be performed in accordance with applicable regulations.

Table 1-a. Group A Inspection ([1])

Gr.No	MIL-STD-750			100V Class			130V Class			200V Class			250V Class		
Sub	Test Item	Method	JAXA R	2SK 4048	2SK 4049	2SK 4050	2SK 4214	2SK 4215	2SK 4216	2SK 4051	2SK 4052	2SK 4053	2SK 4054	2SK 4055	2SK 4056
A -1	**Static Characteristics (T_A=25°C)**		Sample Size	LTPD 3											
-1a	Breakdown Voltage Drain to Source V_{DSS}	3407	Conditions	Bias Condition C I_D=1mA , V_{GS}=0V											
			Limits	min 100V DC			min 130V DC			min 200V DC			min 250V DC		
-1b	Gate Current I_{GSS}	3411	Conditions	Bias Condition C V_{GS}=±20V , V_{DS}=0V											
			Limits	max ±100nA DC											
-1c	Drain Current I_{DSS}	3413	Conditions	Bias Condition C V_{DS}=80V , V_{GS}=0V			Bias Condition C V_{DS}=104V , V_{GS}=0V			Bias Condition C V_{DS}=160V , V_{GS}=0V			Bias Condition C V_{DS}=200V , V_{GS}=0V		
			Limits	max 10µA DC											
-1d	Gate to Source Voltage (Threshold) $V_{GS(th)}$	3404	Conditions	Bias Condition C V_{GS}=V_{DS} , I_D=1mA											
			Limits	2.5 - 4.5V DC											
-1e	Static Drain to Source On-State Resistance $R_{DS(on)}$	3421	Conditions	Pulse Test([2]) , V_{GS}=12V											
				I_D 21A	I_D 21A	I_D 7.5A	I_D 21A	I_D 17.5A	I_D 7.5A	I_D 21A	I_D 16.5A	I_D 7A	I_D 21A	I_D 13.5A	I_D 6A
			Limits	max [mΩ] 18	max [mΩ] 33	max [mΩ] 69	max [mΩ] 24	max [mΩ] 46	max [mΩ] 96	max [mΩ] 33	max [mΩ] 69	max [mΩ] 155	max [mΩ] 45	max [mΩ] 98	max [mΩ] 230
-1f	Forward Transconductance gfs	3475	Conditions	Pulse Test([2]) , V_{GS}=25V											
				I_D 21A	I_D 21A	I_D 7.5A	I_D 21A	I_D 17.5A	I_D 7.5A	I_D 21A	I_D 16.5A	I_D 7A	I_D 21A	I_D 13.5A	I_D 6A
			Limits	min 8S	min 8S	min 4S	min 8S	min 8S	min 4S	min 8S	min 8S	min 4S	min 8S	min 8S	min 4S
-1g	Forward Voltage V_{SD}	---	Conditions	Pulse Test([2]) , V_{GS}=0V											
				I_D 42A	I_D 42A	I_D 15A	I_D 42A	I_D 35A	I_D 15A	I_D 42A	I_D 33A	I_D 14A	I_D 42A	I_D 27A	I_D 12A
			Limits	max 1.6V											
A -2	**Static Characteristics (T_A=125°C)**		Sample Size	LTPD 5											
-2a	Gate Current I_{GSS} (125°C)	3411	Conditions	Bias Condition C V_{GS}=±20V , V_{DS}=0V											
			Limits	max ±100nA DC											
-2b	Drain Current II_{DSS} (125°C)	3413	Conditions	Bias Condition C V_{DS}=80V , V_{GS}=0V			Bias Condition C V_{DS}=104V , V_{GS}=0V			Bias Condition C V_{DS}=160V , V_{GS}=0V			Bias Condition C V_{DS}=200V , V_{GS}=0V		
			Limits	max 25µA DC											
-2c	Gate to Source Voltage (Threshold) $V_{GS(th)}$ (125°C)	3404	Conditions	Bias Condition C V_{GS}=V_{DS} , I_D=1mA											
			Limits	min 1.5V DC											
-2d	Static Drain to Source On-State Resistance $R_{DS(on)}$ (125°C)	3421	Conditions	Pulse Test([2]) , V_{GS}=12V											
				I_D 21A	I_D 21A	I_D 7.5A	I_D 21A	I_D 17.5A	I_D 7.5A	I_D 21A	I_D 16.5A	I_D 7A	I_D 21A	I_D 13.5A	I_D 6A
			Limits	max [mΩ] 31	max [mΩ] 56	max [mΩ] 117	max [mΩ] 44	max [mΩ] 84	max [mΩ] 175	max [mΩ] 66	max [mΩ] 138	max [mΩ] 310	max [mΩ] 90	max [mΩ] 196	max [mΩ] 460

Notes([1]) The same sample may be used for all subgroups.

([2]) Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

Table 1-b. Group A Inspection ([1])

Gr.No	MIL-STD-750			100V Class			130V Class			200V Class			250V Class		
Sub	Test Item	Method	JAXA R	2SK 4048	2SK 4049	2SK 4050	2SK 4214	2SK 4215	2SK 4216	2SK 4051	2SK 4052	2SK 4053	2SK 4054	2SK 4055	2SK 4056
A -3	**Static Characteristics (T_A=-55°C)**		Sample Size	LTPD 5											
-3a	Gate to Source Voltage (Threshold) $V_{GS(th)}$ (-55°C)	3404	Conditions	Bias Condition C $V_{GS}=V_{DS}$, I_D=1mA											
			Limits	max 5.0V DC											
-3b	Forward Transconductance gfs (-55°C)	3475	Conditions	Pulse Test ([2]) , V_{GS}=25V											
				I_D			I_D			I_D			I_D		
				21A	21A	7.5A	21A	17.5A	7.5A	21A	16.5A	7A	21A	13.5A	6A
			Limits	min			min			min			min		
				8.5S	8.5S	4.5S	8.5S	8.5S	4.5S	8.5S	8.5S	4.5S	8.5S	8.5S	4.5S
A -4	**Dynamic Characteristics (T_A=25°C)**		Sample Size	LTPD 3											
	Switching Time Test (1) Turn-on delay time: $t_{d(on)}$ Rise time: t_r (2) Turn-off delay time: $t_{d(off)}$ Fall time: t_f	3472	Conditions	V_{DD}=50V V_{GS}=12V, R_g=10Ω			V_{DD}=65V V_{GS}=12V, R_g=10Ω			V_{DD}=100V V_{GS}=12V, R_g=10Ω			V_{DD}=125V V_{GS}=12V, R_g=10Ω		
				I_D			I_D			I_D			I_D		
				42A	42A	15A	42A	35A	15A	42A	33A	14A	42A	27A	12A
			Limits	max			max			max			max		
			$t_{d(on)}$	65ns	40ns	30ns	65ns	40ns	30ns	65ns	40ns	30ns	65ns	40ns	30ns
			t_r	30ns	20ns	20ns	30ns	20ns	20ns	30ns	20ns	20ns	30ns	20ns	20ns
			$t_{d(off)}$	190ns	100ns	65ns	190ns	100ns	65ns	190ns	100ns	65ns	190ns	100ns	65ns
			t_f	65ns	30ns	15ns	65ns	30ns	15ns	35ns	20ns	15ns	30ns	15ns	10ns
A -6a	**Safe Operating Area Test([3])**		Sample Size	LTPD 5											
		3474	Conditions	---											
-6b	**End-Point Electrical Measurements**	---		Same as Gr.A-1											
A -7	**Other Characteristics (T_A=25°C)** ([4])		Sample Size	LTPD 10											
-7a	Gate Charge (1) Gate Charge: Q_g (2) Gate to Drain Charge: Q_{gd} (3) Gate to Source Charge: Q_{gs}	3471	Conditions	V_{GS}=12V V_{DS}=50V			V_{GS}=12V V_{DS}=65V			V_{GS}=12V V_{DS}=100V			V_{GS}=12V V_{DS}=125V		
				I_D			I_D			I_D			I_D		
				42A	42A	15A	42A	35A	15A	42A	33A	14A	42A	27A	12A
			Limits	max			max			max			max		
			Q_g	220nC	100nC	50nC	220nC	100nC	50nC	220nC	100nC	50nC	220nC	100nC	50nC
			Q_{gd}	70nC	30nC	10nC	70nC	30nC	10nC	70nC	30nC	10nC	70nC	30nC	10nC
			Q_{gs}	60nC	30nC	13nC	60nC	30nC	13nC	60nC	30nC	13nC	60nC	30nC	13nC
-7b	Reverse Recovery Characteristics (1) T_{rr} (2) Q_{rr}	3473	Conditions	I_F= I_D			I_F= I_D			I_F= I_D			I_F= I_D		
				42A	42A	15A	42A	35A	15A	42A	33A	14A	42A	27A	12A
				V_{GS}=0V -di/dt=100A/μs											
			Limits	max			max			max			max		
			T_{rr}	765ns	750ns	525ns	765ns	750ns	525ns	1050ns	1200ns	950ns	1500ns	1350ns	950ns
			Q_{rr}	10.5μC	10.0μC	5.5μC	13.0μC	12.0μC	6.5μC	20.0μC	18.0μC	9.0μC	29.0μC	18.0μC	10.0μC

Notes([1]) The same sample may be used for all subgroups.

([2]) Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

([3]) The samples used for subgroups A-1, A-2, and A-3 tests shall be used.

([4]) The samples used for subgroups A-6 tests shall be used.

Table 2-a. Group B Inspection

Gr.No	Sub	Test Item	MIL-STD-750 Method	JAXA R	100V Class 2SK 4048	100V Class 2SK 4049	100V Class 2SK 4050	130V Class 2SK 4214	130V Class 2SK 4215	130V Class 2SK 4216	200V Class 2SK 4051	200V Class 2SK 4052	200V Class 2SK 4053	250V Class 2SK 4054	250V Class 2SK 4055	250V Class 2SK 4056
B	-1	**Dimensions**([1])		Sample Size	Level I ([2]) 3p Level II ([2]) 3p											
			2066	Conditions	See Fig. 1											
B	-2	**Resistance to Solvents**([3]) ([4])		Sample Size	Level I 3p Level II 3p											
			1022	Conditions	Solvent a, b, c											
B	-3b	**Temperature Cycling (Air to Air)**		Sample Size	Level I 6p Level II 6p											
			1051	Conditions	-55^{+0}_{-5}°C↔25^{+10}_{-5}°C↔150^{+5}_{-0}°C 100 cycles											
	-3c	**Surge Test** (1) Gate Shock	4066	Conditions	V_{GS}=35V											
		(2) Avalanche	4066	Conditions	V_{DS}=48V, L= See paragraph 4.5.2, Equation (1), R_g=10Ω $I_{D(pulse)}$											
					42A	42A	15A	42A	35A	15A	42A	33A	14A	42A	27A	12A
	-3d	**Hermetic Seal** (1) Fine	1071	Conditions	Condition H											
				Limits	max 1×10^{-3}Pa-cm^3/s											
		(2) Gross	1071	Conditions	--- Condition C											
	-3e	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											
	-3f	**Decap-Internal Visual**	2075 2071	Conditions	---											
	-3g	**Bond Strength**	2037	Conditions	Condition A											
				Limits	Gate Wire >90gf											
					Source Wire											
					>300gf	>300gf	>90gf	>300gf	>300gf	>90gf	>300gf	>300gf	>90gf	>300gf	>300gf	>90gf
	-3h	**SEM**([1])	2077	Conditions	---											
	-3i	**Die Shear**		Sample Size	Level I 3p Level II 3p											
			2017	Conditions	---											
				Limits	min 2.5kgf											
B	-4	**Solderability**([3]) ([4])		Sample Size	Level I 6 leads([5]) Level II 6 leads([5])											
			2026	Conditions	---											

Notes([1]) The test may be performed using the samples prior to inspection lot formation.

([2]) Level I and Level II shall be applicable to the qualification test or the quality conformance inspection, respectively. (See paragraphs C.3.2 and C.3.3 of JAXA-QTS-2030)

([3]) Electrically defective products from the same inspection lot may be used.

([4]) When electrically defective products are used, the samples shall be exposed to the same thermal environments as the certified samples experience in all thermal tests required as part of the screening test.

([5]) This test shall be performed for each 3 lead from 2 devices.

Table 2-b. Group B Inspection

Gr.No	MIL-STD-750			100V Class			130V Class			200V Class			250V Class		
Sub	Test Item	Method	JAXA R	2SK 4048	2SK 4049	2SK 4050	2SK 4214	2SK 4215	2SK 4216	2SK 4051	2SK 4052	2SK 4053	2SK 4054	2SK 4055	2SK 4056
B -5a	**Intermittent Operation Life**		Sample Size	Level I LTPD 10 Level II 12p											
		1042	Conditions	Condition D, 2000 cycles([1])											
-5b	**End-Point Electrical Measurements**	---		Same as Gr.A-1											
B -6c	**Accelerated Steady-state Gate Stress (High Temp. GS)**		Sample Size	Level I LTPD 10 Level II 12p											
		1042	Conditions	V_{GS}=20V, T_A =150°C, 48hr or V_{GS}=20V, T_A =175°C, 24hr											
-6d	**End-Point Electrical Measurements**	---		Same as Gr.A-1											
-6e	**Accelerated Steady-state Reverse Bias (DS)**	1042	Conditions	V_{DS}=100V			V_{DS}=130V			V_{DS}=200V			V_{DS}=250V		
				T_A =150°C, 240hr or T_A =175°C, 120hr											
-6f	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											
-6g	**Bond Strength**		Sample Size	20 wires											
		2037	Conditions	Condition A											
			Limits	Gate Wire >90gf											
				Source Wire											
				>300gf	>300gf	>90gf	>300gf	>300gf	>90gf	>300gf	>300gf	>90gf	>300gf	>300gf	>90gf
B -7	**Thermal Resistance** $R_{th(ch-c)}(\Delta V_{SD})$		Sample Size	Level I LTPD 10 Level II 8p											
		3161	Conditions	T_A =25°C											
			Limits	max (°C/W)			max (°C/W)			max (°C/W)			max (°C/W)		
				0.5	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0

Note([1]) If the samples are also used for “Intermittent operating life test” of C1-1 in the Group C test, the test shall be performed up to 6000 cycles.

Table 3. Group C Inspection

Gr.No	Sub	Test Item	MIL-STD-750 Method	JAXA R	100V Class 2SK 4048	100V Class 2SK 4049	100V Class 2SK 4050	130V Class 2SK 4214	130V Class 2SK 4215	130V Class 2SK 4216	200V Class 2SK 4051	200V Class 2SK 4052	200V Class 2SK 4053	250V Class 2SK 4054	250V Class 2SK 4055	250V Class 2SK 4056
C	1-1a	**Intermittent Operation Life**		Sample Size	Level I LTPD 10 Level II LTPD 10											
			1042	Conditions	Condition D, 6000 cycles ([1])											
	1-1b	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											
C	1-2a	**Steady-state Bias Life test (high temperature GS applied)** ([2])		Sample Size	Level I LTPD 5 Level II NA											
			1042	Conditions	V_{GS}=16V T_A=150°C , 1000hr											
	1-2b	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											
	1-2c	**Steady-state Bias Life test (high temperature DS applied)** ([2])	1042	Conditions	V_{DS}=80V			V_{DS}=104V			V_{DS}=160V			V_{DS}=200V		
					T_A=150°C, 1000hr											
	1-2d	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											
C	-2a	**Thermal Shock Temperature Cycling**		Sample Size	Level I 12p Level II NA											
			1051	Conditions	-55^{+0}_{-5}°C↔25^{+10}_{-5}°C↔150^{+5}_{-0}°C 100 cycles											
	-2b	**Hermetic Seal** (1) Fine	1071	Conditions	Condition H											
				Limits	max 1×10^{-3}Pa-cm^3/s											
		(2) Gross	1071	Conditions	Condition C											
	-2c	**End-Point Electrical Measurements** ([3])	---	Conditions	Same as Gr.A-1											
C	-3	**Thermal Resistance** ([4]) $R_{th(ch-c)}(\Delta V_{SD})$		Sample Size	Level I LTPD 10 Level II 8p											
			3161	Conditions	T_A =25°C											
				Limits	max (°C/W)			max (°C/W)			max (°C/W)			max (°C/W)		
					0.5	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0
C	-4a	**Safe Operating Area Test**([5])		Sample Size	Level I LTPD 10 Level II LTPD 10											
			3474	Conditions	---											
	-4b	**End-Point Electrical Measurements** ([5])	---	Conditions	Same as Gr.A-1											
C	-6a	**Electric Discharge Sensitivity Classification**		Sample Size	Level I 3p Level II NA											
			1020	Conditions	V_{GS}											
					±2750V	±1000V	±500V	±2750V	±1000V	±500V	±2750V	±1000V	±500V	±2750V	±1000V	±500V
					V_{DS}=0V											
	-6b	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											

Notes([1]) For the quality conformance inspection, the cycles may be reduced to 2000 cycles as a minimum.

([2]) The legibility of the marking shall not apply.

([3]) This test may be conducted prior to the hermetic seal.

([4]) Thermal impedance curve shall be obtained during the qualification test.

([5]) This test may be exempted if performed in the Group A test.

Table 4-a. Group D Inspection

Gr.No	Sub	MIL-STD-750 Test Item	Method	JAXA R	100V Class 2SK 4048	100V Class 2SK 4049	100V Class 2SK 4050	130V Class 2SK 4214	130V Class 2SK 4215	130V Class 2SK 4216	200V Class 2SK 4051	200V Class 2SK 4052	200V Class 2SK 4053	250V Class 2SK 4054	250V Class 2SK 4055	250V Class 2SK 4056
D	-1a	**Thermal Shock (Glass Strain)**		Sample Size	Level I LTPD 15 Level II LTPD 15											
			1056	Conditions	Condition B, 15 cycles											
	-1b	**Thermal Shock (Temperature Cycling)**	1051	Conditions	-55^{+0}_{-5}°C↔25^{+10}_{-5}°C↔150^{+5}_{-0}°C 45 cycles											
	-1c	**Terminal Strength**	2036	Conditions	Condition A 1.5kg, 30s											
	-1d	**Moisture Resistance**	1021	Conditions	(MIL-STD-202, Method 106)											
	-1e	**Hermetic Seal** (1) Fine	1071	Conditions	Condition H											
				Limits	max 1×10^{-3}Pa-cm^3/s											
		(2) Gross	1071	Conditions	Condition C											
	-1f	**Visual Inspection**	1051 1021	Conditions	---											
	1g	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											
D	-2a	**Shock**(1)		Sample Size	Level I LTPD 15 Level II LTPD 15											
			2016	Conditions	No Operating, 14710m/s^2 (1500G) 5 blows in each orientation, X_1, Y_1, Y_2 and Z_1											
	-2b	**Vibration, Variable Frequency**(1)	2056	Conditions	100 to 2000 Hz, 4min 196.1 m/s^2 (20G)											
	-2c	**Constant Acceleration**(1)	2006	Conditions	98066.5m/s^2 (10000G) X_1, Y_1, Y_2 and Z_1 orientation											
	-2d	**Hermetic Seal**(1) (1) Fine	1071	Conditions	Condition H											
				Limits	max 1×10^{-3}Pa-cm^3/s											
		(2) Gross	1071	Conditions	Condition C											
	-2e	**End-Point Electrical Measurements**(1)	---	Conditions	Same as Gr.A-1											
D	-3a	**Salt Atmosphere**(2)		Sample Size	Level I LTPD 15 Level II LTPD 15											
			1041	Conditions	35°C, 24hr Rate of salt deposit=10 to 50g/m^2/24hr											

Notes(1) Samples used for subgroup 1 may be used.

(2) Electrically defective products from the same inspection lot may be used.

Table 4-b. Group D Inspection

Gr.No	MIL-STD-750			100V Class			130V Class			200V Class			250V Class		
Sub	Test Item	Method	JAXA R	2SK 4048	2SK 4049	2SK 4050	2SK 4214	2SK 4215	2SK 4216	2SK 4051	2SK 4052	2SK 4053	2SK 4054	2SK 4055	2SK 4056
D -4	**Barometric Pressure (reduced)**		Sample Size	Level I 3p Level II NA											
		1001	Conditions	Not applicable for devices with rated voltage ≤ 200V.									8mmHg 60sec (minimum) V_{DS}=250V, V_{GS}=0V		
D -5	**Internal Water Vapor** (1)		Sample Size	Level I 3p Level II 3p											
		1018	Conditions	---											
D -6a	**Resistance to Soldering Heat**		Sample Size	Level I 3p Level II NA											
		2031	Conditions	250°C, 10s											
-6b	**Visual Inspection**	---	Conditions	---											
-6c	**Hermetic Seal** (1) Fine	1071	Conditions	Condition H											
			Limits	max 1×10^{-3}Pa-cm^3/s											
	(2) Gross	1071	Conditions	Condition C											
-6d	**End-Point Electrical Measurements**	---	Conditions	Same as Gr.A-1											

Note(1) Electrically defective products from the same inspection lot may be used.

Table 5. Group E Inspection

Gr.No	Sub	Test Item	MIL-STD-750 Method	JAXA R	100V Class 2SK 4048	100V Class 2SK 4049	100V Class 2SK 4050	130V Class 2SK 4214	130V Class 2SK 4215	130V Class 2SK 4216	200V Class 2SK 4051	200V Class 2SK 4052	200V Class 2SK 4053	250V Class 2SK 4054	250V Class 2SK 4055	250V Class 2SK 4056
E	**-1a**	**Total Dose Irradiation (TID)**	1019	Sample Size	Level I 4p([1]) Level II 4p([1])											
				Conditions	Total Dose 1×10^3Gy(Si) Dose Rate 36Gy(Si)/h to 360Gy(Si)/h Bias Condition (during irradiation, after irradiation) (a) V_{DS}=0V , V_{GS}=20V (b) V_{DS}=0V , V_{GS}=-20V											
					(c) V_{DS}=80V, V_{GS}=0V			(c) V_{DS}=104V, V_{GS}=0V			(c) V_{DS}=160V, V_{GS}=0V			(c) V_{DS}=200V, V_{GS}=0V		
	-1b	**End-Point Electrical Measurements**			Within 24hr after irradiation											
	(1)	Breakdown Voltage Drain to Source V_{DSS}	3407	Conditions	Bias Condition C I_D=1mA , V_{GS}=0V											
				Limits	min 100V DC			min 130V DC			min 200V DC			min 250V DC		
	(2)	Gate Current I_{GSS}	3411	Conditions	Bias Condition C V_{GS}=±20V , V_{DS}=0V											
				Limits	max ±100nA DC											
	(3)	Drain Current I_{DSS}	3413	Conditions	Bias Condition C V_{DS}=80V , V_{GS}=0V			Bias Condition C V_{DS}=104V , V_{GS}=0V			Bias Condition C V_{DS}=160V , V_{GS}=0V			Bias Condition C V_{DS}=200V , V_{GS}=0V		
				Limits	max 10μA DC											
	(4)	Gate to Source Voltage (Threshold) $V_{GS(th)}$	3404	Conditions	Bias Condition C V_{GS}=V_{DS} , I_D=1mA											
				Limits	min 1.5V DC $\Delta V_{GS(th)}$ max 2.0V											
	(5)	Static Drain to Source On-State Resistance $R_{DS(on)}$	3421	Conditions	Pulse Test([2]) , V_{GS}=12V											
					I_D			I_D			I_D			I_D		
					21A	21A	7.5A	21A	17.5A	7.5A	21A	16.5A	7A	21A	13.5A	6A
				Limits	max [mΩ]			max [mΩ]			max [mΩ]			max [mΩ]		
					18	33	69	24	46	96	33	69	155	45	98	230

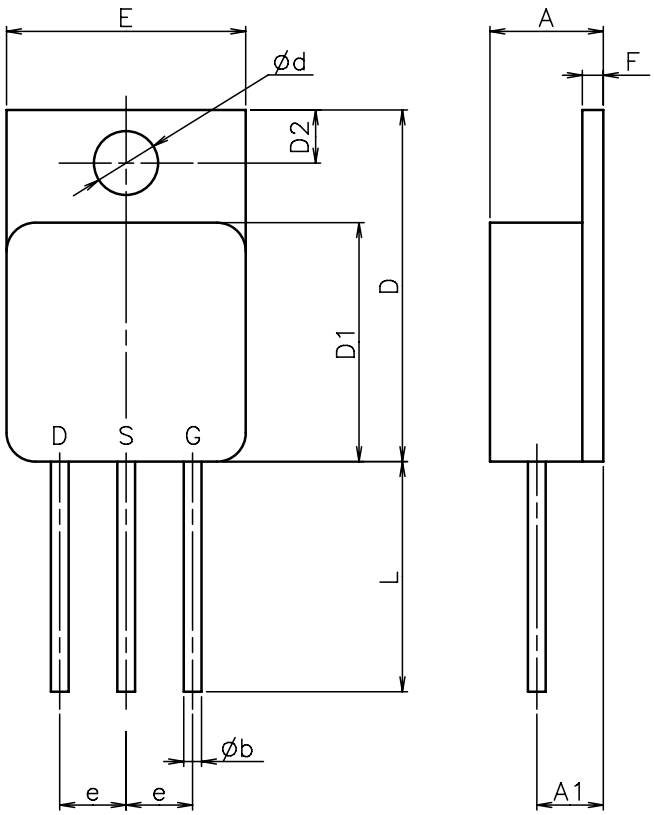
Notes([1]) This test shall be performed for each single wafer lot. When an inspection lot consists of multiple inspection sublots, one inspection sublot may be performed this test.

([2]) Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

Table 6. Exemption of Quality Conformance Inspection

When the qualification test or the quality conformance inspection for products specified as following table was initiated within a year from the completion date of the screening test for the inspection lot, and the device passed the test or inspection, the corresponding tests may be exempted.

Gr.No	Sub	JAXA R	100V Class			130V Class			200V Class			250V Class		
			2SK 4048	2SK 4049	2SK 4050	2SK 4214	2SK 4215	2SK 4216	2SK 4051	2SK 4052	2SK 4053	2SK 4054	2SK 4055	2SK 4056
		JAXA-QTS-2030 Appendix C	Die Size			Die Size			Die Size			Die Size		
		Test Item	1/1	1/2	1/4	1/1	1/2	1/4	1/1	1/2	1/4	1/1	1/2	1/4
C	**1-1a**	Intermittent Operation Life	These tests may be exempted when the following two conditions are satisfied. • When the devices having the same die size or larger die size passed. • When the devices passed using the value of V_{DS} defined in paragraph 1.2 or larger value of the V_{DS}.											
	1-1b	End-Point Electrical Measurements												
	-2a	Temperature Cycling												
	-2b	Hermetic Seal												
	-2c	End-Point Electrical Measurements												
	-3	Thermal Resistance	This test may be exempted when the device passed in the Group B-7 test.											
	-4a	Safe Operating Area Test	This test may be exempted when the device passed in the Group A-6 test.											
	-4b	End-Point Electrical Measurements												
D	**-1a**	Thermal Shock (Glass Strain)	This test may be exempted when any one of the products passed in the Group D-1 test.											
	-1b	Thermal Shock (Temperature Cycling)												
	-1c	Terminal Strength												
	-1d	Moisture Resistance												
	-1e	Hermetic Seal												
	-1f	Visual Inspection												
	-1g	End-Point Electrical Measurements												
	-2a	Shock												
	-2b	Vibration, Variable Frequency												
	-2c	Constant Acceleration												
	-2d	Hermetic Seal												
	-2e	End-Point Electrical Measurements												
	-3a	Salt Atmosphere	This test may be exempted when any one of the products passed in the Group D-3 test.											
	-4	Barometric Pressure	This test shall not be performed in the quality conformance inspection.									This test may be exempted when the device having same package passed in this test.		
	-5	Internal Water Vapor	This test may be exempted when any one of the products passed in the Group D-5 test.											



Symbol	Dimension (mm)	
	Min	Max
A	6.35	6.65
A1	3.61	4.01
øb	0.90	1.14
D	20.07	20.31
D1	13.59	13.85
D2	2.93	3.17

Symbol	Dimension (mm)	
	Min	Max
ød	3.56	3.80
E	13.60	13.84
e	3.51	4.11
F	1.10	1.30
L	12.84	13.60

Note: All leads are isolated from the case.

Figure 1. Package Configuration and Lead Connection of TO-254 type package

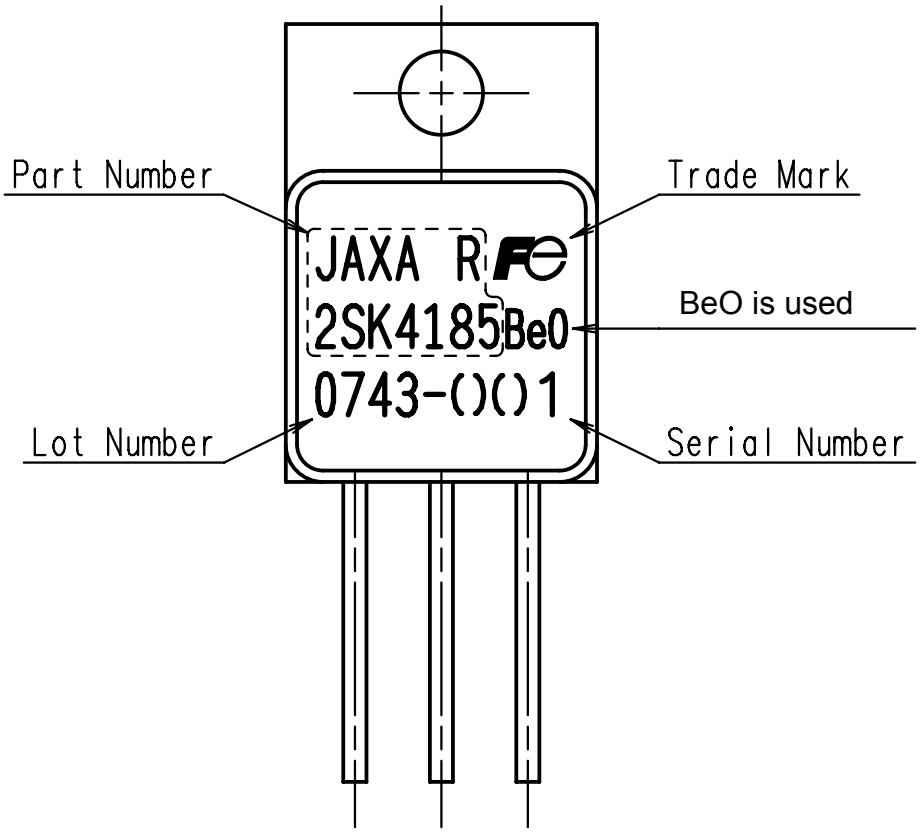


Figure 2. Marking

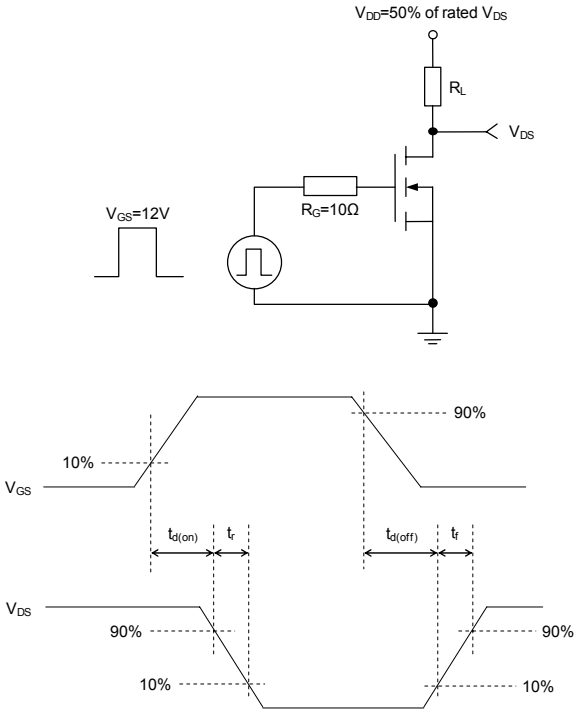


Figure 3. Switching time test circuit and waveforms

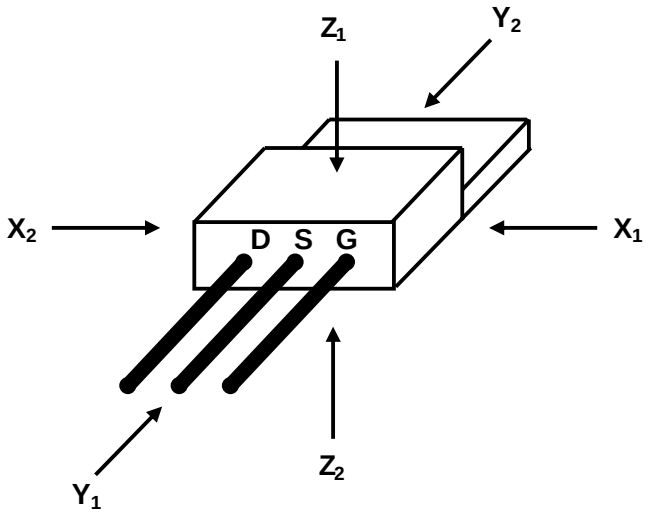


Figure 4. Orientation

JAXA R 2SK4048

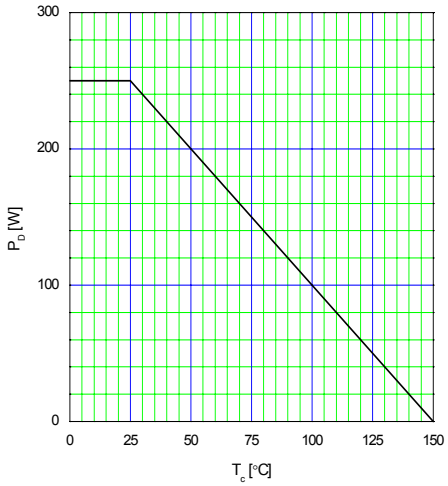


Fig. 5 Allowable Power Dissipation
$P_D=f(T_c)$

JAXA R 2SK4048

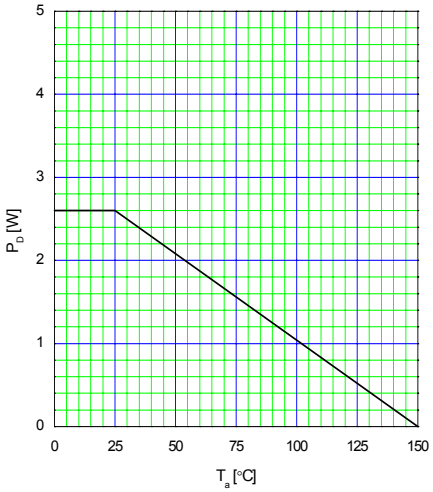


Fig. 6 Allowable Power Dissipation
$P_D=f(T_a)$

JAXA R 2SK4048

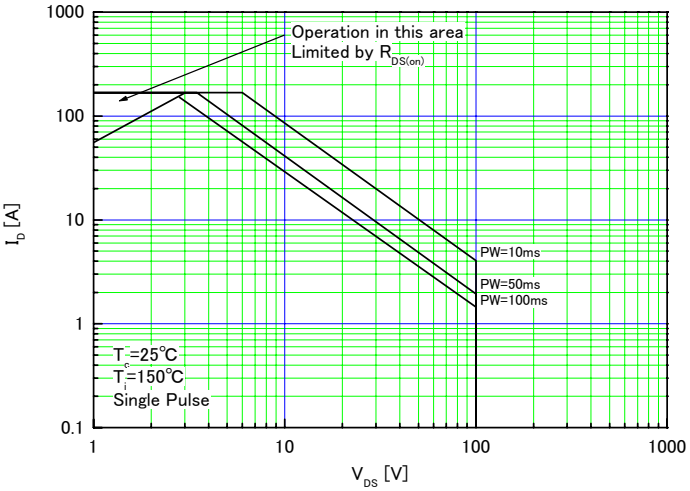


Fig. 7 Maximum Safe Operating Area
$I_D=f(V_{DS})$

JAXA R 2SK4049

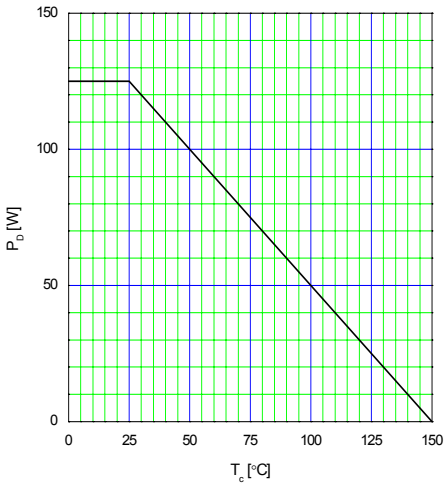


Fig. 8 Allowable Power Dissipation
$P_D=f(T_c)$

JAXA R 2SK4049

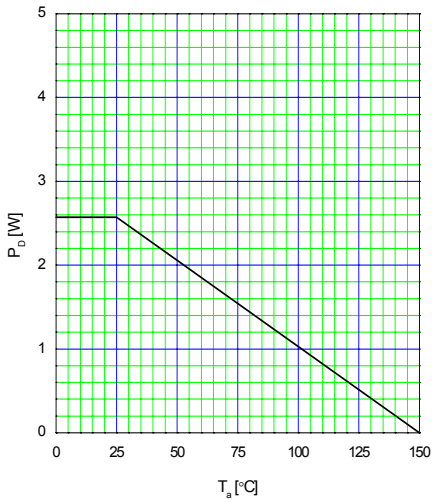


Fig. 9 Allowable Power Dissipation
$P_D=f(T_a)$

JAXA R 2SK4049

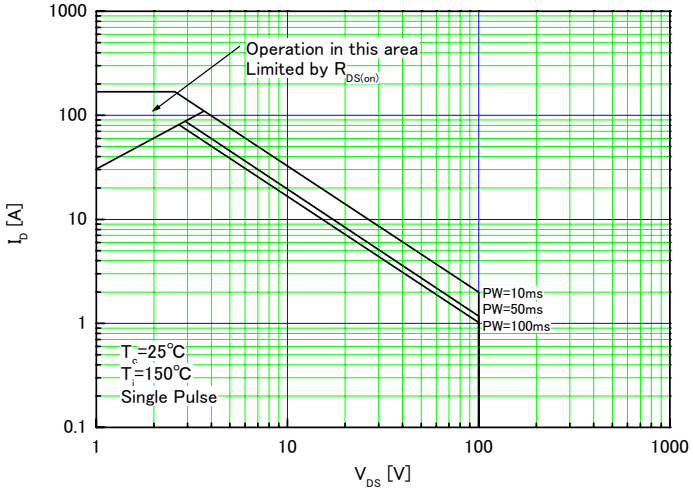


Fig. 10 Maximum Safe Operating Area
$I_D=f(V_{DS})$

JAXA R 2SK4050

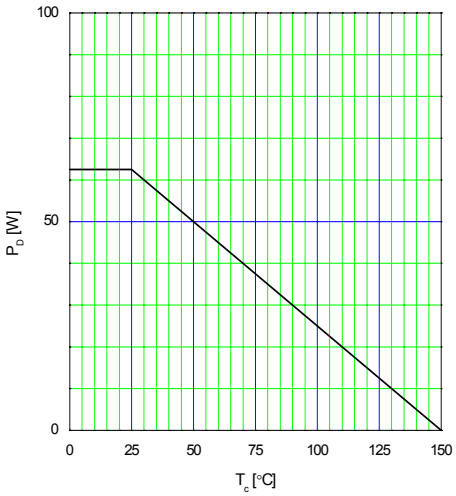


Fig. 11 Allowable Power Dissipation
$P_D=f(T_c)$

JAXA R 2SK4050

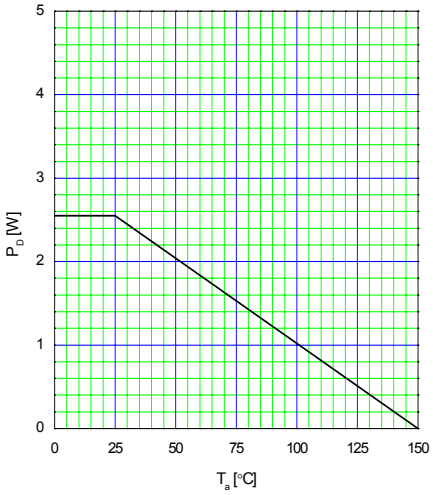


Fig. 12 Allowable Power Dissipation
$P_D=f(T_a)$

JAXA R 2SK4050

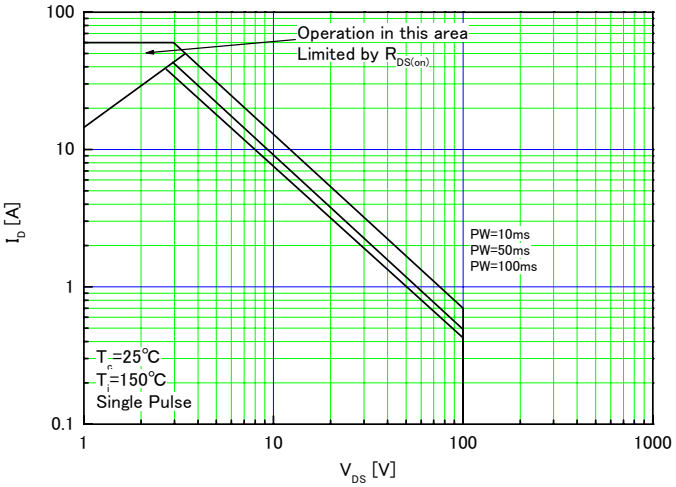


Fig. 13 Maximum Safe Operating Area
$I_D=f(V_{DS})$

JAXA R 2SK4051

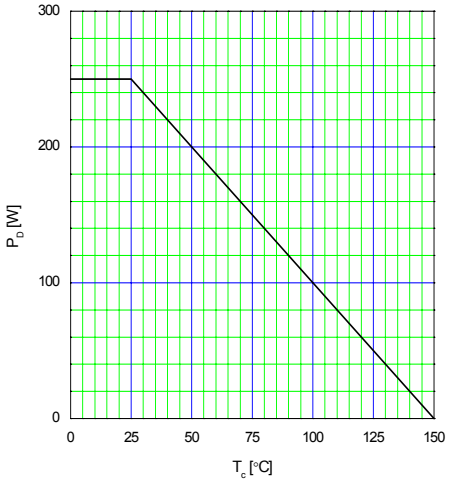


Fig. 14 Allowable Power Dissipation
$P_D=f(T_c)$

JAXA R 2SK4051

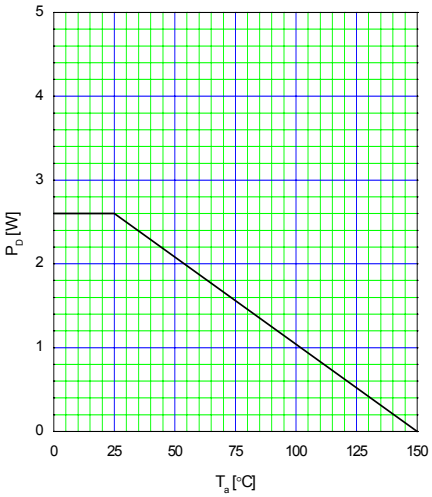


Fig. 15 Allowable Power Dissipation
$P_D=f(T_a)$

JAXA R 2SK4051

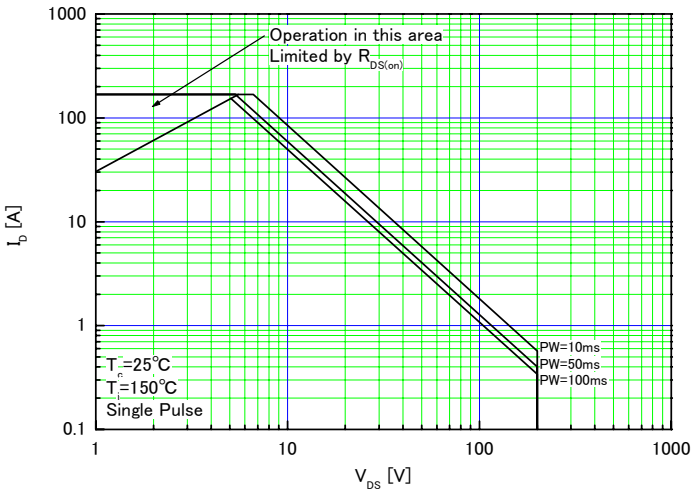


Fig. 16 Maximum Safe Operating Area
$I_D=f(V_{DS})$

JAXA R 2SK4052

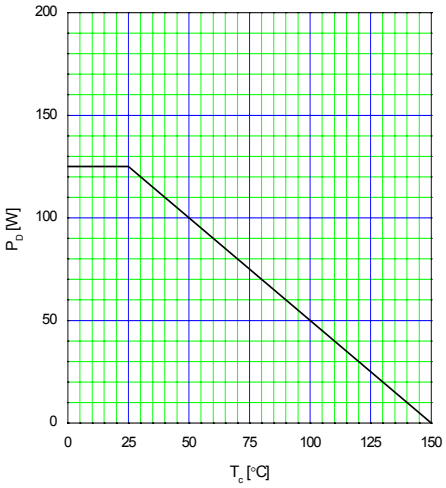


Fig. 17 Allowable Power Dissipation $P_D=f(T_c)$

JAXA R 2SK4052

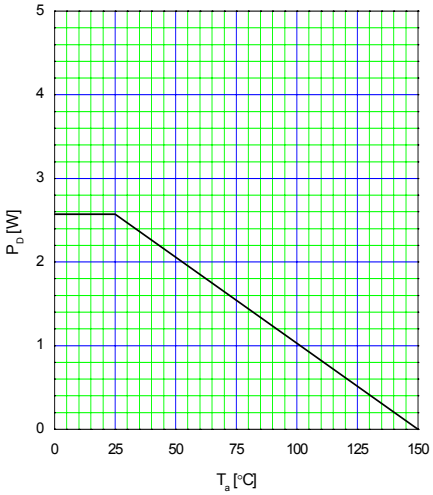


Fig. 18 Allowable Power Dissipation $P_D=f(T_a)$

JAXA R 2SK4052

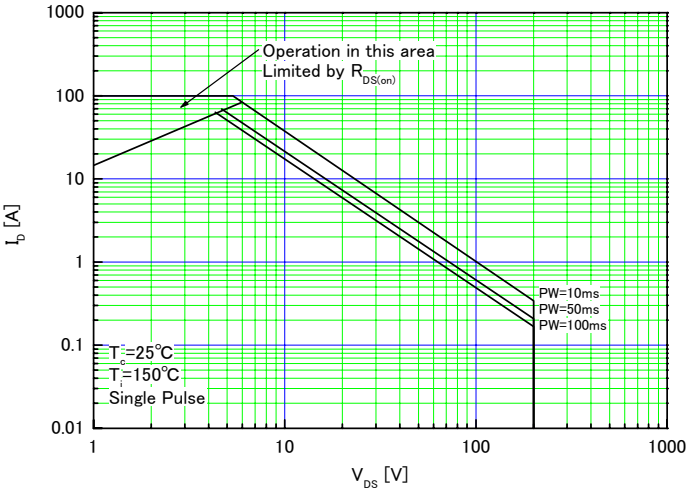


Fig. 19 Maximum Safe Operating Area $I_D=f(V_{DS})$

JAXA R 2SK4053

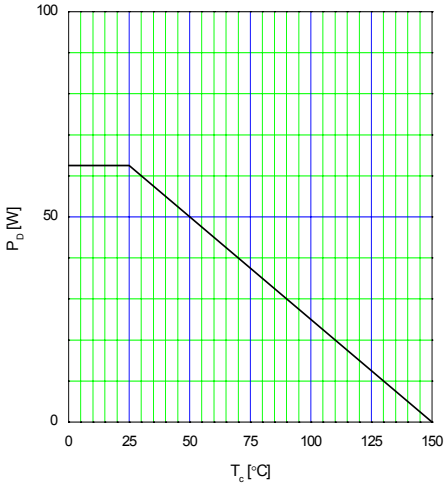


Fig. 20 Allowable Power Dissipation $P_D=f(T_c)$

JAXA R 2SK4053

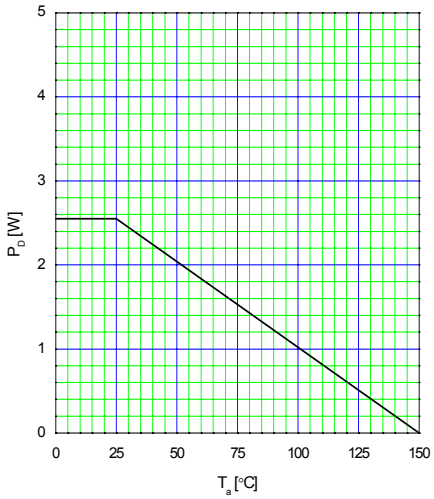


Fig. 21 Allowable Power Dissipation $P_D=f(T_a)$

JAXA R 2SK4053

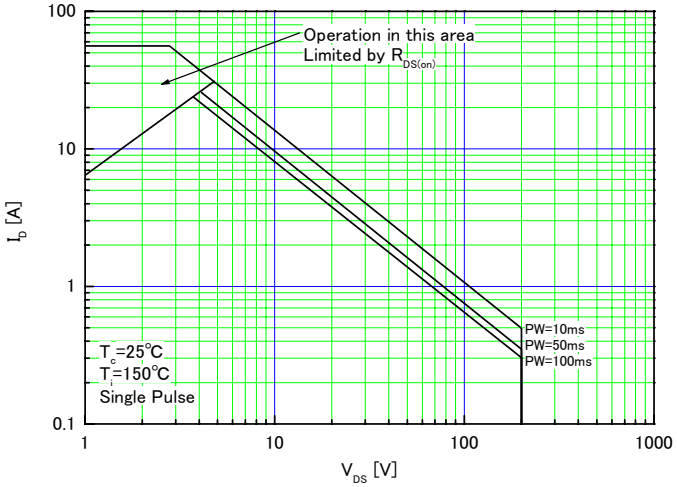


Fig. 22 Maximum Safe Operating Area $I_D=f(V_{DS})$

JAXA R 2SK4054

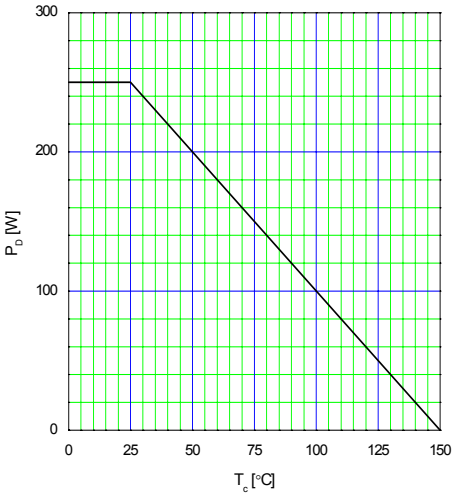


Fig. 23 Allowable Power Dissipation
$P_D=f(T_c)$

JAXA R 2SK4054

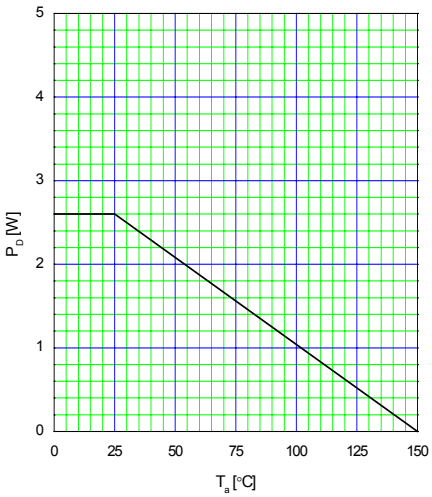


Fig. 24 Allowable Power Dissipation
$P_D=f(T_a)$

JAXA R 2SK4054

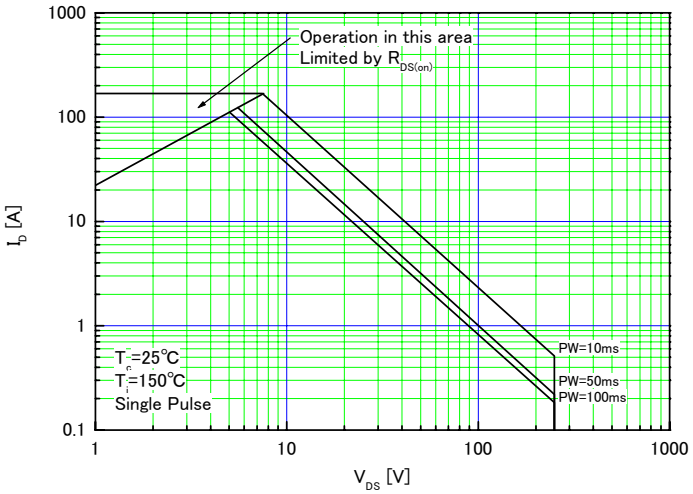


Fig. 25 Maximum Safe Operating Area
$I_D=f(V_{DS})$

JAXA R 2SK4055

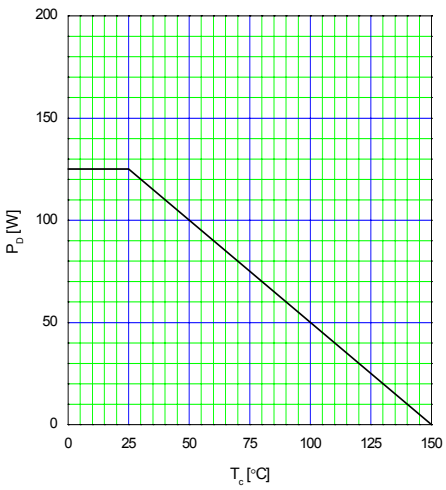


Fig. 26 Allowable Power Dissipation
$P_D=f(T_c)$

JAXA R 2SK4055

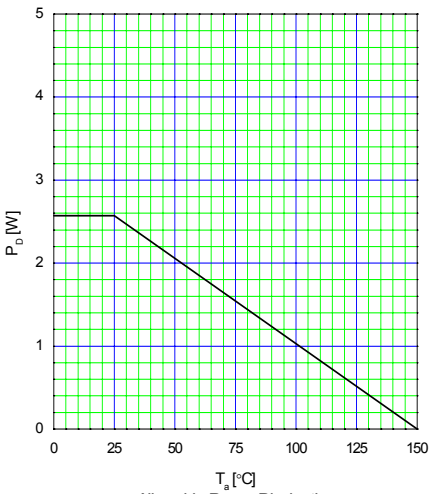


Fig. 27 Allowable Power Dissipation
$P_D=f(T_a)$

JAXA R 2SK4055

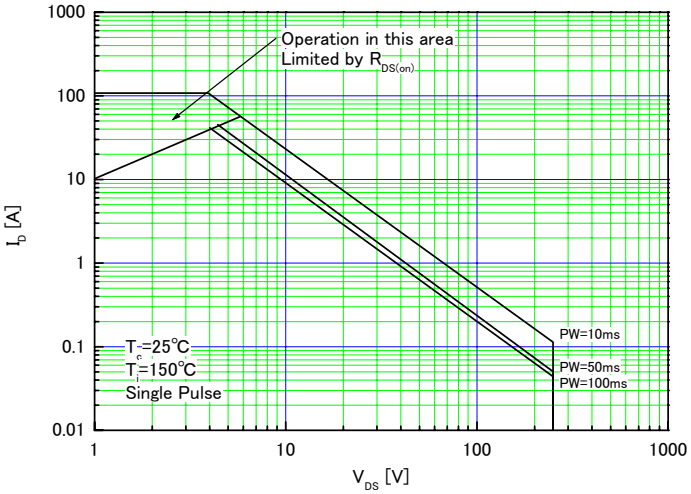


Fig. 28 Maximum Safe Operating Area
$I_D=f(V_{DS})$

JAXA R 2SK4056

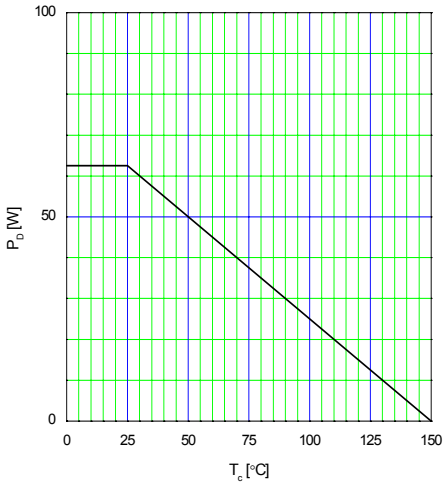


Fig. 29 Allowable Power Dissipation $P_D=f(T_c)$

JAXA R 2SK4056

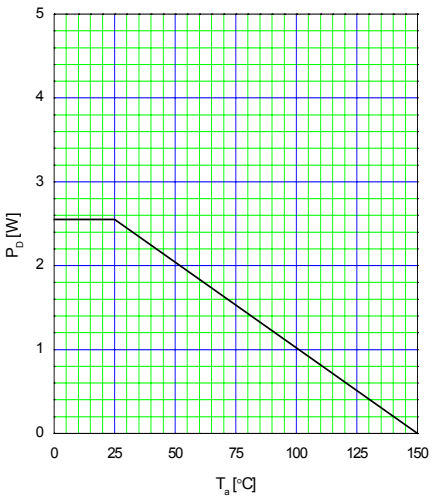


Fig. 30 Allowable Power Dissipation $P_D=f(T_a)$

JAXA R 2SK4056

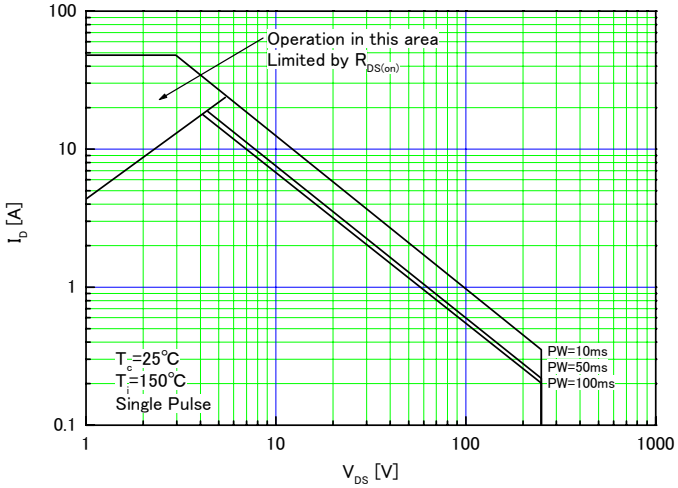


Fig. 31 Maximum Safe Operating Area $I_D=f(V_{DS})$

JAXA R 2SK4214

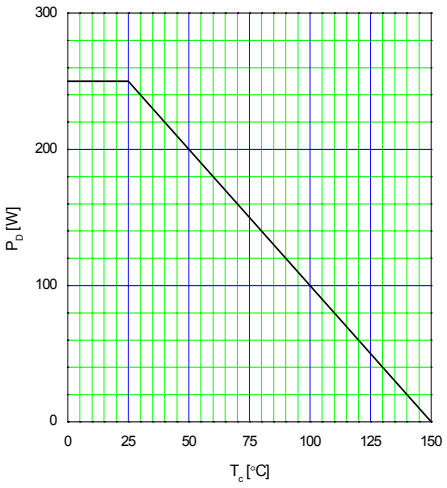


Fig. 32 Allowable Power Dissipation $P_D=f(T_c)$

JAXA R 2SK4214

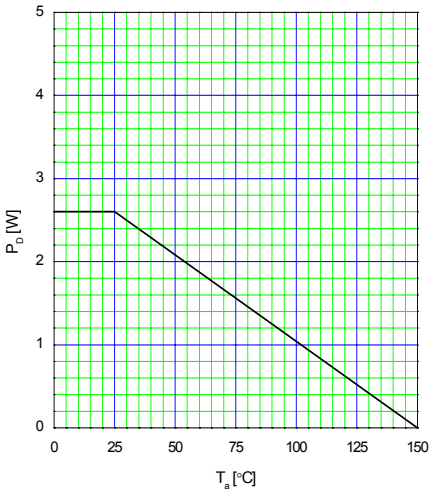


Fig. 33 Allowable Power Dissipation $P_D=f(T_a)$

JAXA R 2SK4214

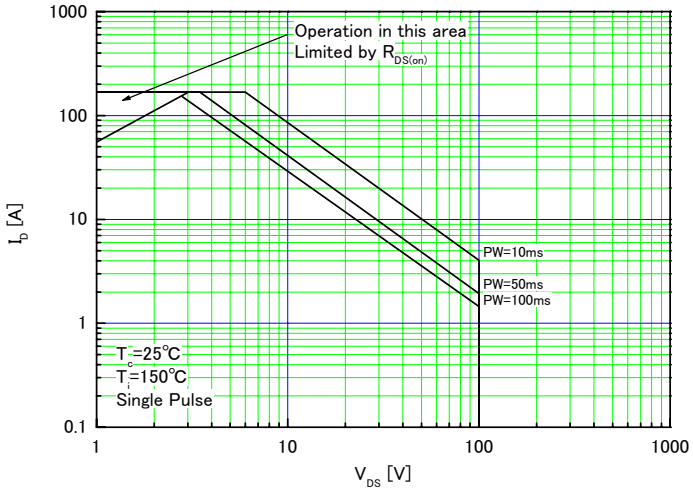


Fig. 34 Maximum Safe Operating Area $I_D=f(V_{DS})$

JAXA R 2SK4215

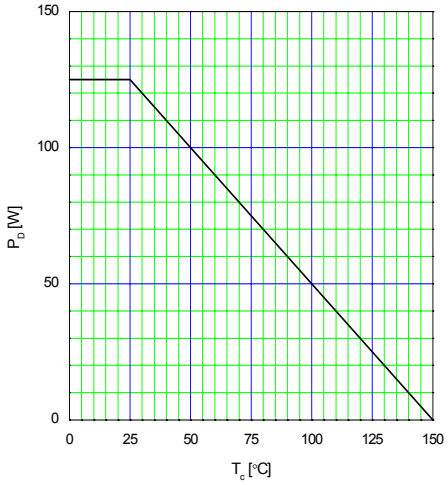


Fig. 35 Allowable Power Dissipation $P_D=f(T_c)$

JAXA R 2SK4215

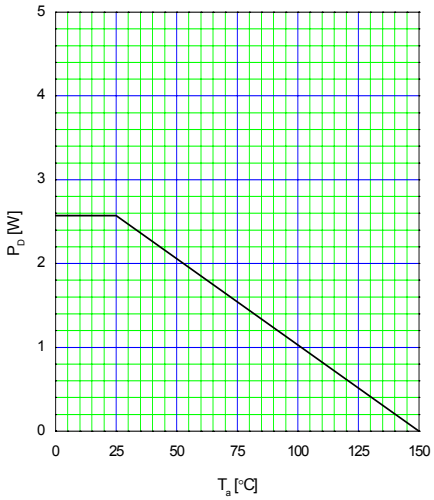


Fig. 36 Allowable Power Dissipation $P_D=f(T_a)$

JAXA R 2SK4215

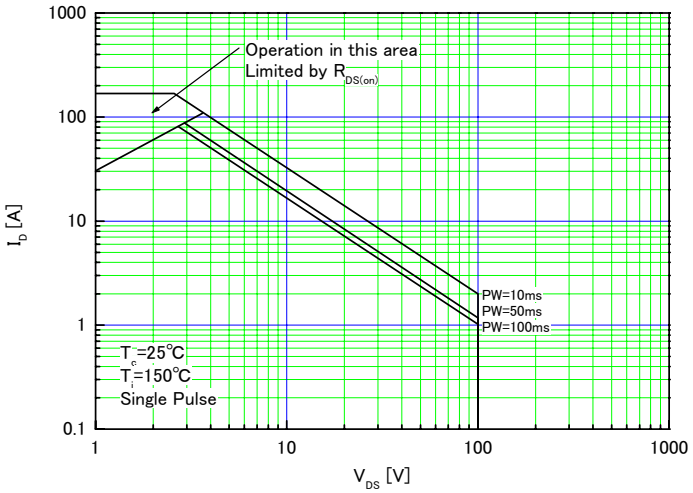


Fig. 37 Maximum Safe Operating Area $I_D=f(V_{DS})$

JAXA R 2SK4216

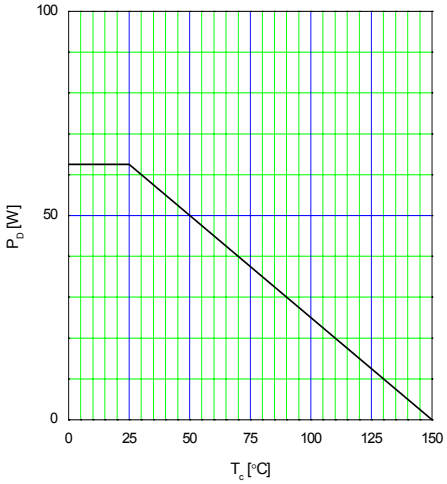


Fig. 38 Allowable Power Dissipation $P_D=f(T_c)$

JAXA R 2SK4216

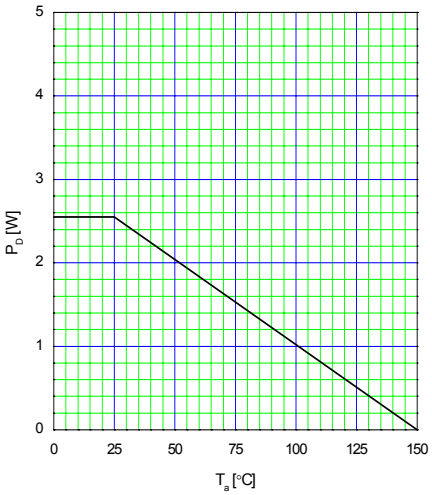


Fig. 39 Allowable Power Dissipation $P_D=f(T_a)$

JAXA R 2SK4216

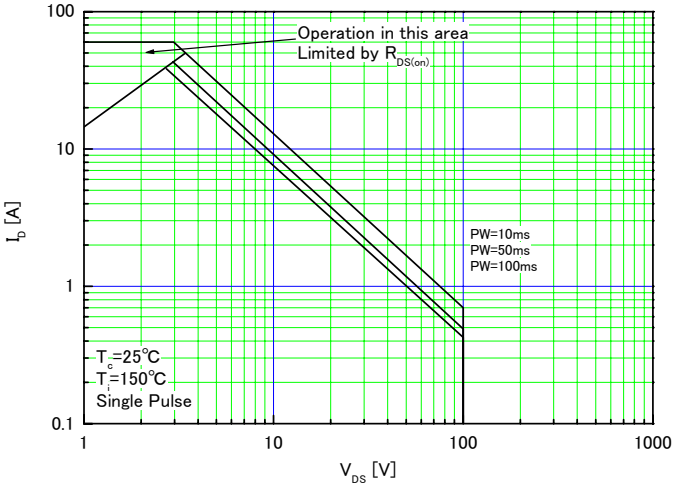


Fig. 40 Maximum Safe Operating Area $I_D=f(V_{DS})$