
HM62V16256B Series

4 M SRAM (256-kword × 16-bit)

HITACHI

ADE-203-933B (Z)

Rev. 1.0

March 8, 1999

Description

The Hitachi HM62V16256B Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62V16256B Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.

Features

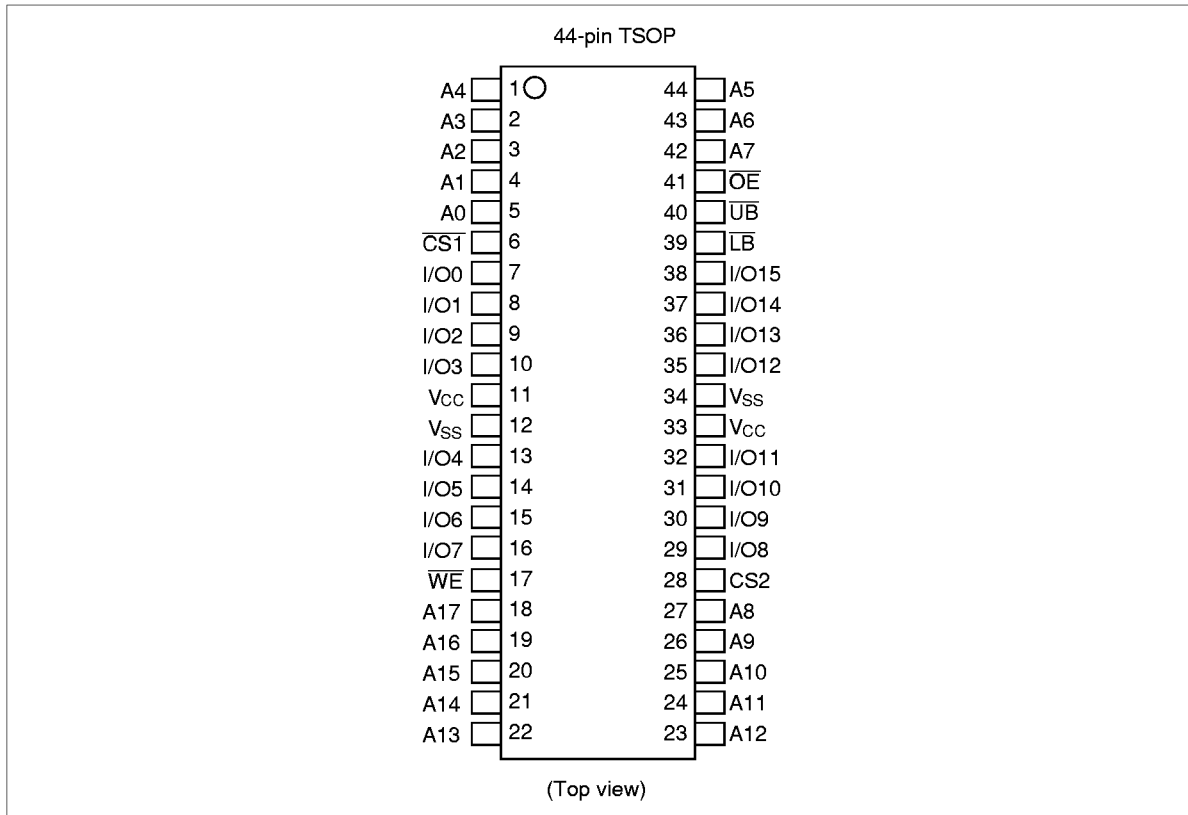
- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 70 ns/85 ns (max)
- Power dissipation:
 - Active: 9 mW (typ)
 - Standby: 3 μW (typ)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup

Ordering Information

Type No.	Access time	Package
HM62V16256BLTT-7	70 ns	400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB)
HM62V16256BLTT-8	85 ns	
HM62V16256BLTT-7SL	70 ns	
HM62V16256BLTT-8SL	85 ns	

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Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
\overline{WE}	Write enable
\overline{OE}	Output enable
\overline{LB}	Lower byte select
\overline{UB}	Upper byte select
V _{CC}	Power supply
V _{SS}	Ground

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Operation Table

$\overline{CS1}$	$\overline{CS2}$	\overline{WE}	\overline{OE}	\overline{UB}	\overline{LB}	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-10 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +4.6 V.

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DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	1
Ambient temperature range	T_a	0	—	70	°C	

Note: 1. V_{IL} min: -3.0 V for pulse half-width \leq 30 ns.

DC Characteristics

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions	
Input leakage current	$ I_{LI} $	—	—	1	μ A	$V_{in} = V_{SS}$ to V_{CC}	
Output leakage current	$ I_{LO} $	—	—	1	μ A	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, or $\overline{LB} = \overline{UB} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	
Operating current	I_{CC}	—	—	20	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL} , $I_{I/O} = 0$ mA	
Average operating current	HM62V16256B-7	I_{CC1}	—	—	70	mA	Min. cycle, duty = 100%, $I_{I/O} = 0$ mA, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL}
	HM62V16256B-8	I_{CC1}	—	—	65	mA	
		I_{CC2}	—	3	15	mA	Cycle time = 1 μ s, duty = 100%, $I_{I/O} = 0$ mA, $\overline{CS1} \leq 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current	I_{SB}	—	—	0.3	mA	$CS2 = V_{IL}$	
Standby current	I_{SB1}^{*2}	—	1	40	μ A	0 V \leq V_{in} (1) 0 V \leq $CS2 \leq 0.2$ V or (2) $\overline{CS1} \geq V_{CC} - 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V	
		I_{SB1}^{*3}	—	1	20	μ A	
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1$ mA	
		$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100$ μ A	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2$ mA	
		—	—	0.2	V	$I_{OL} = 100$ μ A	

Notes: 1. Typical values are at $V_{CC} = 3.0$ V, $T_a = +25^\circ$ C and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.

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Capacitance ($T_a = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0\text{ V}$	1
Input/output capacitance	$C_{i/o}$	—	—	10	pF	$V_{i/o} = 0\text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$ to 3.6 V , unless otherwise noted.)

Test Conditions

- Input pulse levels: $V_{IL} = 0.4\text{ V}$, $V_{IH} = 2.2\text{ V}$
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference levels: 1.4 V
- Output load: 1 TTL + 30 pF (HM62V16256B-7) (Including scope and jig)
1 TTL + 100 pF (HM62V16256B-8) (Including scope and jig)

Read Cycle

HM62V16256B							
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	70	—	85	—	ns	
Address access time	t_{AA}	—	70	—	85	ns	
Chip select access time	t_{ACS1}	—	70	—	85	ns	
	t_{ACS2}	—	70	—	85	ns	
Output enable to output valid	t_{OE}	—	40	—	45	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
\overline{LB} , \overline{UB} access time	t_{BA}	—	70	—	85	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	2, 3
	t_{CLZ2}	10	—	10	—	ns	2, 3
\overline{LB} , \overline{UB} enable to low-z	t_{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	25	0	25	ns	1, 2, 3
	t_{CHZ2}	0	25	0	25	ns	1, 2, 3
\overline{LB} , \overline{UB} disable to high-Z	t_{BHZ}	0	25	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	25	0	25	ns	1, 2, 3

HM62V16256B Series

Write Cycle

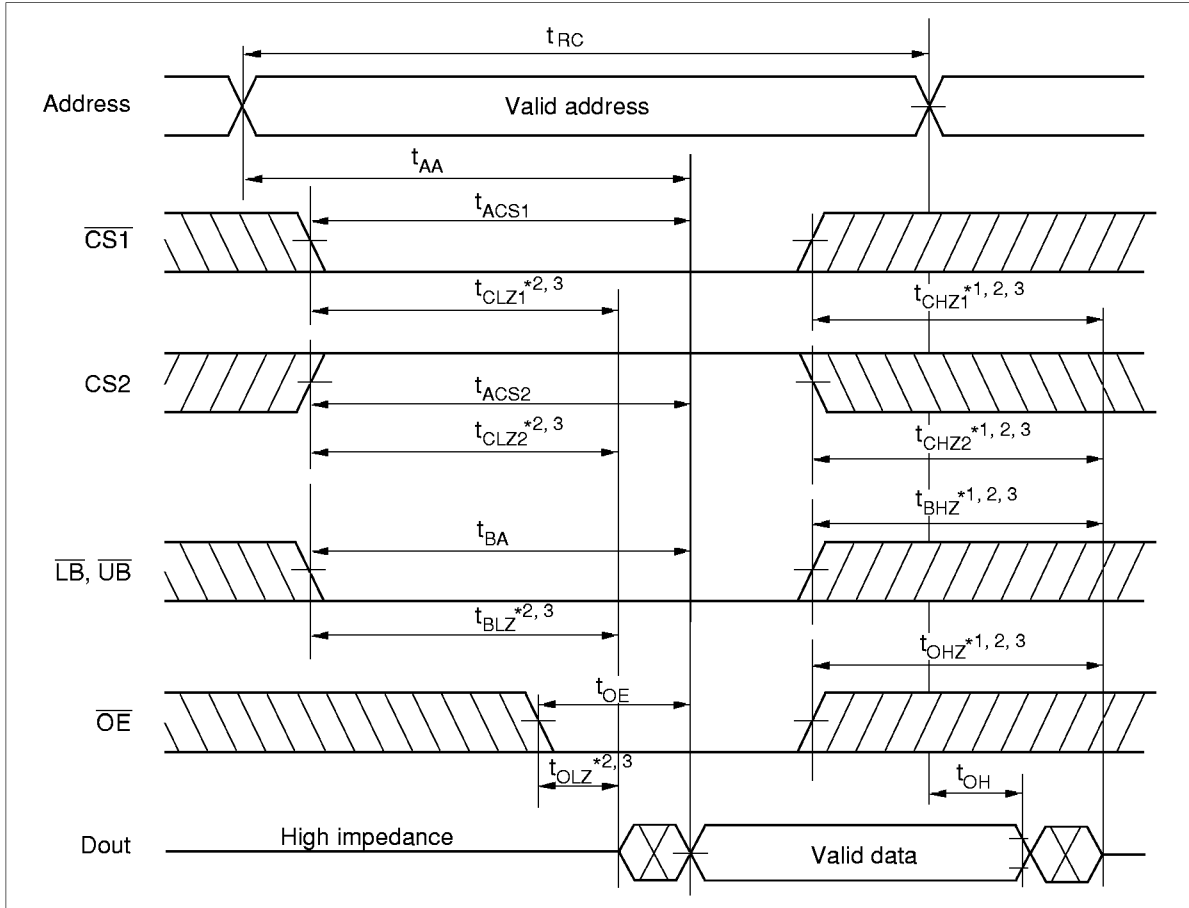
HM62V16256B							
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	70	—	85	—	ns	
Address valid to end of write	t_{AW}	60	—	70	—	ns	
Chip selection to end of write	t_{CW}	60	—	70	—	ns	5
Write pulse width	t_{WP}	50	—	55	—	ns	4
\overline{LB} , \overline{UB} valid to end of write	t_{BW}	55	—	70	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	25	0	25	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	25	0	25	ns	1, 2

- Notes:
1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, a low \overline{WE} and a low \overline{LB} or a low \overline{UB} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, \overline{WE} going low and \overline{LB} going low or \overline{UB} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, \overline{WE} going high and \overline{LB} going high or \overline{UB} going high. t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 6. t_{AS} is measured from the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or CS2 going low to the end of write cycle.

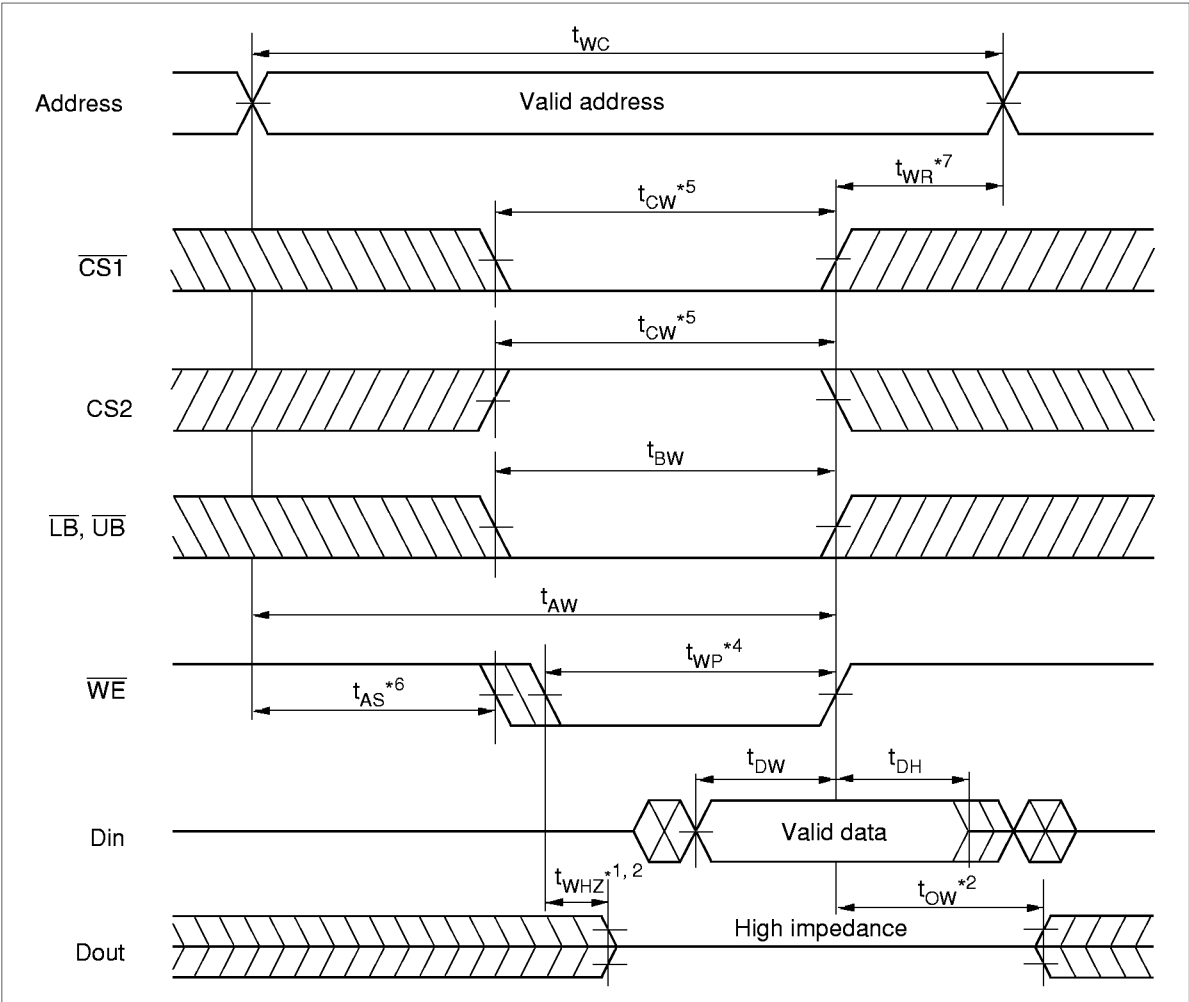
HM62V16256B Series

Timing Waveform

Read Cycle

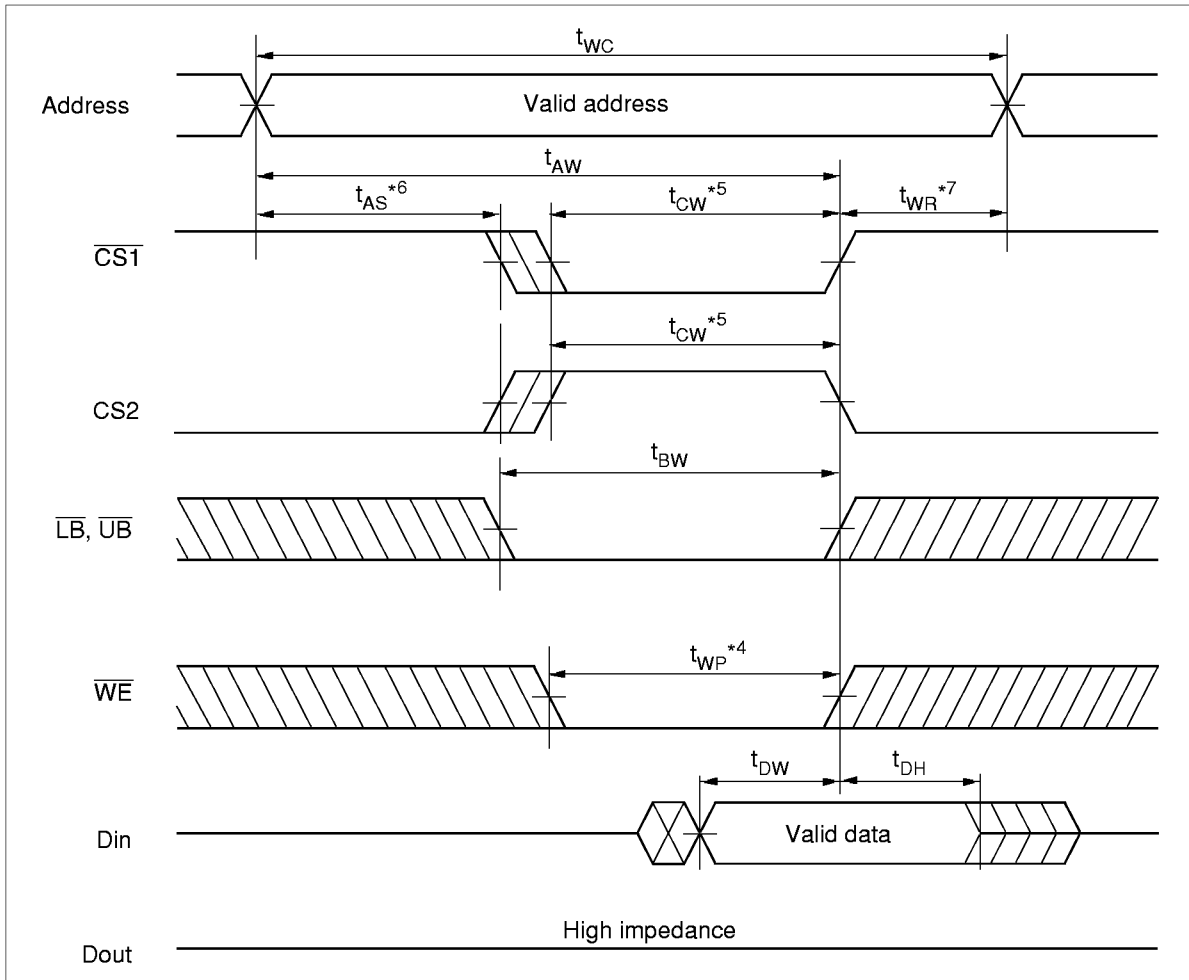


Write Cycle (1) (\overline{WE} Clock)

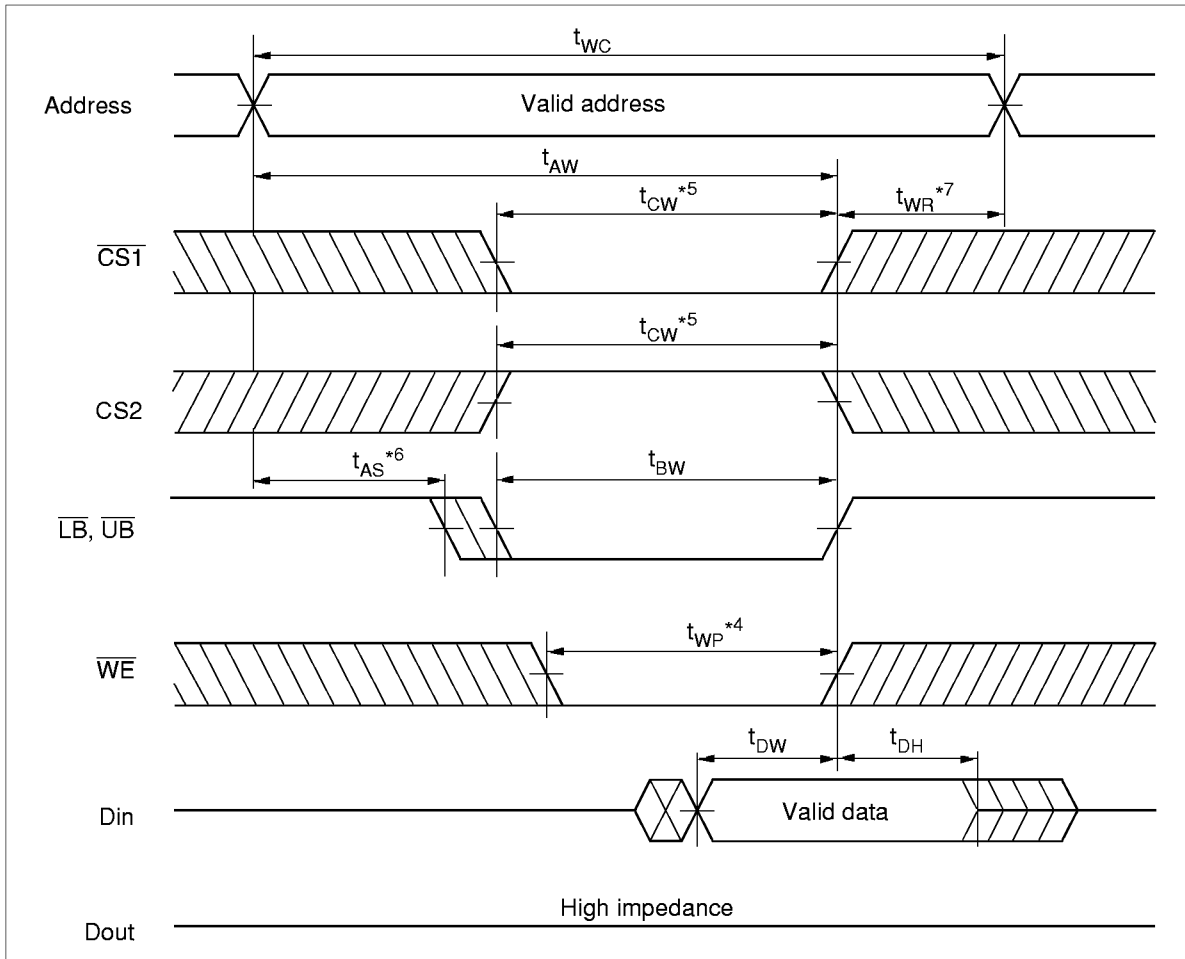


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Write Cycle (2) (\overline{CS} Clock, $\overline{OE} = V_{IH}$)



Write Cycle (3) ($\overline{\text{LB}}, \overline{\text{UB}}$ Clock, $\overline{\text{OE}} = V_{\text{IH}}$)



Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

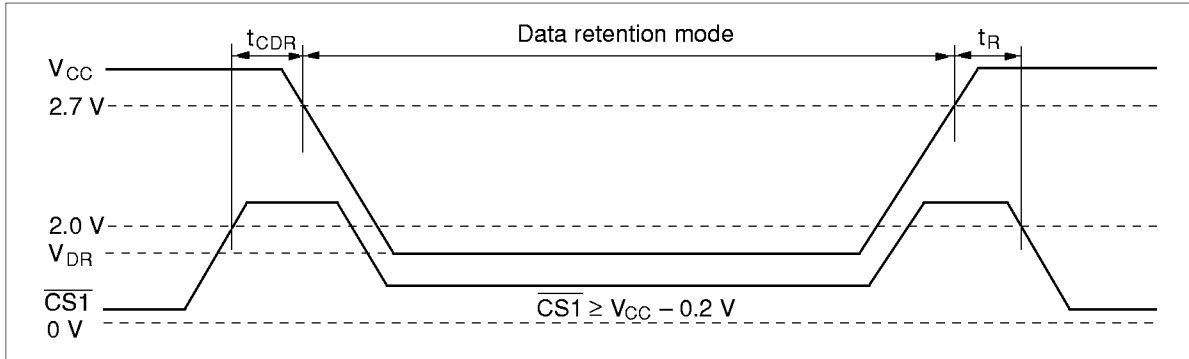
Parameter	Symbol	Min	Typ ^{*4}	Max	Unit	Test conditions ^{*3}
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{\text{in}} \geq 0\text{V}$ (1) $0\text{V} \leq \text{CS2} \leq 0.2\text{V}$ or $\text{CS2} \geq V_{\text{CC}} - 0.2\text{V}$ $\text{CS1} \geq V_{\text{CC}} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{\text{CC}} - 0.2\text{V}$ $\text{CS2} \geq V_{\text{CC}} - 0.2\text{V}$ $\text{CS1} \leq 0.2\text{V}$
Data retention current	$I_{\text{CCDR}}^{\text{*1}}$	—	0.8	20	μA	$V_{\text{CC}} = 3.0\text{V}$, $V_{\text{in}} \geq 0\text{V}$ (1) $0\text{V} \leq \text{CS2} \leq 0.2\text{V}$ or $\text{CS2} \geq V_{\text{CC}} - 0.2\text{V}$, $\text{CS1} \geq V_{\text{CC}} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{\text{CC}} - 0.2\text{V}$ $\text{CS2} \geq V_{\text{CC}} - 0.2\text{V}$ $\text{CS1} \leq 0.2\text{V}$

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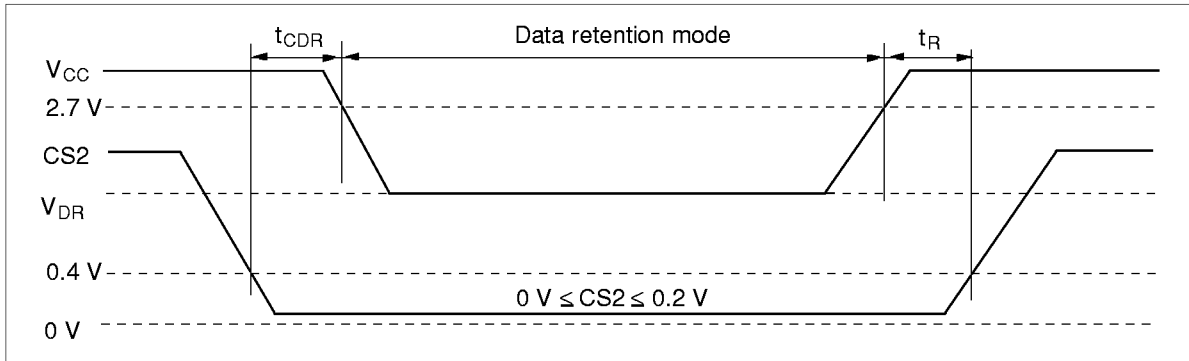
Parameter	Symbol	Min	Typ* ⁴	Max	Unit	Test conditions* ³
	I_{CCDR}^{*2}	—	0.8	10	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*5}	—	—	ns	

- Notes:
1. This characteristic is guaranteed only for L-version, 10 μA max. at $T_a = 0$ to $+40^\circ C$.
 2. This characteristic is guaranteed only for L-SL version, 5 μA max. at $T_a = 0$ to $+40^\circ C$.
 3. CS2 controls address buffer, \overline{WE} buffer, $\overline{CS1}$ buffer, \overline{OE} buffer, \overline{LB} , \overline{UB} buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, \overline{WE} , \overline{OE} , $\overline{CS1}$, \overline{LB} , \overline{UB} , I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2 V$ or $0 V \leq CS2 \leq 0.2 V$. The other input levels (address, \overline{WE} , \overline{OE} , \overline{LB} , \overline{UB} , I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 3.0 V$, $T_a = +25^\circ C$ and not guaranteed.
 5. t_{RC} = read cycle time.

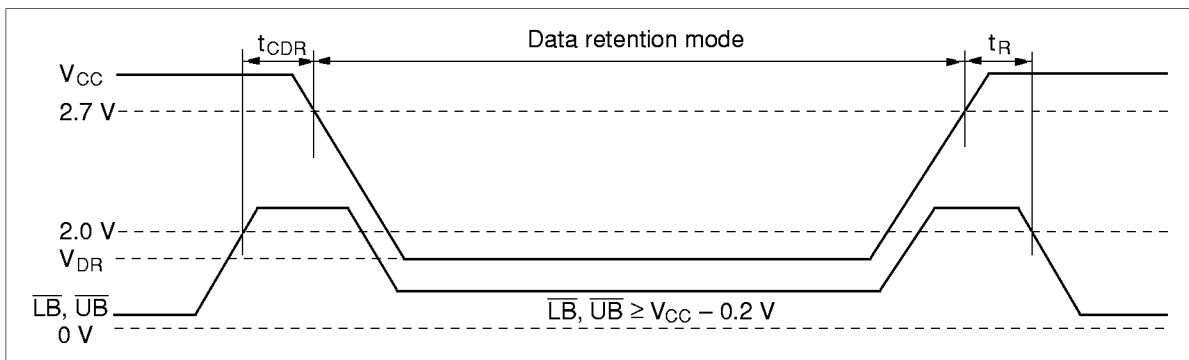
Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) ($CS2$ Controlled)



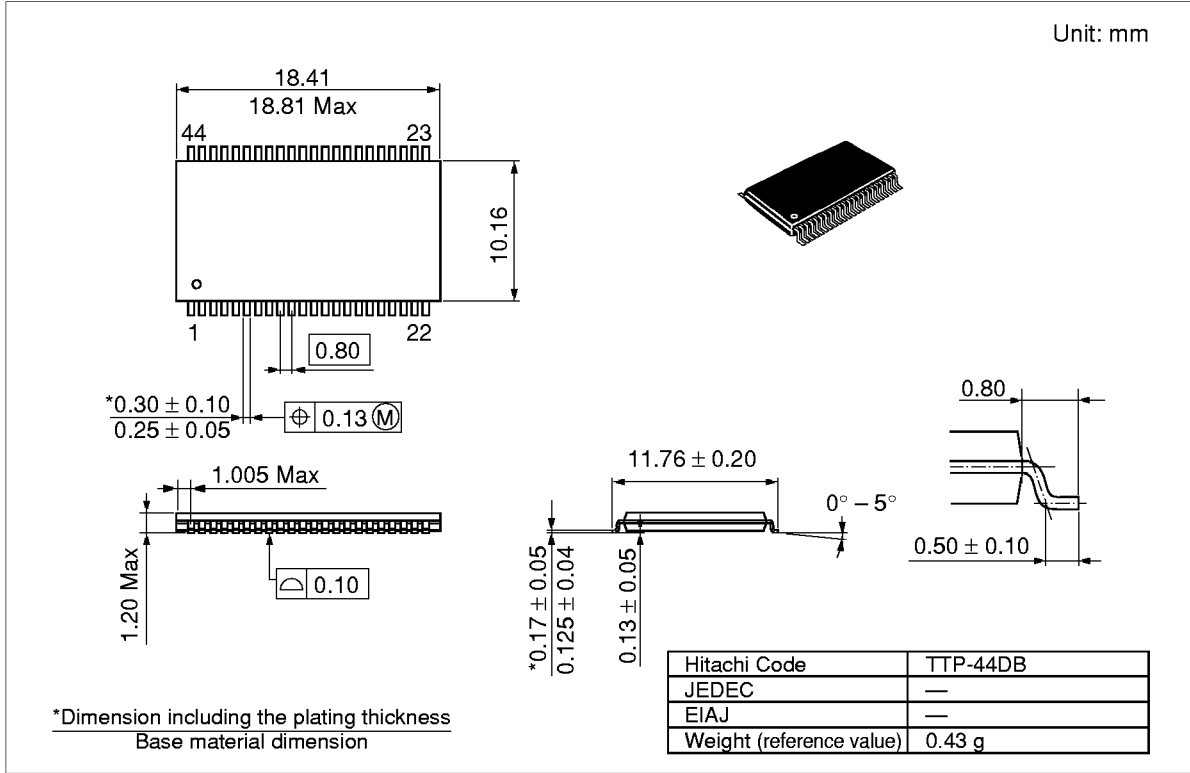
Low V_{CC} Data Retention Timing Waveform (3) (\overline{LB} , \overline{UB} Controlled)



HM62V16256B Series

Package Dimensions

HM62V16256BLTT Series (TTP-44DB)



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HM62V16256B Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 26, 1998	Initial issue	M.Higuchi	K. Imato
0.1	Nov. 25, 1998	Change of format Features Change of Power dissipation Active: 15 mW (typ) to TBD mW (typ) Standby: 1.5 μ W (typ) to TBD μ W (typ) Change of Pin Arrangement (CSP) Change of Block Diagram DC Characteristics I_{CC2} typ: — mA to TBD mA I_{SB1} typ: —/— μ A to TBD/TBD μ A I_{SB1} max: 20/2 μ A to 40/20 μ A AC Characteristics t_{BW} min: 60/70 ns to 55/70 ns t_{WP} min: 55/70 ns to 50/55 ns Low V_{CC} Data Retention Characteristics I_{CCDR} typ: 1/1 μ A to —/— μ A I_{CCDR} max: 10/1 μ A to 20/10 μ A Change of note1 and 2 Change of Timing Waveform(1),(2) and (3)	M.Higuchi	K. Imato
1.0	Mar. 8, 1999	Deletion of HM62V16256BLBT Series (TBT-48) Features: Change of Power dissipation Active: TBD mW (typ) to 9 mW (typ) Standby: TBD μ W (typ) to 3 μ W (typ) DC Characteristics I_{CC2} typ: TBD mA to 3 mA I_{SB1} typ: TBD/TBD μ A to 1/1 μ A AC Characteristics t_{OE} max: 35/45 ns to 40/45 ns Low V_{CC} Data Retention Characteristics I_{CCDR} typ: —/— μ A to 0.8/0.8 μ A		
