

# 1Gb C-die DDR3 SDRAM Specification

**Revision 1.0**

**June 2007**

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**Revision History**

| Revision | Month   | Year | History   |
|----------|---------|------|---|
| 0.0      | January | 2007 | - Revision 0.0 release  |
| 0.1      | June    | 2007 | - Deleted 800Mbps 5-5-5 speed<br>- Timing Parameters by Speed Grade (13.0)<br>- Input/Output Capacitance (11.0) |
| 1.0      | June    | 2007 | - Revision 1.0 specification release.   |
|          |         |      |   |

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## 1.0 Ordering Information

[ Table 1 ] Samsung DDR3 ordering information table

| Organization | DDR3-800 (6-6-6) | DDR3-1066 (7-7-7/8-8-8) | DDR3-1333 (8-8-8/9-9-9) | Package  |
|--------------|------------------|-------------------------|-------------------------|----------|
| 256Mx4       | K4B1G0446C-ZCF7  | K4B1G0446C-CF8/G8       | K4B1G0446C-ZCG9/H9      | 94 FBGA  |
| 128Mx8       | K4B1G0846C-ZCF7  | K4B1G0846C-CF8/G8       | K4B1G0846C-ZCG9/H9      | 94 FBGA  |
| 64Mx16       | K4B1G1646C-ZCF7  | K4B1G1646C-CF8/G8       | K4B1G1646C-ZCG9/H9      | 112 FBGA |

Note :

1. Speed bin is in order of CL-tRCD-tRP.
2. x4/x8/x16 Package - including 16 support balls

## 2.0 Key Features

[ Table 2 ] 1Gb DDR3 C-die Speed bins

| Speed       | DDR3-800 | DDR3-1066 |       | DDR3-1333 |       | Unit |
|-------------|----------|-----------|-------|-----------|-------|------|
|             | 6-6-6    | 7-7-7     | 8-8-8 | 8-8-8     | 9-9-9 |      |
| tCK(min)    | 2.5      | 1.875     |       | 1.5       |       | ns   |
| CAS Latency | 6        | 7         | 8     | 8         | 9     | tCK  |
| tRCD(min)   | 15       | 13.125    | 15    | 12        | 13.5  | ns   |
| tRP(min)    | 15       | 13.125    | 15    | 12        | 13.5  | ns   |
| tRAS(min)   | 37.5     | 37.5      | 37.5  | 36        | 36    | ns   |
| tRC(min)    | 52.5     | 50.625    | 52.5  | 48        | 49.5  | ns   |

- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- 400 MHz f<sub>CK</sub> for 800Mb/sec/pin, 533MHz f<sub>CK</sub> for 1066Mb/sec/pin, 667MHz f<sub>CK</sub> for 1333Mb/sec/pin
- 8 Banks
- Posted CAS
- Programmable CAS Latency: 5, 6, 7, 8, 9, 10, (11 for high density only)
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than T<sub>CASE</sub> 85×C, 3.9us at 85×C < T<sub>CASE</sub> ≤ 95 ×C
- Asynchronous Reset
- Package : 94 balls FBGA - x4/x8 (with 16 support balls)  
112 balls FBGA - x16 (with 16 support balls)
- All of Lead-free products are compliant for RoHS

The 1Gb DDR3 SDRAM C-die is organized as a 32Mbit x 4/16Mbit x 8/8Mbit x 16 I/Os x 8banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 1333Mb/sec/pin (DDR3-1333) for general applications.

The chip is designed to comply with the following key DDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset .

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and  $\overline{CK}$  falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and  $\overline{DQS}$ ) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a  $\overline{RAS}/\overline{CAS}$  multiplexing style. The DDR3 device operates with a single 1.5V ± 0.075V power supply and 1.5V ± 0.075V VDDQ.

The 1Gb DDR3 device is available in 94ball FBGAs(x4/x8) and 112ball FBGA(x16)

Note : 1. The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

2. 1066Mbps CL7 doesn't have back-ward compatibility with 800Mbps CL5

Note : This data sheet is an abstract of full DDR3 specification and does not cover the common features which are described in "DDR3 SDRAM Device Operation & Timing Diagram".

3.0 Package pinout/Mechanical Dimension & Addressing

3.1 x4 Package Pinout (Top view) : 94ball FBGA Package(78balls + 16 balls of support balls)

|   | 1  | 2      | 3                         | 4                       | 5 | 6 | 7 | 8                           | 9      | 10   | 11 |   |
|---|----|--------|---------------------------|-------------------------|---|---|---|-----------------------------|--------|------|----|---|
| A | NC | NC     |                           | NC                      |   |   |   | NC                          |        | NC   | NC |   |
| B |    |        |                           |                         |   |   |   |                             |        |      |    |   |
| C |    |        |                           |                         |   |   |   |                             |        |      |    |   |
| D | NC | VSS    | VDD                       | NC                      |   |   |   | NC                          | VSS    | VDD  | NC | D |
| E |    | VSS    | VSSQ                      | DQ0                     |   |   |   | DM                          | VSSQ   | VDDQ |    | E |
| F |    | VDDQ   | DQ2                       | DQS                     |   |   |   | DQ1                         | DQ3    | VSSQ |    | F |
| G |    | VSSQ   | NC                        | $\overline{\text{DQS}}$ |   |   |   | VDD                         | VSS    | VSSQ |    | G |
| H |    | VREFDQ | VDDQ                      | NC                      |   |   |   | NC                          | NC     | VDDQ |    | H |
| J |    | NC     | VSS                       | $\overline{\text{RAS}}$ |   |   |   | CK                          | VSS    | NC   |    | J |
| K |    | ODT    | VDD                       | $\overline{\text{CAS}}$ |   |   |   | $\overline{\text{CK}}$      | VDD    | CKE  |    | K |
| L |    | NC     | $\overline{\text{CS}}$    | $\overline{\text{WE}}$  |   |   |   | A10/AP                      | ZQ     | NC   |    | L |
| M |    | VSS    | BA0                       | BA2                     |   |   |   | A15                         | VREFCA | VSS  |    | M |
| N |    | VDD    | A3                        | A0                      |   |   |   | A12/ $\overline{\text{BC}}$ | BA1    | VDD  |    | N |
| P |    | VSS    | A5                        | A2                      |   |   |   | A1                          | A4     | VSS  |    | P |
| R |    | VDD    | A7                        | A9                      |   |   |   | A11                         | A6     | VDD  |    | R |
| T | NC | VSS    | $\overline{\text{RESET}}$ | A13                     |   |   |   | NC                          | A8     | VSS  | NC | T |
| U |    |        |                           |                         |   |   |   |                             |        |      |    |   |
| V |    |        |                           |                         |   |   |   |                             |        |      |    |   |
| W | NC | NC     |                           | NC                      |   |   |   | NC                          |        | NC   | NC |   |

Note1: A1,A2,A4,A8,A10,A11,D1,D11,T1,T11,W1,W2,W4,W8,W10 and W11 balls indicate mechanical support balls with no internal connection

Ball Locations (x4)

- Populated ball
- + Ball not populated

Top view  
(See the balls through the Package)

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|----|----|
| A | ● | ● | + | ● | + | + | + | ● | + | ●  | ●  |
| B | + | + | + | + | + | + | + | + | + | +  | +  |
| C | + | + | + | + | + | + | + | + | + | +  | +  |
| D | ● | ● | ● | ● | + | + | + | ● | ● | ●  | ●  |
| E | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| F | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| G | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| H | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| J | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| K | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| L | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| M | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| N | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| P | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| R | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| T | ● | ● | ● | ● | + | + | + | ● | ● | ●  | ●  |
| U | + | + | + | + | + | + | + | + | + | +  | +  |
| V | + | + | + | + | + | + | + | + | + | +  | +  |
| W | ● | ● | + | ● | + | + | + | ● | + | ●  | ●  |

3.2 x8 Package Pinout (Top view) : 94ball FBGA Package(78balls + 16 balls of support balls)

|   |    |        |       |     |   |   |   |         |        |      |    |   |
|---|----|--------|-------|-----|---|---|---|---------|--------|------|----|---|
|   | 1  | 2      | 3     | 4   | 5 | 6 | 7 | 8       | 9      | 10   | 11 |   |
| A | NC | NC     |       | NC  |   |   |   | NC      |        | NC   | NC |   |
| B |    |        |       |     |   |   |   |         |        |      |    |   |
| C |    |        |       |     |   |   |   |         |        |      |    |   |
| D | NC | VSS    | VDD   | NC  |   |   |   | NU/TDQS | VSS    | VDD  | NC | D |
| E |    | VSS    | VSSQ  | DQ0 |   |   |   | DM/TDQS | VSSQ   | VDDQ |    | E |
| F |    | VDDQ   | DQ2   | DQS |   |   |   | DQ1     | DQ3    | VSSQ |    | F |
| G |    | VSSQ   | DQ6   | DQS |   |   |   | VDD     | VSS    | VSSQ |    | G |
| H |    | VREFDQ | VDDQ  | DQ4 |   |   |   | DQ7     | DQ5    | VDDQ |    | H |
| J |    | NC     | VSS   | RAS |   |   |   | CK      | VSS    | NC   |    | J |
| K |    | ODT    | VDD   | CAS |   |   |   | CK      | VDD    | CKE  |    | K |
| L |    | NC     | CS    | WE  |   |   |   | A10/AP  | ZQ     | NC   |    | L |
| M |    | VSS    | BA0   | BA2 |   |   |   | NC      | VREFCA | VSS  |    | M |
| N |    | VDD    | A3    | A0  |   |   |   | A12/BC  | BA1    | VDD  |    | N |
| P |    | VSS    | A5    | A2  |   |   |   | A1      | A4     | VSS  |    | P |
| R |    | VDD    | A7    | A9  |   |   |   | A11     | A6     | VDD  |    | R |
| T | NC | VSS    | RESET | A13 |   |   |   | NC      | A8     | VSS  | NC | T |
| U |    |        |       |     |   |   |   |         |        |      |    |   |
| V |    |        |       |     |   |   |   |         |        |      |    |   |
| W | NC | NC     |       | NC  |   |   |   | NC      |        | NC   | NC |   |

Note1: A1,A2,A4,A8,A10,A11,D1,D11,T1,T11,W1,W2,W4,W8,W10 and W11 balls indicate mechanical support balls with no internal connection

Ball Locations (x8)

- Populated ball
- + Ball not populated

Top view  
(See the balls through the Package)

|   |   |   |   |   |   |   |   |   |   |    |    |
|---|---|---|---|---|---|---|---|---|---|----|----|
|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| A | ● | ● | + | ● | + | + | + | ● | + | ●  | ●  |
| B | + | + | + | + | + | + | + | + | + | +  | +  |
| C | + | + | + | + | + | + | + | + | + | +  | +  |
| D | ● | ● | ● | ● | + | + | + | ● | ● | ●  | ●  |
| E | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| F | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| G | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| H | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| J | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| K | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| L | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| M | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| N | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| P | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| R | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| T | ● | ● | ● | ● | + | + | + | ● | ● | ●  | ●  |
| U | + | + | + | + | + | + | + | + | + | +  | +  |
| V | + | + | + | + | + | + | + | + | + | +  | +  |
| W | ● | ● | + | ● | + | + | + | ● | + | ●  | ●  |

3.3 x16 Package Pinout (Top view) : 112ball FBGA Package(96balls + 16 balls of support balls)

|    | 1  | 2      | 3     | 4    | 5 | 6 | 7 | 8      | 9      | 10   | 11 |   |
|----|----|--------|-------|------|---|---|---|--------|--------|------|----|---|
| A  | NC | NC     |       | NC   |   |   |   | NC     |        | NC   | NC |   |
| B  |    |        |       |      |   |   |   |        |        |      |    |   |
| C  |    |        |       |      |   |   |   |        |        |      |    |   |
| D  | NC | VDDQ   | DQU5  | DQU7 |   |   |   | DQU4   | VDDQ   | VSS  | NC | D |
| E  |    | VSSQ   | VDD   | VSS  |   |   |   | DQSU   | DQU6   | VSSQ |    | E |
| F  |    | VDDQ   | DQU3  | DQU1 |   |   |   | DQSU   | DQU2   | VDDQ |    | F |
| G  |    | VSSQ   | VDDQ  | DMU  |   |   |   | DQU0   | VSSQ   | VDD  |    | G |
| H  |    | VSS    | VSSQ  | DQL0 |   |   |   | DML    | VSSQ   | VDDQ |    | H |
| J  |    | VDDQ   | DQL2  | DQSL |   |   |   | DQL1   | DQL3   | VSSQ |    | J |
| K  |    | VSSQ   | DQL6  | DQSL |   |   |   | VDD    | VSS    | VSSQ |    | K |
| L  |    | VREFDQ | VDDQ  | DQL4 |   |   |   | DQL7   | DQL5   | VDDQ |    | L |
| M  |    | NC     | VSS   | RAS  |   |   |   | CK     | VSS    | NC   |    | M |
| N  |    | ODT    | VDD   | CAS  |   |   |   | CK     | VDD    | CKE  |    | N |
| P  |    | NC     | CS    | WE   |   |   |   | A10/AP | ZQ     | NC   |    | P |
| R  |    | VSS    | BA0   | BA2  |   |   |   | A15    | VREFCA | VSS  |    | R |
| T  |    | VDD    | A3    | A0   |   |   |   | A12/BC | BA1    | VDD  |    | T |
| U  |    | VSS    | A5    | A2   |   |   |   | A1     | A4     | VSS  |    | U |
| V  |    | VDD    | A7    | A9   |   |   |   | A11    | A6     | VDD  |    | V |
| W  | NC | VSS    | RESET | A13  |   |   |   | NC     | A8     | VSS  | NC | W |
| Y  |    |        |       |      |   |   |   |        |        |      |    |   |
| AA |    |        |       |      |   |   |   |        |        |      |    |   |
| AB | NC | NC     |       | NC   |   |   |   | NC     |        | NC   | NC |   |

Note1: A1,A2,A4,A8,A10,A11,D1,D11,W1,W11,AB1,AB2,AB4,AB8,AB10 and AB11 balls indicate mechanical support balls with no internal connection

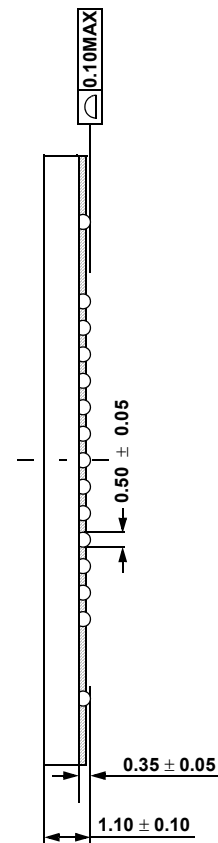
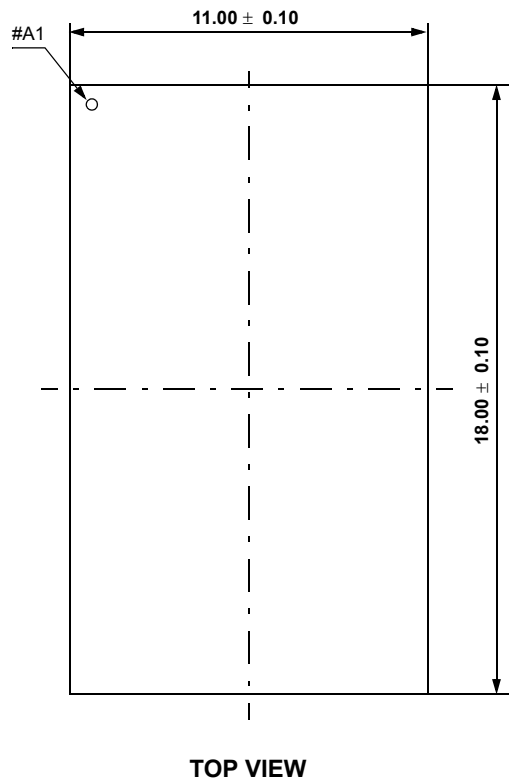
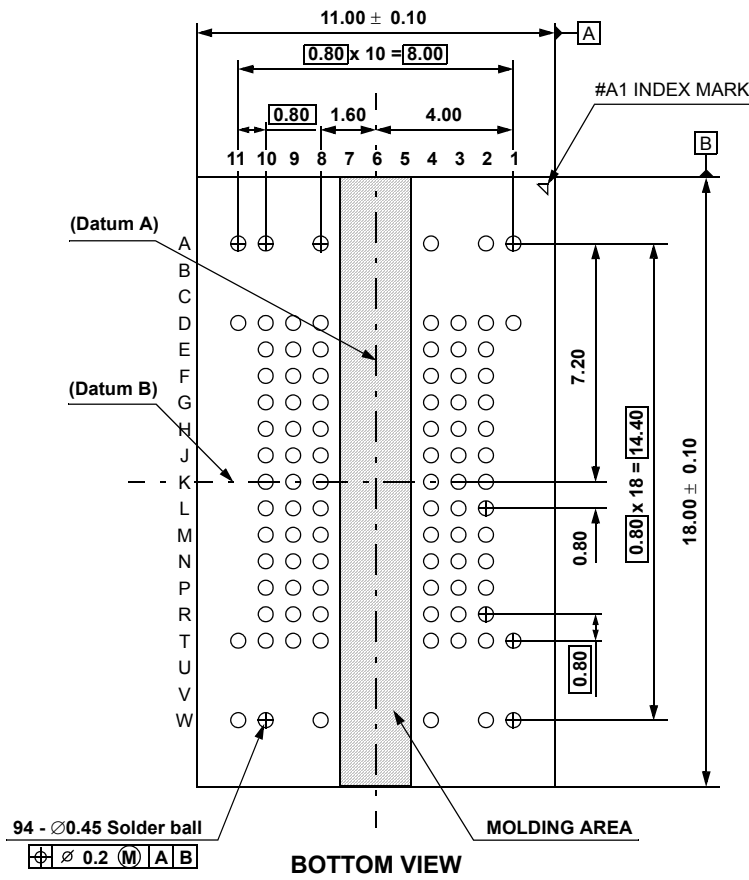
Ball Locations (x16)

- Populated ball
- + Ball not populated

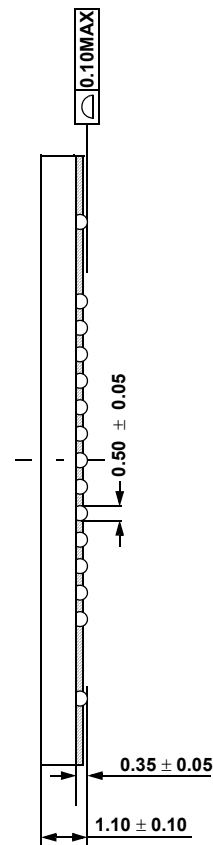
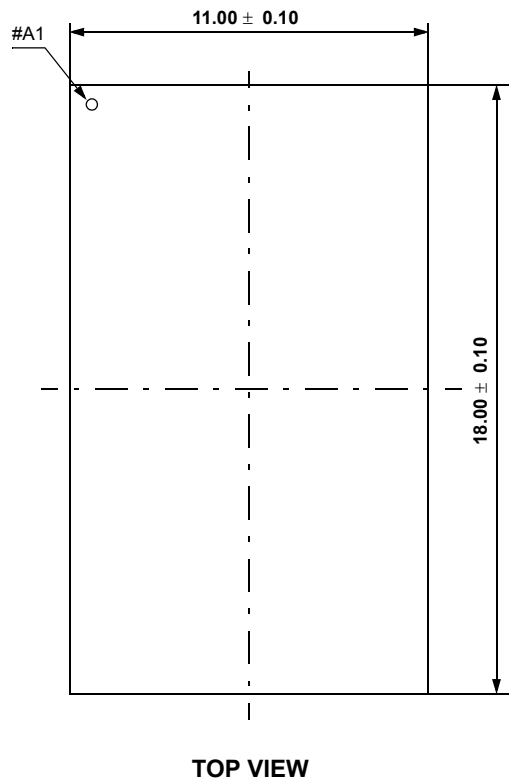
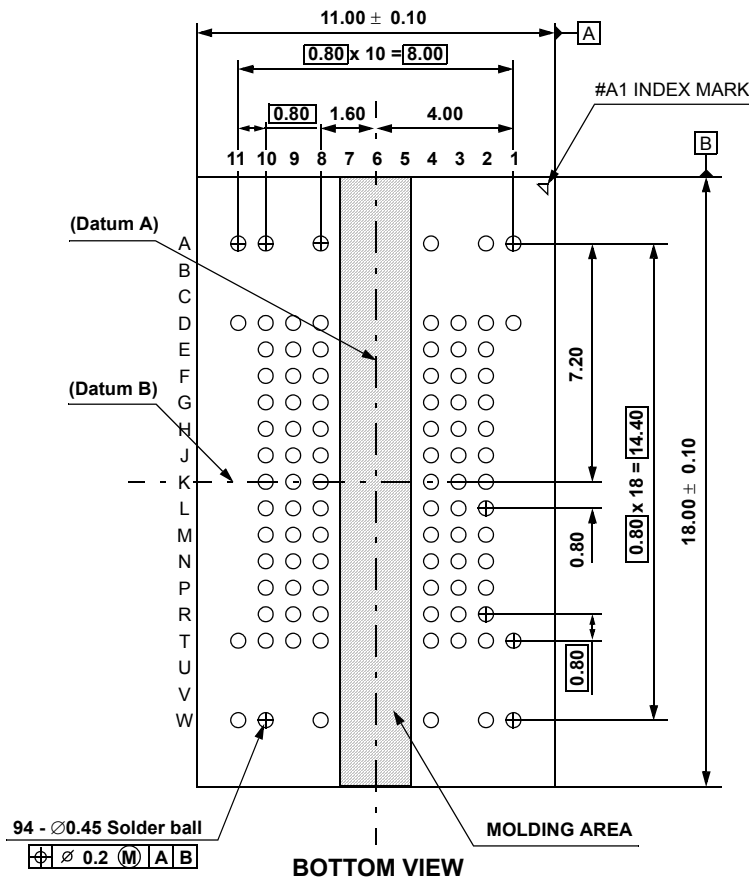
Top view  
(See the balls through the Package)

|    | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|----|---|---|---|---|---|---|---|---|---|----|----|
| A  | ● | ● | + | ● | + | + | + | ● | + | ●  | ●  |
| B  | + | + | + | + | + | + | + | + | + | +  | +  |
| C  | + | + | + | + | + | + | + | + | + | +  | +  |
| D  | ● | ● | ● | + | + | + | ● | ● | ● | ●  | ●  |
| E  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| F  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| G  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| H  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| J  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| K  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| L  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| M  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| N  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| P  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| R  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| T  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| U  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| V  | + | ● | ● | ● | + | + | + | ● | ● | ●  | +  |
| W  | ● | ● | ● | ● | + | + | + | ● | ● | ●  | ●  |
| Y  | + | + | + | + | + | + | + | + | + | +  | +  |
| AA | + | + | + | + | + | + | + | + | + | +  | +  |
| AB | ● | ● | + | ● | + | + | + | ● | + | ●  | ●  |

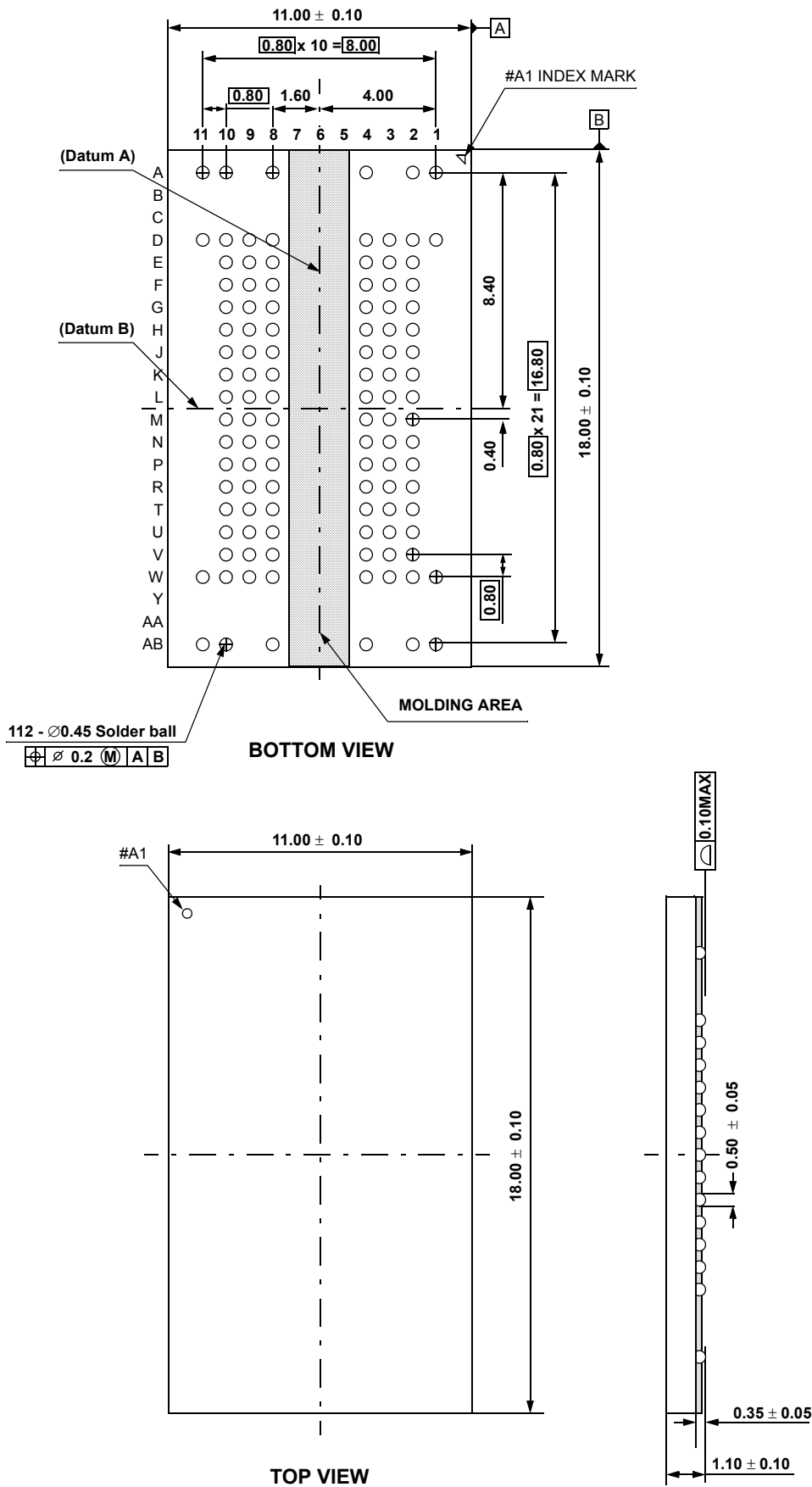
3.4 FBGA Package Dimension (x4)



3.5 FBGA Package Dimension (x8)



3.6 FBGA Package Dimension (x16)



## 4.0 Input/Output Functional Description

[ Table 3 ] Input/Output function description

| Symbol  | Type         | Function  |
|---|--------------|---|
| CK, $\overline{CK}$                                   | Input        | <b>Clock:</b> CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$ . Output (read) data is referenced to the crossings of CK and $\overline{CK}$   |
| CKE   | Input        | <b>Clock Enable:</b> CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self -Refresh. |
| $\overline{CS}$                                       | Input        | <b>Chip Select:</b> All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.   |
| ODT   | Input        | <b>On Die Termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS and DM/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.  |
| $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ | Input        | <b>Command Inputs:</b> $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$ ) define the command being entered.  |
| DM<br>(DMU), (DML)                                    | Input        | <b>Input Data Mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/ $\overline{TDQS}$ is enabled by Mode Register A11 setting in MR1.   |
| BA0 - BA2   | Input        | <b>Bank Address Inputs:</b> BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.  |
| A0 - A12  | Input        | <b>Address Inputs:</b> Provided the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/ $\overline{BC}$ have additional functions, see below)<br>The address inputs also provide the op-code during Mode Register Set commands.  |
| A10 / AP  | Input        | <b>Autoprecharge:</b> A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge)<br>A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.  |
| A12 / $\overline{BC}$                                 | Input        | <b>Burst Chop:</b> A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be performed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details   |
| $\overline{RESET}$                                    | Input        | <b>Active Low Asynchronous Reset:</b> Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.  |
| DQ  | Input/Output | <b>Data Input/ Output:</b> Bi-directional data bus.   |
| DQS, ( $\overline{DQS}$ )                             | Input/Output | <b>Data Strobe:</b> output with read data, input with write data. Edge-aligned with read data, centered in write data.  |
| TDQS, ( $\overline{TDQS}$ )                           | Output       | <b>Termination Data Strobe:</b> TDQS/ $\overline{TDQS}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/ $\overline{TDQS}$ that is applied to DQS/DQS. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and TDQS is not used.  |
| NC  |              | <b>No Connect:</b> No internal electrical connection is present.  |
| V <sub>DDQ</sub>                                      | Supply       | <b>DQ Power Supply:</b> 1.5V +/- 0.075V   |
| V <sub>SSQ</sub>                                      | Supply       | <b>DQ Ground</b>  |
| V <sub>DD</sub>                                       | Supply       | <b>Power Supply:</b> 1.5V +/- 0.075V  |
| V <sub>SS</sub>                                       | Supply       | <b>Ground</b>   |
| V <sub>REFDQ</sub>                                    | Supply       | <b>Reference voltage for DQ</b>   |
| V <sub>REFCA</sub>                                    | Supply       | <b>Reference voltage for CA</b>   |
| ZQ  | Supply       | <b>Reference Pin for ZQ calibration</b>   |

Note : Input only pins (BA0-BA2, A0-A12,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{CS}$ , CKE, ODT and  $\overline{RESET}$ ) do not supply termination.

## 5.0 DDR3 SDRAM Addressing

## 512Mb

| Configuration        | 128Mb x4   | 64Mb x 8                         | 32Mb x16                         |
|----------------------|--|----------------------------------|----------------------------------|
| # of Bank            | 8  | 8                                | 8                                |
| Bank Address         | BA0 - BA2  | BA0 - BA2                        | BA0 - BA2                        |
| Auto precharge       | A <sub>10</sub> /AP                              | A <sub>10</sub> /AP              | A <sub>10</sub> /AP              |
| Row Address          | A <sub>0</sub> - A <sub>12</sub>                 | A <sub>0</sub> - A <sub>12</sub> | A <sub>0</sub> - A <sub>11</sub> |
| Column Address       | A <sub>0</sub> - A <sub>9</sub> ,A <sub>11</sub> | A <sub>0</sub> - A <sub>9</sub>  | A <sub>0</sub> - A <sub>9</sub>  |
| BC switch on the fly | A <sub>12</sub> /BC                              | A <sub>12</sub> /BC              | A <sub>12</sub> /BC              |
| Page size *1         | 1 KB   | 1 KB                             | 2 KB                             |

\* Reference Information : The following tables are address mapping information for other densities

## 1Gb

| Configuration        | 256Mb x4   | 128Mb x 8                        | 64Mb x16                         |
|----------------------|--|----------------------------------|----------------------------------|
| # of Bank            | 8  | 8                                | 8                                |
| Bank Address         | BA0 - BA2  | BA0 - BA2                        | BA0 - BA2                        |
| Auto precharge       | A <sub>10</sub> /AP                              | A <sub>10</sub> /AP              | A <sub>10</sub> /AP              |
| Row Address          | A <sub>0</sub> - A <sub>13</sub>                 | A <sub>0</sub> - A <sub>13</sub> | A <sub>0</sub> - A <sub>12</sub> |
| Column Address       | A <sub>0</sub> - A <sub>9</sub> ,A <sub>11</sub> | A <sub>0</sub> - A <sub>9</sub>  | A <sub>0</sub> - A <sub>9</sub>  |
| BC switch on the fly | A <sub>12</sub> /BC                              | A <sub>12</sub> /BC              | A <sub>12</sub> /BC              |
| Page size *1         | 1 KB   | 1 KB                             | 2 KB                             |

## 2Gb

| Configuration        | 512Mb x4   | 256Mb x 8                         | 128Mb x16                         |
|----------------------|--|-----------------------------------|-----------------------------------|
| # of Bank            | 8  | 8                                 | 8                                 |
| Bank Address         | BA <sub>0</sub> - BA <sub>2</sub>                | BA <sub>0</sub> - BA <sub>2</sub> | BA <sub>0</sub> - BA <sub>2</sub> |
| Auto precharge       | A <sub>10</sub> /AP                              | A <sub>10</sub> /AP               | A <sub>10</sub> /AP               |
| Row Address          | A <sub>0</sub> - A <sub>14</sub>                 | A <sub>0</sub> - A <sub>14</sub>  | A <sub>0</sub> - A <sub>13</sub>  |
| Column Address       | A <sub>0</sub> - A <sub>9</sub> ,A <sub>11</sub> | A <sub>0</sub> - A <sub>9</sub>   | A <sub>0</sub> - A <sub>9</sub>   |
| BC switch on the fly | A <sub>12</sub> /BC                              | A <sub>12</sub> /BC               | A <sub>12</sub> /BC               |
| Page size            | 1 KB   | 1 KB                              | 2 KB                              |

## 4Gb

| Configuration        | 1Gb x4   | 512Mb x 8                         | 256Mb x16                         |
|----------------------|--|-----------------------------------|-----------------------------------|
| # of Bank            | 8  | 8                                 | 8                                 |
| Bank Address         | BA <sub>0</sub> - BA <sub>2</sub>                | BA <sub>0</sub> - BA <sub>2</sub> | BA <sub>0</sub> - BA <sub>2</sub> |
| Auto precharge       | A <sub>10</sub> /AP                              | A <sub>10</sub> /AP               | A <sub>10</sub> /AP               |
| Row Address          | A <sub>0</sub> - A <sub>15</sub>                 | A <sub>0</sub> - A <sub>15</sub>  | A <sub>0</sub> - A <sub>14</sub>  |
| Column Address       | A <sub>0</sub> - A <sub>9</sub> ,A <sub>11</sub> | A <sub>0</sub> - A <sub>9</sub>   | A <sub>0</sub> - A <sub>9</sub>   |
| BC switch on the fly | A <sub>12</sub> /BC                              | A <sub>12</sub> /BC               | A <sub>12</sub> /BC               |
| Page size            | 1 KB   | 1 KB                              | 2 KB                              |

## 8Gb

| Configuration        | 2Gb x4               | 1Gb x 8              | 512Mb x16            |
|----------------------|----------------------|----------------------|----------------------|
| # of Bank            | 8                    | 8                    | 8                    |
| Bank Address         | BA0 - BA2            | BA0 - BA2            | BA0 - BA2            |
| Auto precharge       | A10/AP               | A10/AP               | A10/AP               |
| Row Address          | A0 - A15             | A0 - A15             | A0 - A15             |
| Column Address       | A0 - A9,A11,A13      | A0 - A9,A11          | A0 - A9              |
| BC switch on the fly | A12/ $\overline{BC}$ | A12/ $\overline{BC}$ | A12/ $\overline{BC}$ |
| Page size            | 2 KB                 | 2 KB                 | 2 KB                 |

Note 1 : Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.

Page size is per bank, calculated as follows:  $\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \approx 8$

where, COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

## 6.0 Absolute Maximum Ratings

### 6.1 Absolute Maximum DC Ratings

| Symbol                             | Parameter                           | Rating           | Units | Notes |
|------------------------------------|-------------------------------------|------------------|-------|-------|
| VDD                                | Voltage on VDD pin relative to Vss  | -0.4 V ~ 1.975 V | V     | 1,3   |
| VDDQ                               | Voltage on VDDQ pin relative to Vss | -0.4 V ~ 1.975 V | V     | 1,3   |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage on any pin relative to Vss  | -0.4 V ~ 1.975 V | V     | 1     |
| T <sub>STG</sub>                   | Storage Temperature                 | -55 to +100      | °C    |       |

[ Table 4 ] Absolute Maximum DC Ratings

Note :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6xVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

### 6.2 DRAM Component Operating Temperature Range

| Symbol            | Parameter                             | rating   | Unit | Notes |
|-------------------|---------------------------------------|----------|------|-------|
| T <sub>OPER</sub> | Normal Operating Temperature Range    | 0 to 85  | °C   | 1,2   |
|                   | Extended Temperature Range (Optional) | 85 to 95 | °C   | 1,3   |

[ Table 5 ] Temperature Range

Note :

- Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
- Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

## 7.0 AC & DC Operating Conditions

### 7.1 Recommended DC operating Conditions (SSTL\_1.5)

| Symbol | Parameter                 | Rating |      |       | Units | Notes |
|--------|---------------------------|--------|------|-------|-------|-------|
|        |                           | Min.   | Typ. | Max.  |       |       |
| VDD    | Supply Voltage            | 1.425  | 1.5  | 1.575 | V     | 1,2   |
| VDDQ   | Supply Voltage for Output | 1.425  | 1.5  | 1.575 | V     | 1,2   |

[ Table 6 ] Recommended DC Operating Conditions

Note :

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

## 8.0 AC & DC Input Measurement Levels

### 8.1 AC and DC Logic input levels for single-ended signals

| Symbol          | Parameter                      | DDR3-800/1066/1333   |                      | Unit | Notes |
|-----------------|--------------------------------|----------------------|----------------------|------|-------|
|                 |                                | Min.                 | Max.                 |      |       |
| $V_{IH}(DC)$    | dc input logic high            | $V_{REF} + 100$      | VDD                  | mV   | 1     |
| $V_{IL}(DC)$    | dc input logic low             | VSS                  | $V_{REF} - 100$      | mV   | 1     |
| $V_{IH}(AC)$    | ac input logic high            | $V_{REF} + 175$      | -                    | mV   | 1,2   |
| $V_{IL}(AC)$    | ac input logic low             | -                    | $V_{REF} - 175$      | mV   | 1,2   |
| $V_{REFDQ}(DC)$ | I/O Reference Voltage(DQ)      | $0.49 \cdot V_{DDQ}$ | $0.51 \cdot V_{DDQ}$ | V    | 3,4   |
| $V_{REFCA}(DC)$ | I/O Reference Voltage(CMD/ADD) | $0.49 \cdot V_{DDQ}$ | $0.51 \cdot V_{DDQ}$ | V    | 3,4   |

[ Table 7 ] Single Ended AC and DC input levels

Note :

1. For DQ and DM,  $V_{REF} = V_{REFDQ}$ . For input only pins except RESET, or  $V_{REF} = V_{REFCA}$
2. See 9.6 "Overshoot and Undershoot specifications" on page 23.
3. The ac peak noise on  $V_{REF}$  may not allow  $V_{REF}$  to deviate from  $V_{REF(DC)}$  by more than  $\pm 1\%$  VDD (for reference : approx.  $\pm 15mV$ )
4. For reference : approx.  $V_{DD}/2 \pm 15mV$

The dc-tolerance limits and ac-noise limits for the reference voltages  $V_{REFCA}$  and  $V_{REFDQ}$  are illustrate in Figure 1. It shows a valid reference voltage  $V_{REF}(t)$  as a function of time. ( $V_{REF}$  stands for  $V_{REFCA}$  and  $V_{REFDQ}$  likewise).

$V_{REF}(DC)$  is the linear average of  $V_{REF}(t)$  over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in above table. Furthermore  $V_{REF}(t)$  may temporarily deviate from  $V_{REF}(DC)$  by no more than  $\pm 1\%$  VDD.

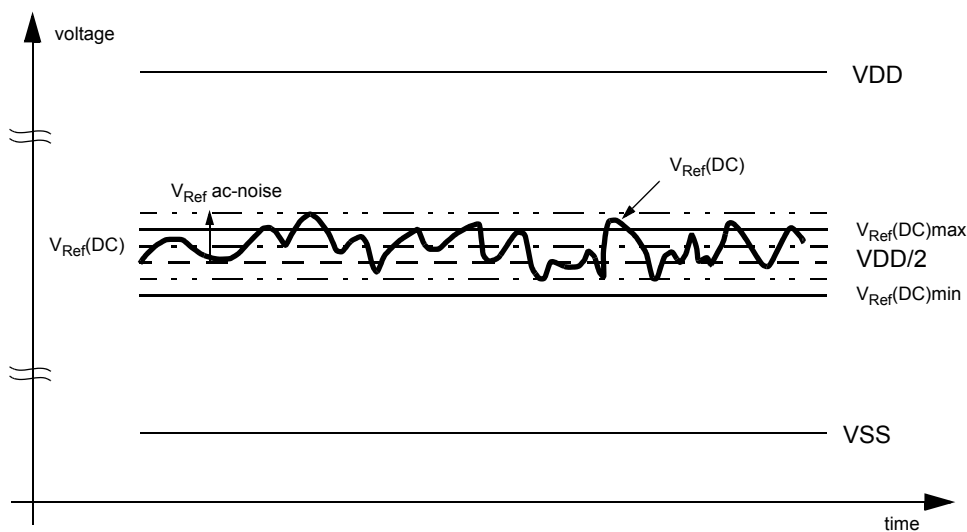


Figure 1. Illustration of  $V_{REF}(DC)$  tolerance and  $V_{REF}$  ac-noise limits

The voltage levels for setup and hold time measurements  $V_{IH}(AC)$ ,  $V_{IH}(DC)$ ,  $V_{IL}(AC)$  and  $V_{IL}(DC)$  are dependent on  $V_{REF}$ .

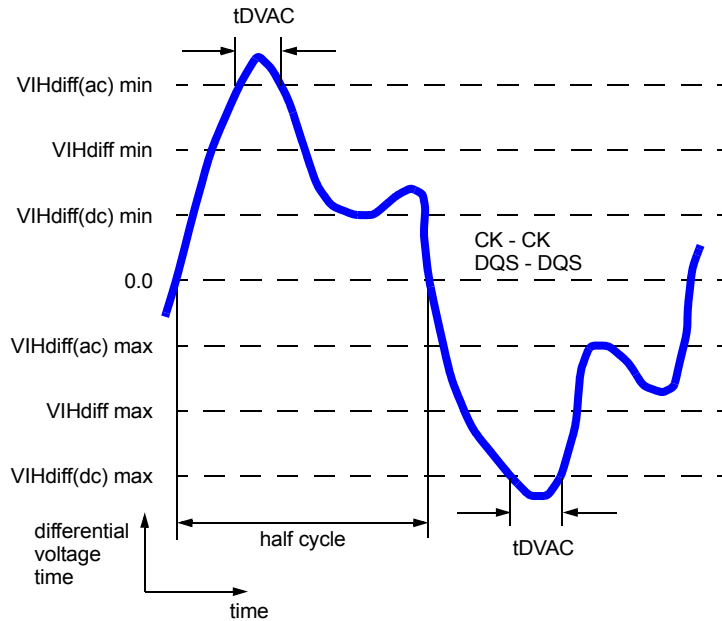
" $V_{REF}$ " shall be understood as  $V_{REF}(DC)$ , as defined in Figure 1.

This clarifies, that dc-variations of  $V_{REF}$  affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for  $V_{REF}(DC)$  deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with  $V_{REF}$  ac-noise. Timing and voltage effects due to ac-noise on  $V_{REF}$  up to the specified limit ( $\pm 1\%$  of VDD) are included in DRAM timings and their associated deratings.

8.2 Differential swing requirement for differential signals

Figure 2 : Definition of differential ac-swing and "time above ac level tDVAC



[ Table 8 ] Differential swing requirement for clock (CK -  $\overline{CK}$ ) and strobe (DQS -  $\overline{DQS}$ )

| Symbol      | Parameter                  | DDR3-800 & 1066 & 1033 & 1600 |                      | unit | Note |
|-------------|----------------------------|-------------------------------|----------------------|------|------|
|             |                            | min                           | max                  |      |      |
| VIHdiff     | differential input high    | +0.2                          | note 3               | V    | 1    |
| VILdiff     | differential input low     | note 3                        | -0.2                 | V    | 1    |
| VIHdiff(ac) | differential input high ac | 2 x (VIH(ac)-Vref)            | note 3               | V    | 2    |
| VIHdiff(ac) | differential input low ac  | note 3                        | 2 x (Vref - VIL(ac)) | V    | 2    |

Notes:

- used to define a differential signal slew-rate.
- for CK -  $\overline{CK}$  use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS -  $\overline{DQS}$ , DQSL -  $\overline{DQSL}$ , DQSU -  $\overline{DQSU}$  use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- these values are not defined, however they single-ended signals CK,  $\overline{CK}$ , DQS,  $\overline{DQS}$ , DQSL,  $\overline{DQSL}$ , DQSU,  $\overline{DQSU}$  need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

[ Table 9 ] Allowed time before ringback (tDVAC) for CLK -  $\overline{CLK}$  and DQS -  $\overline{DQS}$ .

| Slew Rate [V/ns] | tDVAC [ps] @  VIH/Ldiff(ac)  = 350mV |     | tDVAC [ps] @  VIH/Ldiff(ac)  = 300mV |     |
|------------------|--------------------------------------|-----|--------------------------------------|-----|
|                  | min                                  | max | min                                  | max |
| > 4.0            | 75                                   | -   | 175                                  | -   |
| 4.0              | 57                                   | -   | 170                                  | -   |
| 3.0              | 50                                   | -   | 167                                  | -   |
| 2.0              | 38                                   | -   | 163                                  | -   |
| 1.8              | 34                                   | -   | 162                                  | -   |
| 1.6              | 29                                   | -   | 161                                  | -   |
| 1.4              | 22                                   | -   | 159                                  | -   |
| 1.2              | 13                                   | -   | 155                                  | -   |
| 1.0              | 0                                    | -   | 150                                  | -   |
| < 1.0            | 0                                    | -   | 150                                  | -   |

### 8.2.1 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU,  $\overline{\text{CK}}$ ,  $\overline{\text{DQS}}$ ,  $\overline{\text{DQSL}}$ , or  $\overline{\text{DQSU}}$ ) has also to comply with certain requirements for single-ended signals.

CK and  $\overline{\text{CK}}$  have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (  $V_{IH}(ac)$  /  $V_{IL}(ac)$  ) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU,  $\overline{\text{DQS}}$ ,  $\overline{\text{DQSL}}$  have to reach VSEHmin / VSELmax (approximately the ac-levels (  $V_{IH}(ac)$  /  $V_{IL}(ac)$  ) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if  $V_{IH150}(ac)/V_{IL150}(ac)$  is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and  $\overline{\text{CK}}$

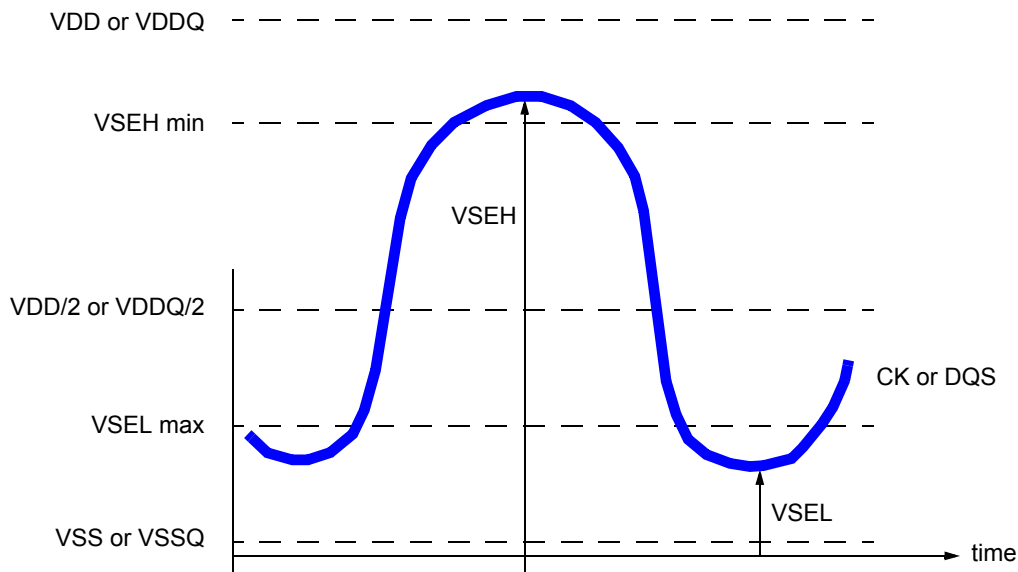


Figure 3: Single-ended requirement for differential signals.

Note that while ADD/CMD and DQ signal requirements are with respect to  $V_{ref}$ , the single-ended components of differential signals have a requirement with respect to  $V_{DD}/2$ ; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

8.3 AC and DC logic input levels for Differential Signals

[ Table 10 ] Differential DC and AC input levels

| Symbol              | Parameter                     | DDR3-800/1066/1333 |       | Unit | Notes |
|---------------------|-------------------------------|--------------------|-------|------|-------|
|                     |                               | Min                | Max   |      |       |
| V <sub>IHdiff</sub> | Differential input logic high | + 200              | -     | mV   | 1     |
| V <sub>ILdiff</sub> | Differential input logic low  | -                  | - 200 |      |       |

Note :

1. Refer to "Overshoot and Undershoot specifications" on page 23.

8.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK,  $\overline{CK}$  and DQS,  $\overline{DQS}$ ) must meet the requirements in below table. The differential input cross point voltage V<sub>IX</sub> is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.

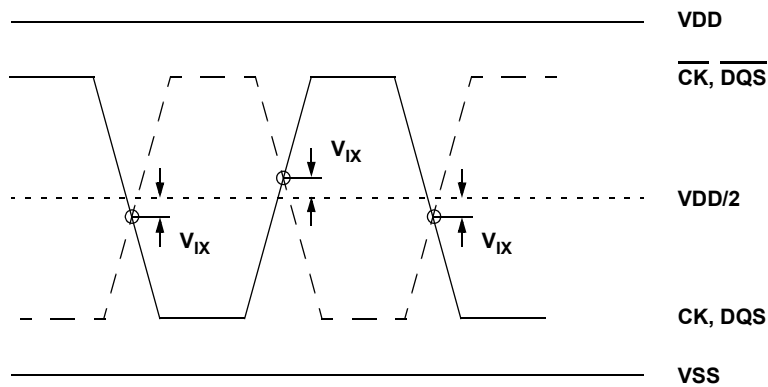


Figure 4. Vix Definition

[ Table 11 ] Cross point voltage for differential input signals (CK, DQS)

| Symbol          | Parameter  | DDR3-800/1066/1333/1600 |     | Unit | Notes |
|-----------------|--|-------------------------|-----|------|-------|
|                 |  | Min                     | Max |      |       |
| V <sub>IX</sub> | Differential input Cross point voltage relative to VDD/2 | -150                    | 150 | mV   |       |

8.5 Slew rate definition for Single Ended Input Signals

8.5.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vref and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vref and the first crossing of VIL(AC)max.

8.5.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of Vref. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of Vref

| Description                      | Measured   |            | Defined by                             | Applicable for   |
|----------------------------------|------------|------------|--|------------------|
|                                  | From       | To         |  |                  |
| Input slew rate for rising edge  | Vref       | VIH(AC)min | $\frac{VIH(AC)min - Vref}{\Delta TRS}$ | Setup (tIS, tDS) |
| Input slew rate for falling edge | Vref       | VIL(AC)max | $\frac{Vref - VIL(AC)max}{\Delta TFS}$ |                  |
| Input slew rate for rising edge  | VIL(DC)max | Vref       | $\frac{Vref - VIL(DC)max}{\Delta TFH}$ | Hold (tIH, tDH)  |
| Input slew rate for falling edge | VIH(DC)min | Vref       | $\frac{VIH(DC)min - Vref}{\Delta TRH}$ |                  |

[ Table 12 ] Single Ended Input Slew Rate definition

Notes: This nominal slew rate applies for linear signal waveforms.

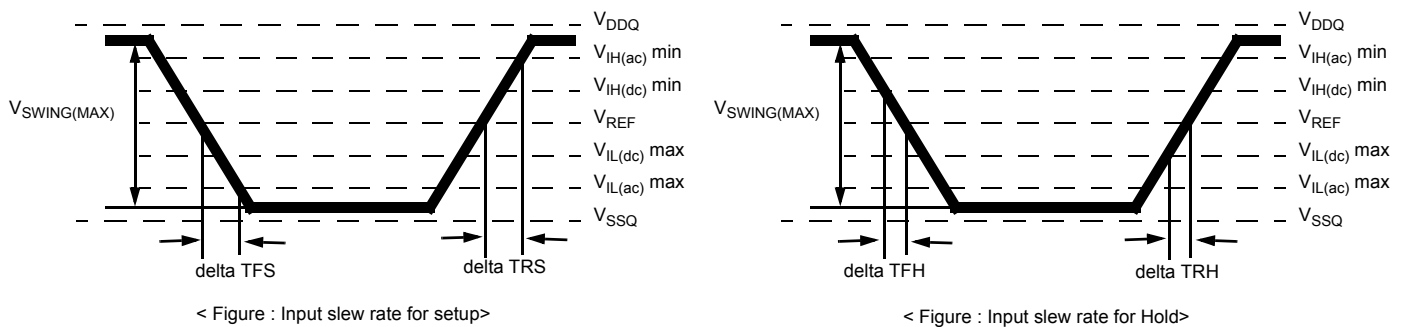


Figure 5. Input Nominal Slew Rate definition for Single ended Signals

8.6 Slew rate definition for Differential Input Signals

| Description   | Measured   |            | Defined by                                      |
|---|------------|------------|---|
|   | From       | To         |   |
| Differential input slew rate for rising edge (CK-CK and DQS-DQS)  | VILdiffmax | VIHdiffmin | $\frac{VIHdiffmin - VILdiffmax}{\Delta TRdiff}$ |
| Differential input slew rate for falling edge (CK-CK and DQS-DQS) | VIHdiffmin | VILdiffmax | $\frac{VIHdiffmin - VILdiffmax}{\Delta TFdiff}$ |

[ Table 13 ] Differential input slew rate definition

Note : The differential signal (i.e. CK - CK and DQS - DQS) must be linear between these thresholds

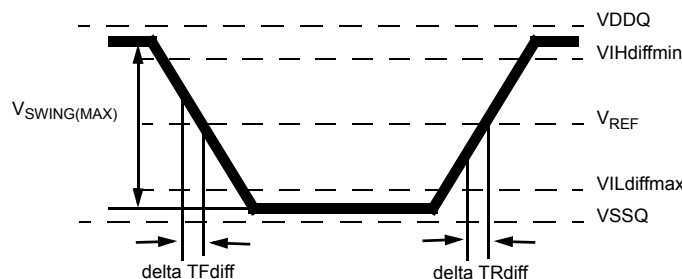


Figure 6. Differential Input Slew Rate definition for DQS, DQS and CK, CK

## 9.0 AC and DC Output Measurement Levels

### 9.1 Single Ended AC and DC Output Levels

[ Table 14 ] Single Ended AC and DC output levels

| Symbol       | Parameter   | DDR3-800/1066/1333/1600 | Units | Notes |
|--------------|---|-------------------------|-------|-------|
| $V_{OH(DC)}$ | DC output high measurement level (for IV curve linearity) | $0.8 \times VDDQ$       | V     |       |
| $V_{OM(DC)}$ | DC output mid measurement level (for IV curve linearity)  | $0.5 \times VDDQ$       | V     |       |
| $V_{OL(DC)}$ | DC output low measurement level (for IV curve linearity)  | $0.2 \times VDDQ$       | V     |       |
| $V_{OH(AC)}$ | AC output high measurement level (for output SR)          | $VTT + 0.1 \times VDDQ$ | V     | 1     |
| $V_{OL(AC)}$ | AC output low measurement level (for output SR)           | $VTT - 0.1 \times VDDQ$ | V     | 1     |

Note :

1. The swing of  $\pm 0.1 \times VDDQ$  is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 34ohms and an effective test load of 25ohms to  $VTT = VDDQ/2$ .

### 9.2 Differential AC and DC Output Levels

| Symbol           | Parameter   | DDR3-800/1066/1333/1600 | Units | Notes |
|------------------|---|-------------------------|-------|-------|
| $V_{OHdiff(AC)}$ | AC differential output high measurement level (for output SR) | $+0.2 \times VDDQ$      | V     | 1     |
| $V_{OLdiff(DC)}$ | AC differential output low measurement level (for output SR)  | $-0.2 \times VDDQ$      | V     | 1     |

[ Table 15 ] Differential AC and DC output levels

Note :

1. The swing of  $\pm 0.2 \times VDDQ$  is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 34ohms and an effective test load of 25ohms to  $VTT = VDDQ/2$  at each of the differential outputs

9.3. Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table 16 and figure 7.

[ Table 16 ] Single Ended Output slew rate definition

| Description                                    | Measured |         | Defined by                            |
|--|----------|---------|---------------------------------------|
|  | From     | To      |                                       |
| Single ended output slew rate for rising edge  | VOL(AC)  | VOH(AC) | $\frac{VOH(AC)-VOL(AC)}{\Delta TRse}$ |
| Single ended output slew rate for falling edge | VOH(AC)  | VOL(AC) | $\frac{VOH(AC)-VOL(AC)}{\Delta TFse}$ |

| Parameter                     | Symbol | DDR3-800 |     | DDR3-1066 |     | DDR3-1333 |     | DDR3-1600 |     | Units |
|-------------------------------|--------|----------|-----|-----------|-----|-----------|-----|-----------|-----|-------|
|                               |        | Min      | Max | Min       | Max | Min       | Max | Min       | Max |       |
| Single ended output slew rate | SRQse  | 2.5      | 5   | 2.5       | 5   | 2.5       | 5   | TBD       | 5   | V/ns  |

[ Table 17 ] Single Ended Output slew rate

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.

For Ron=RZQ/7 setting

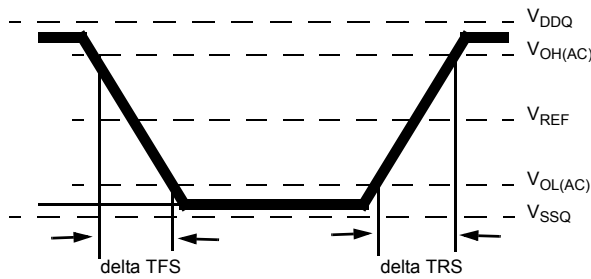


Figure 7. Single Ended Output Slew Rate definition

9.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 18 and figure 8.

[ Table 18 ] Differential Output slew rate definition

| Description                                    | Measured    |             | Defined by                                      |
|--|-------------|-------------|---|
|  | From        | To          |   |
| Differential output slew rate for rising edge  | VOLdiff(AC) | VOHdiff(AC) | $\frac{VOHdiff(AC)-VOLdiff(AC)}{\Delta TRdiff}$ |
| Differential output slew rate for falling edge | VOHdiff(AC) | VOLdiff(AC) | $\frac{VOHdiff(AC)-VOLdiff(AC)}{\Delta TFdiff}$ |

| Parameter                     | Symbol | DDR3-800 |     | DDR3-1066 |     | DDR3-1333 |     | DDR3-1600 |     | Units |
|-------------------------------|--------|----------|-----|-----------|-----|-----------|-----|-----------|-----|-------|
|                               |        | Min      | Max | Min       | Max | Min       | Max | Min       | Max |       |
| Single ended output slew rate | SRQse  | 5        | 10  | 5         | 10  | 5         | 10  | TBD       | 10  | V/ns  |

[ Table 19 ] Differential Output slew rate

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.

For Ron=RZQ/7 setting

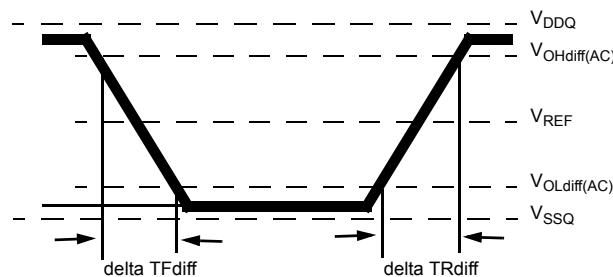


Figure 8. Differential Output Slew Rate definition

### 9.5 Reference Load for AC Timing and Output Slew Rate

Figure 9 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

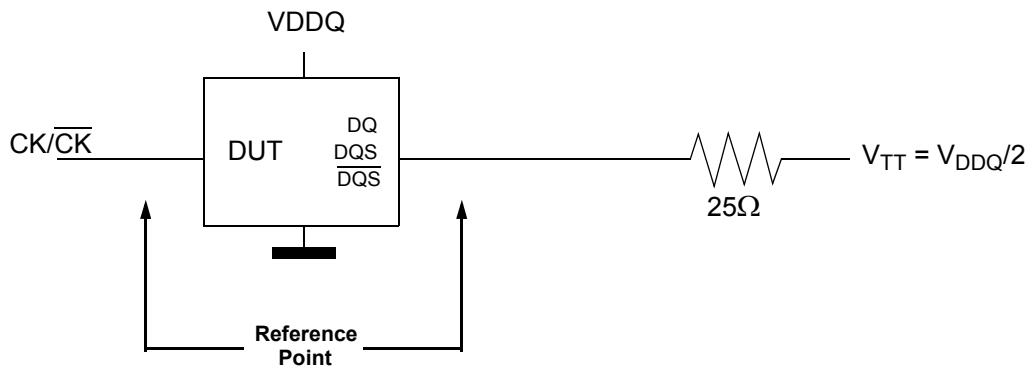


Figure 9. Reference Load for AC Timing and Output Slew Rate

9.6 Overshoot/Undershoot Specification

9.6.1 Address and Control Overshoot and Undershoot specifications

AC Overshoot/Undershoot Specification for Address and Control Pins

(A0-A12, BA0-BA2,  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , CKE, ODT)

| Parameter   | Specification |           |           |           |
|---|---------------|-----------|-----------|-----------|
|   | DDR3-800      | DDR3-1066 | DDR3-1333 | DDR3-1600 |
| Maximum peak amplitude allowed for overshoot area (See Figure 8)  | 0.4V          | 0.4V      | 0.4V      | 0.4V      |
| Maximum peak amplitude allowed for undershoot area (See Figure 8) | 0.4V          | 0.4V      | 0.4V      | 0.4V      |
| Maximum overshoot area above VDD (See Figure 8)                   | 0.67V-ns      | 0.5V-ns   | 0.4V-ns   | 0.33V-ns  |
| Maximum undershoot area below VSS (See Figure 8)                  | 0.67V-ns      | 0.5V-ns   | 0.4V-ns   | 0.33V-ns  |

[ Table 20 ] AC overshoot/undershoot specification for Address and Control pins

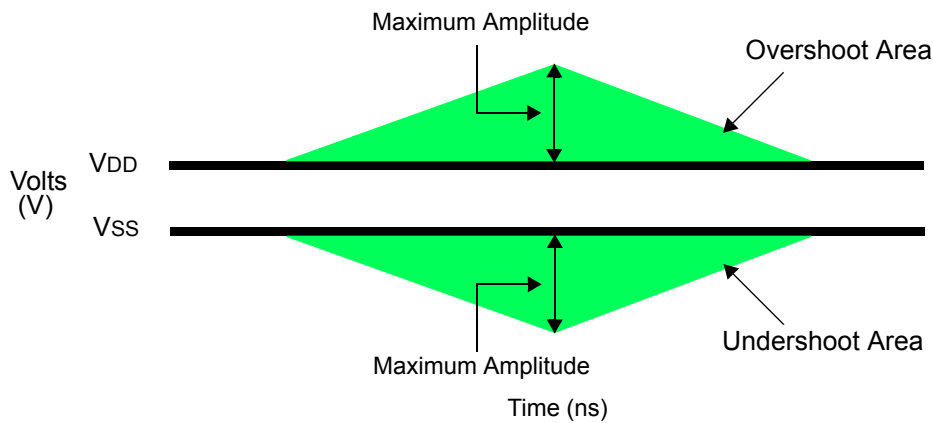


Figure 10. Address and Control Overshoot and Undershoot definition

9.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot specifications

AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask Pins

(DQ, DQS,  $\overline{DQS}$ , DM, CK,  $\overline{CK}$ )

| Parameter   | Specification |           |           |           |
|---|---------------|-----------|-----------|-----------|
|   | DDR3-800      | DDR3-1066 | DDR3-1333 | DDR3-1600 |
| Maximum peak amplitude allowed for overshoot area (See Figure 9)  | 0.4V          | 0.4V      | 0.4V      | 0.4V      |
| Maximum peak amplitude allowed for undershoot area (See Figure 9) | 0.4V          | 0.4V      | 0.4V      | 0.4V      |
| Maximum overshoot area above VDDQ (See Figure 9)                  | 0.25V-ns      | 0.19V-ns  | 0.15V-ns  | 0.13V-ns  |
| Maximum undershoot area below VSSQ (See Figure 9)                 | 0.25V-ns      | 0.19V-ns  | 0.15V-ns  | 0.13V-ns  |

[ Table 21 ] AC overshoot/undershoot specification for Clock, Data, Strobe and Mask

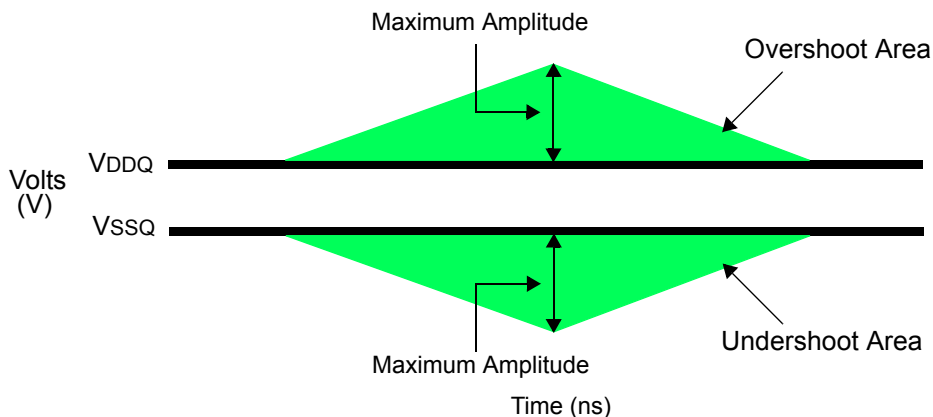


Figure 11. Clock, Data, Strobe and Mask Overshoot and Undershoot definition

9.7 34 ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown below. Output driver impedance RON is defined by the value of external reference resistor RZQ as follows:

$$RON_{34} = RZQ/7 \text{ (Nominal 34ohms +/- 10% with nominal RZQ=240ohm)}$$

The individual Pull-up and Pull-down resistors (RONpu and RONpd) are defined as follows

$$RON_{pu} = \frac{VDDQ - V_{out}}{|I_{out}|} \text{ under the condition that } RON_{pd} \text{ is turned off}$$

$$RON_{pd} = \frac{V_{out}}{|I_{out}|} \text{ under the condition that } RON_{pu} \text{ is turned off}$$

Output Driver : Definition of Voltages and Currents

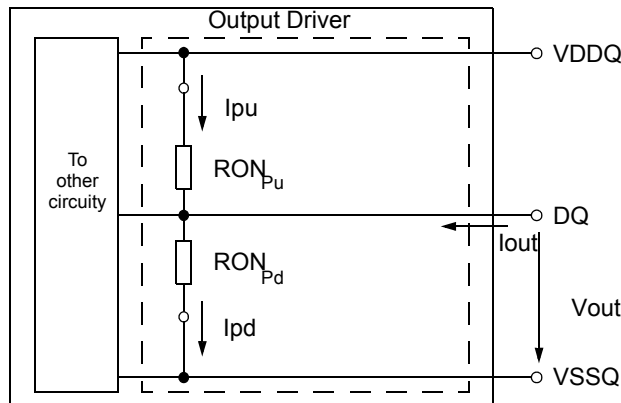


Figure 12. Output Driver : Definition of Voltages and Currents

[ Table 22 ] Output Driver DC Electrical Characteristics, assuming RZQ=240 ohms ; entire operating temperature range; after proper ZQ calibration

| RONnom   | Resistor | Vout               | Min | Nom | Max | Units | Notes |
|--|----------|--------------------|-----|-----|-----|-------|-------|
| 34Ohms   | RON34pd  | VOLdc = 0.2 x VDDQ | 0.6 | 1.0 | 1.1 | RZQ/7 | 1,2,3 |
|  |          | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.1 | RZQ/7 | 1,2,3 |
|  |          | VOHdc = 0.8 x VDDQ | 0.9 | 1.0 | 1.4 | RZQ/7 | 1,2,3 |
|  | RON34pu  | VOLdc = 0.2 x VDDQ | 0.9 | 1.0 | 1.4 | RZQ/7 | 1,2,3 |
|  |          | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.1 | RZQ/7 | 1,2,3 |
|  |          | VOHdc = 0.8 x VDDQ | 0.6 | 1.0 | 1.1 | RZQ/7 | 1,2,3 |
| Mismatch between Pull-up and Pull-down, MMpupd |          | VOMdc = 0.5 x VDDQ | -10 |     | 10  | %     | 1,2,4 |

Note :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS
3. Pull-down and pull-up output driver impedance are recommended to be calibrated at 0.5 X VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 X VDDQ and 0.8 X VDDQ
4. Measurement definition for mismatch between pull-up and pull-down, MMpupd: Measure RONpu and RONpd. both at 0.5 X VDDQ:

$$MMpupd = \frac{RON_{pu} - RON_{pd}}{RON_{nom}} \times 100$$

9.7.1 Output Drive Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to table below

$\Delta T = T - T(@\text{calibration})$ ;  $\Delta V = VDDQ - VDDQ (@\text{calibration})$ ;  $VDD = VDDQ$

\* $dR_{ONdT}$  and  $dR_{ONdV}$  are not subject to production test but are verified by design and characterization

[ Table 23 ] Output Driver Sensitivity Definition

|                     | Min   | Max   | Units |
|---------------------|---|---|-------|
| $R_{ONPU}@V_{OHDC}$ | $0.6 - dR_{ONdTH} *  \Delta T  - dR_{ONdVH} *  \Delta V $ | $1.1 + dR_{ONdTH} *  \Delta T  + dR_{ONdVH} *  \Delta V $ | RZQ/7 |
| $R_{ON}@V_{OMDC}$   | $0.9 - dR_{ONdTM} *  \Delta T  - dR_{ONdVM} *  \Delta V $ | $1.1 + dR_{ONdTM} *  \Delta T  + dR_{ONdVM} *  \Delta V $ | RZQ/7 |
| $R_{ONPD}@V_{OLDC}$ | $0.6 - dR_{ONdTL} *  \Delta T  - dR_{ONdVL} *  \Delta V $ | $1.1 + dR_{ONdTL} *  \Delta T  + dR_{ONdVL} *  \Delta V $ | RZQ/7 |

[ Table 24 ] Output Driver Voltage and Temperature Sensitivity

|              | Min | Max  | Units |
|--------------|-----|------|-------|
| $dR_{ONdTM}$ | 0   | 1.5  | %/°C  |
| $dR_{ONdVM}$ | 0   | 0.15 | %/mV  |
| $dR_{ONdTL}$ | 0   | 1.5  | %/°C  |
| $dR_{ONdVL}$ | 0   | TBD  | %/mV  |
| $dR_{ONdTH}$ | 0   | 1.5  | %/°C  |
| $dR_{ONdVH}$ | 0   | TBD  | %/mV  |

9.8 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance  $R_{TT}$  is defined by bits A9, A6 and A2 of MR1 register.

ODT is applied to the DQ, DQ, DQS/DQS and TDQS, TDQS (x8 devices only) pins.

A functional representation of the on-die termination is shown below. The individual pull-up and pull-down resistors ( $R_{TTpu}$  and  $R_{TTpd}$ ) are defined as follows :

$$R_{TTpu} = \frac{VDDQ - V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{TTpd} \text{ is turned off}$$

$$R_{TTpd} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{TTpu} \text{ is turned off}$$

On-Die Termination : Definition of Voltages and Currents

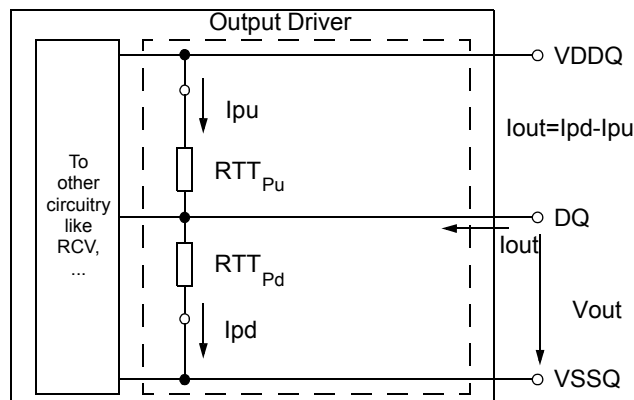


Figure 13. On-Die Termination : Definition of Voltages and Currents

## 9.8.1 ODT DC electrical characteristics

Table # provides an overview of the ODT DC electrical characteristics. The values for  $RTT_{60pd120}$ ,  $RTT_{60pu120}$ ,  $RTT_{120pd240}$ ,  $RTT_{120pu240}$ ,  $RTT_{40pd80}$ ,  $RTT_{40pu80}$ ,  $RTT_{30pd60}$ ,  $RTT_{30pu60}$ ,  $RTT_{20pd40}$ ,  $RTT_{20pu40}$  are not specification requirements, but can be used as design guide lines:.

| MR1 (A9,A6,A2)                    | RTT  | RESISTOR                | Vout     | MIN | NOM                 | MAX   | UNIT               | NOTES   |
|-----------------------------------|--|-------------------------|----------|-----|---------------------|-------|--------------------|---------|
| (0,1,0)                           | 120 ohm                                    | RTT <sub>120pd240</sub> | 0.2XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub>    | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub>    | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub>    | 1,2,3,4 |
|                                   |  | RTT <sub>120pu240</sub> | 0.2XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub>    | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub>    | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub>    | 1,2,3,4 |
| RTT <sub>120</sub>                | V <sub>IL(AC)</sub> TO V <sub>IH(AC)</sub> | 0.9                     | 1.0      | 1.6 | R <sub>ZQ</sub> /2  | 1,2,5 |                    |         |
| (0,0,1)                           | 60 ohm                                     | RTT <sub>60pd240</sub>  | 0.2XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /2 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /2 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /2 | 1,2,3,4 |
|                                   |  | RTT <sub>60pu240</sub>  | 0.2XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /2 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /2 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /2 | 1,2,3,4 |
| RTT <sub>60</sub>                 | V <sub>IL(AC)</sub> TO V <sub>IH(AC)</sub> | 0.9                     | 1.0      | 1.6 | R <sub>ZQ</sub> /4  | 1,2,5 |                    |         |
| (0,1,1)                           | 40 ohm                                     | RTT <sub>40pd240</sub>  | 0.2XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /3 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /3 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /3 | 1,2,3,4 |
|                                   |  | RTT <sub>40pu240</sub>  | 0.2XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /3 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /3 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /3 | 1,2,3,4 |
| RTT <sub>40</sub>                 | V <sub>IL(AC)</sub> TO V <sub>IH(AC)</sub> | 0.9                     | 1.0      | 1.6 | R <sub>ZQ</sub> /6  | 1,2,5 |                    |         |
| (1,0,1)                           | 30 ohm                                     | RTT <sub>60pd240</sub>  | 0.2XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /4 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /4 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /4 | 1,2,3,4 |
|                                   |  | RTT <sub>60pu240</sub>  | 0.2XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /4 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /4 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /4 | 1,2,3,4 |
| RTT <sub>60</sub>                 | V <sub>IL(AC)</sub> TO V <sub>IH(AC)</sub> | 0.9                     | 1.0      | 1.6 | R <sub>ZQ</sub> /8  | 1,2,5 |                    |         |
| (1,0,0)                           | 20 ohm                                     | RTT <sub>60pd240</sub>  | 0.2XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /6 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /6 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /6 | 1,2,3,4 |
|                                   |  | RTT <sub>60pu240</sub>  | 0.2XVDDQ | 0.9 | 1.0                 | 1.4   | R <sub>ZQ</sub> /6 | 1,2,3,4 |
|                                   |  |                         | 0.5XVDDQ | 0.9 | 1.0                 | 1.1   | R <sub>ZQ</sub> /6 | 1,2,3,4 |
|                                   |  |                         | 0.8XVDDQ | 0.6 | 1.0                 | 1.1   | R <sub>ZQ</sub> /6 | 1,2,3,4 |
| RTT <sub>60</sub>                 | V <sub>IL(AC)</sub> TO V <sub>IH(AC)</sub> | 0.9                     | 1.0      | 1.6 | R <sub>ZQ</sub> /12 | 1,2,5 |                    |         |
| Deviation of VM w.r.t VDDQ/2, ΔVM |  |                         |          | -5  |                     | 5     | %                  | 1,2,5,6 |

[ Table 25 ] ODT DC Electrical characteristics, assuming RZQ=240 ohm +/- 1% entire operating temperature range; after proper ZQ calibration

**Note :**

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5XVDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2XVDDQ and 0.8XVDDQ.
4. Not a specification requirement, but a design guide line
5. Measurement definition for RTT:

Apply VIH(ac) to pin under test and measure current I(VIH(ac)), then apply VIL(ac) to pin under test and measure current I(VIL(ac)) respectively

$$RTT = \frac{VIH(ac) - VIL(ac)}{I(VIH(ac)) - I(VIL(ac))}$$

6. Measurement definition for VM and ΔVM : Measure voltage (VM) at test pin (midpoint) with no load

$$\Delta VM = \left( \frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

**9.8.2 ODT Temperature and Voltage sensitivity**

If temperature and/or voltage change after calibration, the tolerance limits widen according to table below

ΔT = T - T(@calibration); ΔV = VDDQ - VDDQ (@calibration); VDD = VDDQ

**[ Table 26 ] ODT Sensitivity Definition**

|     | Min  | Max  | Units          |
|-----|--|--|----------------|
| RTT | 0.9 - dR <sub>TT</sub> dT *  ΔT  - dR <sub>TT</sub> dV *  ΔV | 1.6 + dR <sub>TT</sub> dT *  ΔT  + dR <sub>TT</sub> dV *  ΔV | RZQ/2,4,6,8,12 |

**[ Table 27 ] ODT Voltage and Temperature Sensitivity**

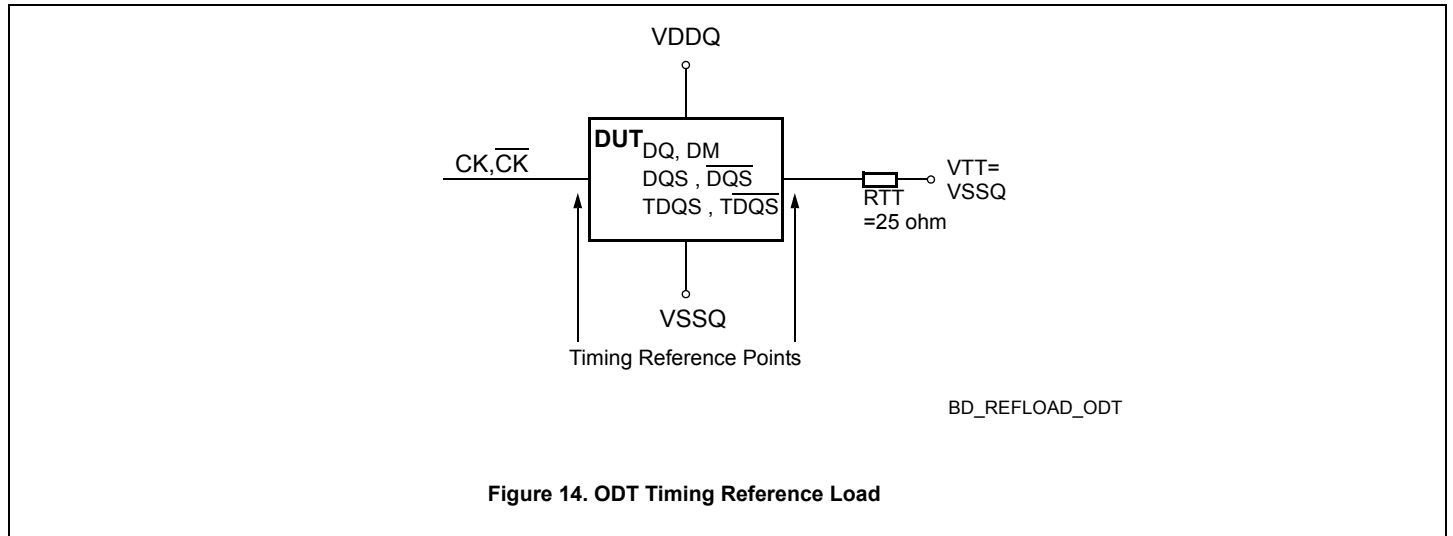
|                     | Min | Max  | Units |
|---------------------|-----|------|-------|
| dR <sub>TT</sub> dT | 0   | 1.5  | %/°C  |
| dR <sub>TT</sub> dV | 0   | 0.15 | %/mV  |

These parameters may not be subject to production test. They are verified by design and characterization.

9.9 ODT Timing Definitions

9.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 14.



9.9.2 ODT Timing Definition

Definitions for  $t_{AON}$ ,  $t_{AONPD}$ ,  $t_{AOF}$ ,  $t_{AOFPD}$  and  $t_{ADC}$  are provided in Table 28 and subsequent figures. Measurement reference settings are provided in Table 29.

[ Table 28 ] ODT Timing Definitions

| Symbol      | Begin Point Definition  | End Point Definition   | Figure   |
|-------------|---|--|----------|
| $t_{AON}$   | Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLon                        | Extrapolated point at VSSQ   | Figure 2 |
| $t_{AONPD}$ | Rising edge of CK - $\overline{CK}$ with ODT being first registered high                      | Extrapolated point at VSSQ   | Figure 3 |
| $t_{AOF}$   | Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLoff                       | End point: Extrapolated point at VRTT_Nom                          | Figure 4 |
| $t_{AOFPD}$ | Rising edge of CK - $\overline{CK}$ with ODT being first registered low                       | End point: Extrapolated point at VRTT_Nom                          | Figure 5 |
| $t_{ADC}$   | Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLcwn, ODTLcwn4 of ODTLcwn8 | End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively | Figure 6 |

[ Table 29 ] Reference Settings for ODT Timing Measurements

| Measured Parameter | RTT_Nom Setting | RTT_Wr Setting | V <sub>sw1</sub> [V] | V <sub>sw2</sub> [V] | Note |
|--------------------|-----------------|----------------|----------------------|----------------------|------|
| $t_{AON}$          | $R_{ZQ}/4$      | NA             | 0.05                 | 0.10                 |      |
|                    | $R_{ZQ}/12$     | NA             | 0.10                 | 0.20                 |      |
| $t_{AONPD}$        | $R_{ZQ}/4$      | NA             | 0.05                 | 0.10                 |      |
|                    | $R_{ZQ}/12$     | NA             | 0.10                 | 0.20                 |      |
| $t_{AOF}$          | $R_{ZQ}/4$      | NA             | 0.05                 | 0.10                 |      |
|                    | $R_{ZQ}/12$     | NA             | 0.10                 | 0.20                 |      |
| $t_{AOFPD}$        | $R_{ZQ}/4$      | NA             | 0.05                 | 0.10                 |      |
|                    | $R_{ZQ}/12$     | NA             | 0.10                 | 0.20                 |      |
| $t_{ADC}$          | $R_{ZQ}/12$     | $R_{ZQ}/2$     | 0.20                 | 0.30                 |      |

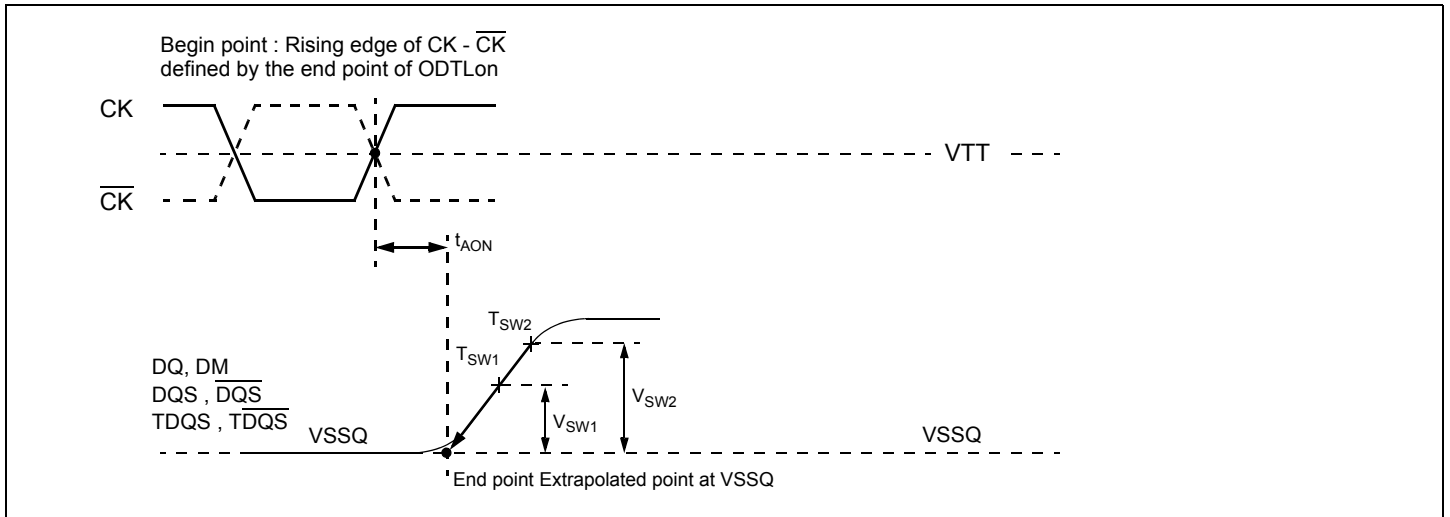


Figure 15. Definition of tAON

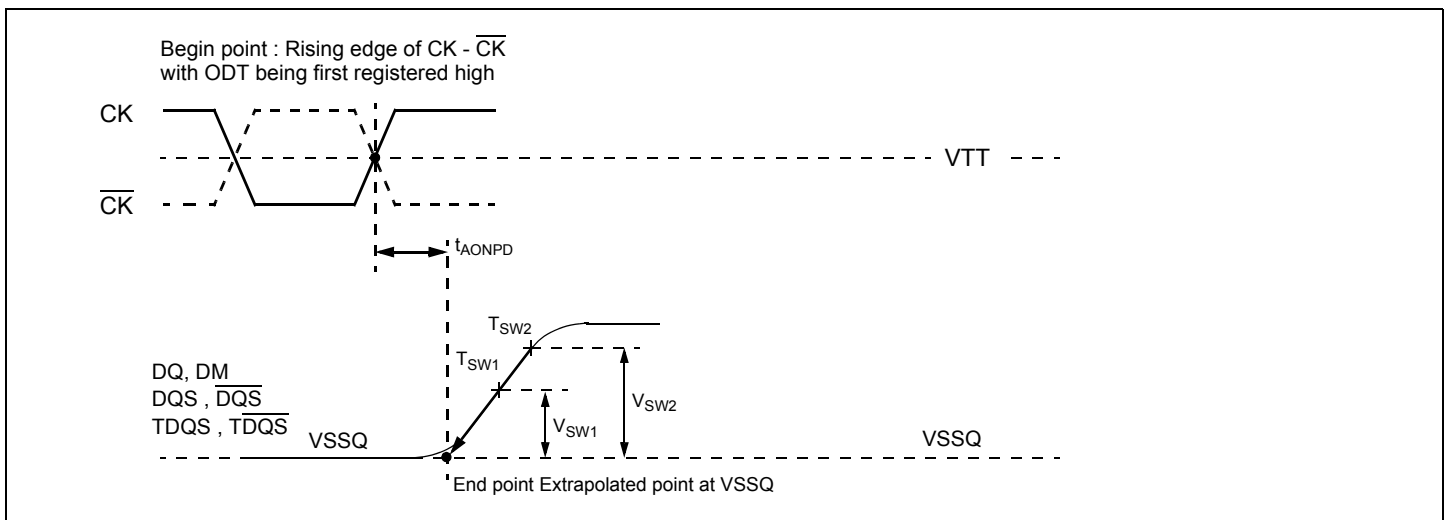


Figure 16. Definition of tAONPD

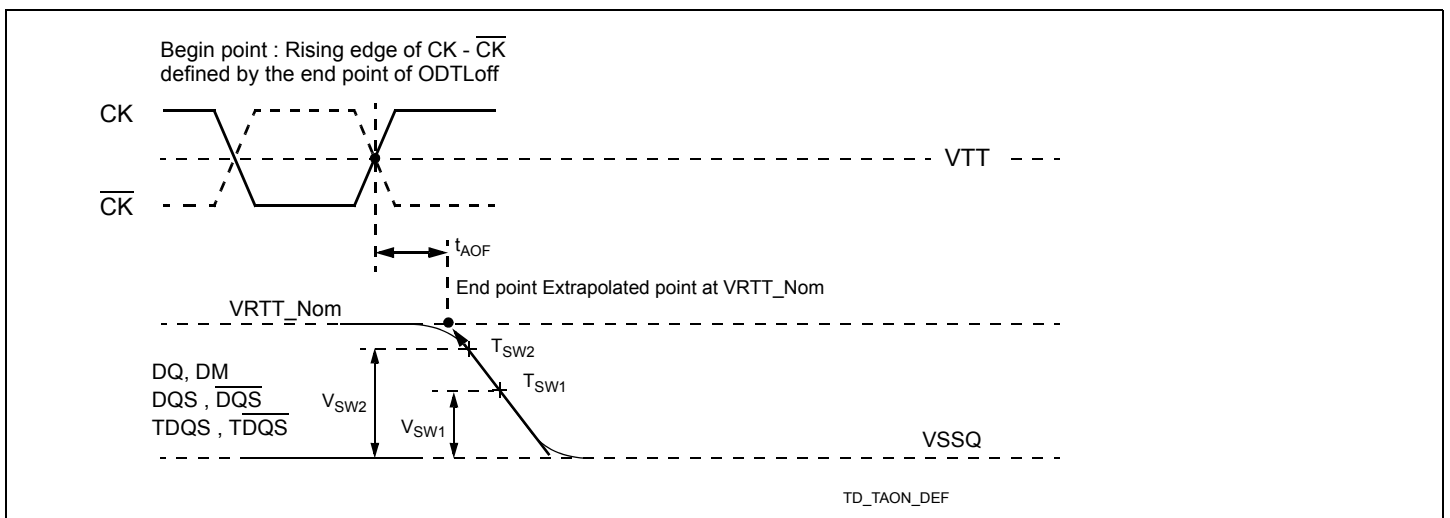


Figure 17. Definition of tAOF

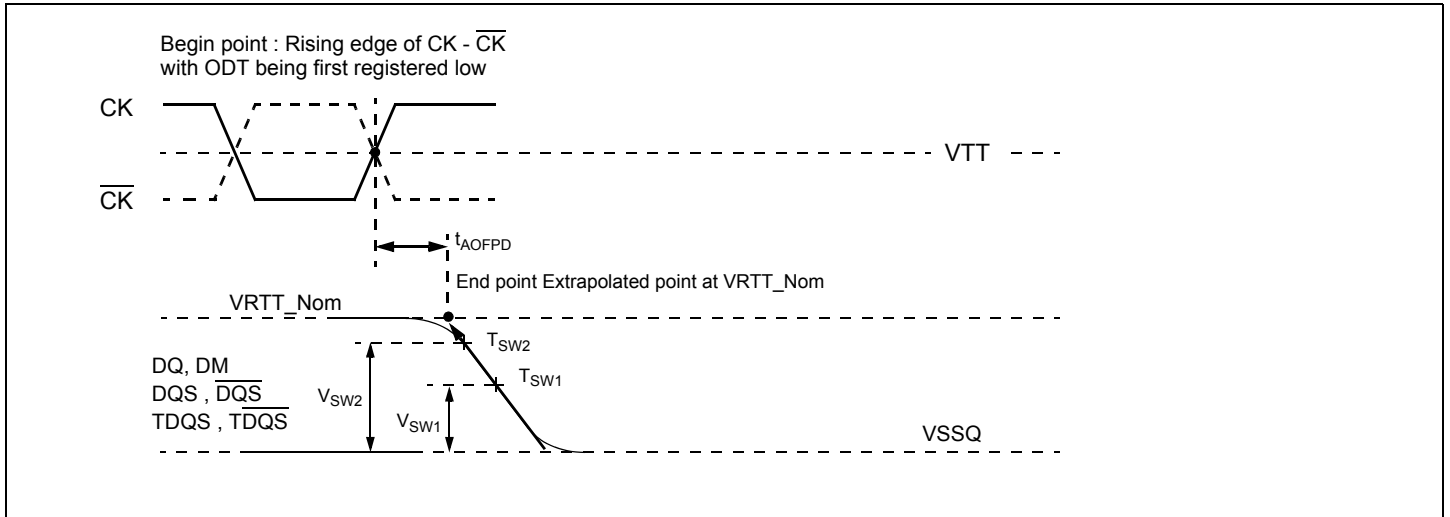


Figure 18. Definition of  $t_{\text{AOFPD}}$

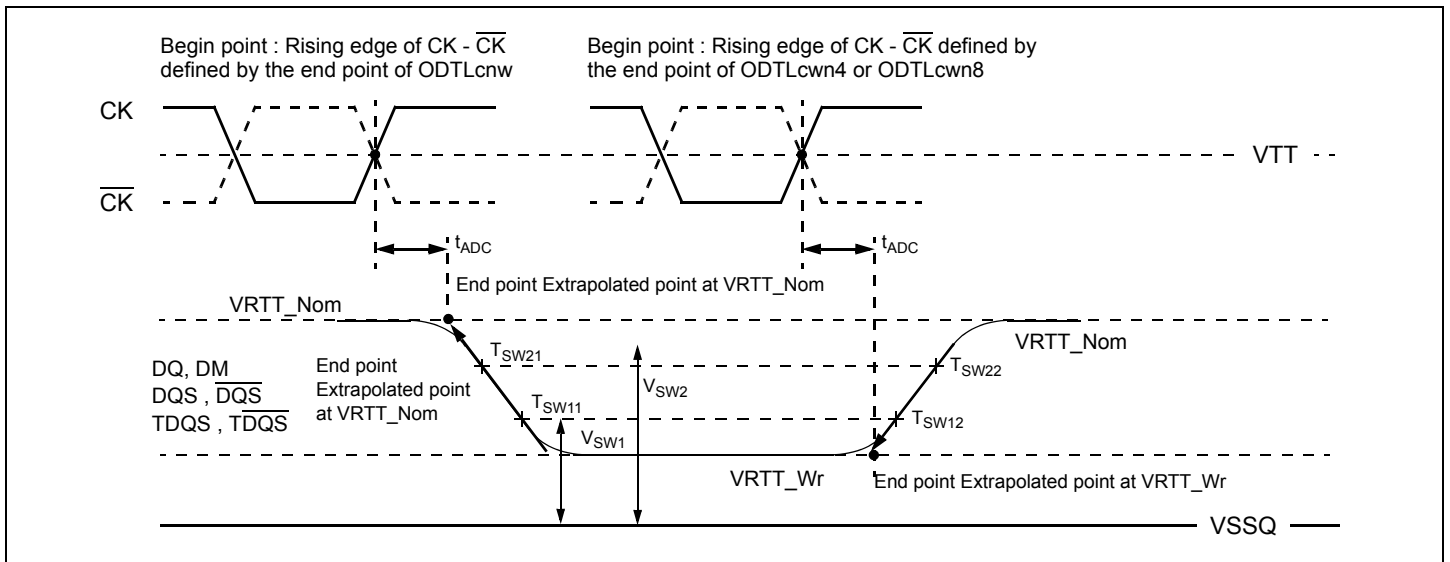


Figure 19. Definition of  $t_{\text{ADC}}$

## 10.0 Idd Specification Parameters and Test Conditions

### 10.1 IDD Measurement Conditions

Within the tables provided further down, an overview about the IDD measurement conditions is provided as follows:

[ Table 30 ] Overview of Tables providing IDD Measurement Conditions and DRAM Behavior

| Table number | Measurement Conditions  |
|--------------|---|
| Table 34     | IDD0 and IDD1   |
| Table 35     | IDD2N, IDD2Q, IDD2P(0), IDD2P(1)                                    |
| Table 36     | IDD3N and IDD3P   |
| Table 37     | IDD4R, IDD4W, IDD7  |
| Table 38     | IDD7 for different speed grades and different tRRD, tFAW conditions |
| Table 39     | IDD5B   |
| Table 40     | IDD6, IDD6ET  |

Within the tables about IDD measurement conditions, the following definitions are used:

- LOW is defined as  $V_{IN} \leq V_{ILAC}(\text{max.})$ ; HIGH is defined as  $V_{IN} \geq V_{IHAC}(\text{min.})$ ;
- STABLE is defined as inputs are stable at a HIGH or LOW level
- FLOATING is defined as inputs are  $V_{REF} = V_{DDQ} / 2$
- SWITCHING is defined as described in the following 2 tables.

[ Table 31 ] Definition of SWITCHING for Address and Command Input Signals

| SWITCHING for Address (row, column) and Command Signals ( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ ) is defined as: |  |
|--|--|
| <b>Address</b><br>(Row, Column):   | If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value<br>(e.g. Ax Ax Ax Ax Ax Ax Ax Ax Ax Ax Ax .....<br>please see each IDDX definition for details   |
| <b>Bank address:</b>   | If not otherwise mentioned the bank addresses should be switched like the row/<br>column addresses - please see each IDDX definition for details   |
| <b>Command</b><br>( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ ):   | Define $D = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} := \{\text{HIGH}, \text{LOW}, \text{LOW}, \text{LOW}\}$<br>Define $\overline{D} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} := \{\text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}\}$<br><br>Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ ...<br><br>If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R) the Background Pattern Command is substituted by the respective $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ levels of the necessary command.<br>See each IDDX definition for details and figures 1,2,3 as examples. |

[ Table 32 ] Definition of SWITCHING for Data (DQ)

| SWITCHING for Data (DQ) is defined as |  |
|---------------------------------------|--|
| <b>Data</b><br>(DQ)                   | Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDX definition for exceptions from this rule and for further details.<br>See figures 1,2,3 as examples. |
| <b>Data Masking (DM)</b>              | NO Switching; DM must be driven LOW all the time   |

Timing parameters are listed in the following table:

[ Table 33 ] For IDD testing the following parameters are utilized.

| Parameter Bin                |       | DDR3-800 | DDR3-1066 |       | DDR3-1333 |       | Unit |
|------------------------------|-------|----------|-----------|-------|-----------|-------|------|
|                              |       | 6-6-6    | 7-7-7     | 8-8-8 | 8-8-8     | 9-9-9 |      |
| t <sub>CKmin</sub> (IDD)     |       | 2.5      | 1.875     |       | 1.5       |       | ns   |
| CL(IDD)                      |       | 6        | 7         | 8     | 8         | 9     |      |
| t <sub>RCDmin</sub> (IDD)    |       | 15       | 13.13     | 15    | 12        | 13.5  | ns   |
| t <sub>RCmin</sub> (IDD)     |       | 52.5     | 50.63     | 52.50 | 48        | 49.5  | ns   |
| t <sub>RASmin</sub> (IDD)    |       | 37.5     | 37.5      | 37.5  | 36        | 36    | ns   |
| t <sub>RPmin</sub> (IDD)     |       | 15       | 13.13     | 15    | 12        | 13.5  | ns   |
| t <sub>FAW</sub> (IDD)       | x4/x8 | 40       | 37.5      | 37.5  | 30        | 30    | ns   |
|                              | x16   | 50       | 50        | 50    | 45        | 45    | ns   |
| t <sub>RRD</sub> (IDD)       | x4/x8 | 10       | 7.5       | 7.5   | 6.0       | 6.0   | ns   |
|                              | x16   | 10       | 10        | 10    | 7.5       | 7.5   | ns   |
| t <sub>RFC</sub> (IDD) - 1Gb |       | 110      | 110       | 110   | 110       | 110   | 110  |

The following conditions apply:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric test conditions.
3. IDD parameters are specified with ODT and output buffer disabled (MR1 Bit A12).

[ Table 34 ] IDD Measurement Conditions for IDD0 and IDD1

| Current  | IDD0  | IDD1   |
|--|---|--|
| Name   | Operating Current 0<br>-> One Bank Activate<br>-> Precharge   | Operating Current 1<br>-> One Bank Activate<br>-> Read<br>-> Precharge   |
| <b>Measurement Condition</b>   |   |  |
| Timing Diagram Example   |   | Figure 1   |
| CKE  | HIGH  | HIGH   |
| External Clock   | on  | on   |
| t <sub>CK</sub>  | t <sub>CKmin</sub> (IDD)  | t <sub>CKmin</sub> (IDD)   |
| t <sub>RC</sub>  | t <sub>RCmin</sub> (IDD)  | t <sub>RCmin</sub> (IDD)   |
| t <sub>RAS</sub>   | t <sub>RASmin</sub> (IDD)   | t <sub>RASmin</sub> (IDD)  |
| t <sub>RCD</sub>   | n.a.  | t <sub>RCDmin</sub> (IDD)  |
| t <sub>RRD</sub>   | n.a.  | n.a.   |
| CL   | n.a.  | CL(IDD)  |
| AL   | n.a.  | 0  |
| $\overline{\text{CS}}$   | HIGH between. Activate and Precharge Commands   | HIGH between Activate, Read and Precharge  |
| Command Inputs ( $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ ) | SWITCHING as described in Table 2;<br>only exceptions are Activate and Precharge commands; example of IDD0 pattern:<br><br>A0 D $\overline{\text{D}}$ $\overline{\text{D}}$ D D $\overline{\text{D}}$ $\overline{\text{D}}$ D D $\overline{\text{D}}$ $\overline{\text{D}}$ P0<br>(DDR3-800: t <sub>RAS</sub> = 37.5ns between (A)ctivate and (P)recharge to bank 0 ; Definition of D and $\overline{\text{D}}$ : see Table 2)<br><br>Definition of D and $\overline{\text{D}}$ : See table ##. | SWITCHING as described in Table 2;<br>only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern:<br><br>A0 D $\overline{\text{D}}$ $\overline{\text{D}}$ D R0 D $\overline{\text{D}}$ $\overline{\text{D}}$ DD $\overline{\text{D}}$ $\overline{\text{D}}$ DD $\overline{\text{D}}$ P0<br>(DDR3-800 -555: t <sub>RCD</sub> = 12.5ns between (A)ctivate and (R)ead to bank 0 ; Definition of D and $\overline{\text{D}}$ : see Table 2)<br><br>Definition of D and $\overline{\text{D}}$ : See table ##. |
| Row, Column Addresses  | Row addresses SWITCHING as described in Table 2;<br>Address Input A10 must be LOW all the time!   | Row addresses SWITCHING as described in Table 2;<br>Address Input A10 must be LOW all the time!  |
| Bank Addresses   | bank address is fixed (bank 0)  | bank address is fixed (bank 0)   |
| Data I/O   | SWITCHING as described in Table 3   | Read Data: output data switches every clock, which means that Read data is stable during one clock cycle. To achieve I <sub>out</sub> = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1".<br>When there is no read data burst from DRAM the DQ I/O should be FLOATING.   |
| Output Buffer DQ,DQS / MR1 bit A12   | off / 1   | off / 1  |
| Rtt_NOM, Rtt_WR  | disabled  | disabled   |
| Burst length   | n.a.  | 8 fixed / MR0 Bits [A1, A0] = {0,0}  |
| Active banks   | one ACT-PRE loop  | one ACT-RD-PRE loop  |
| Idle banks   | all other   | all other  |
| Precharge Power Down Mode / Mode Register Bit 12   | n.a.  | n.a.   |

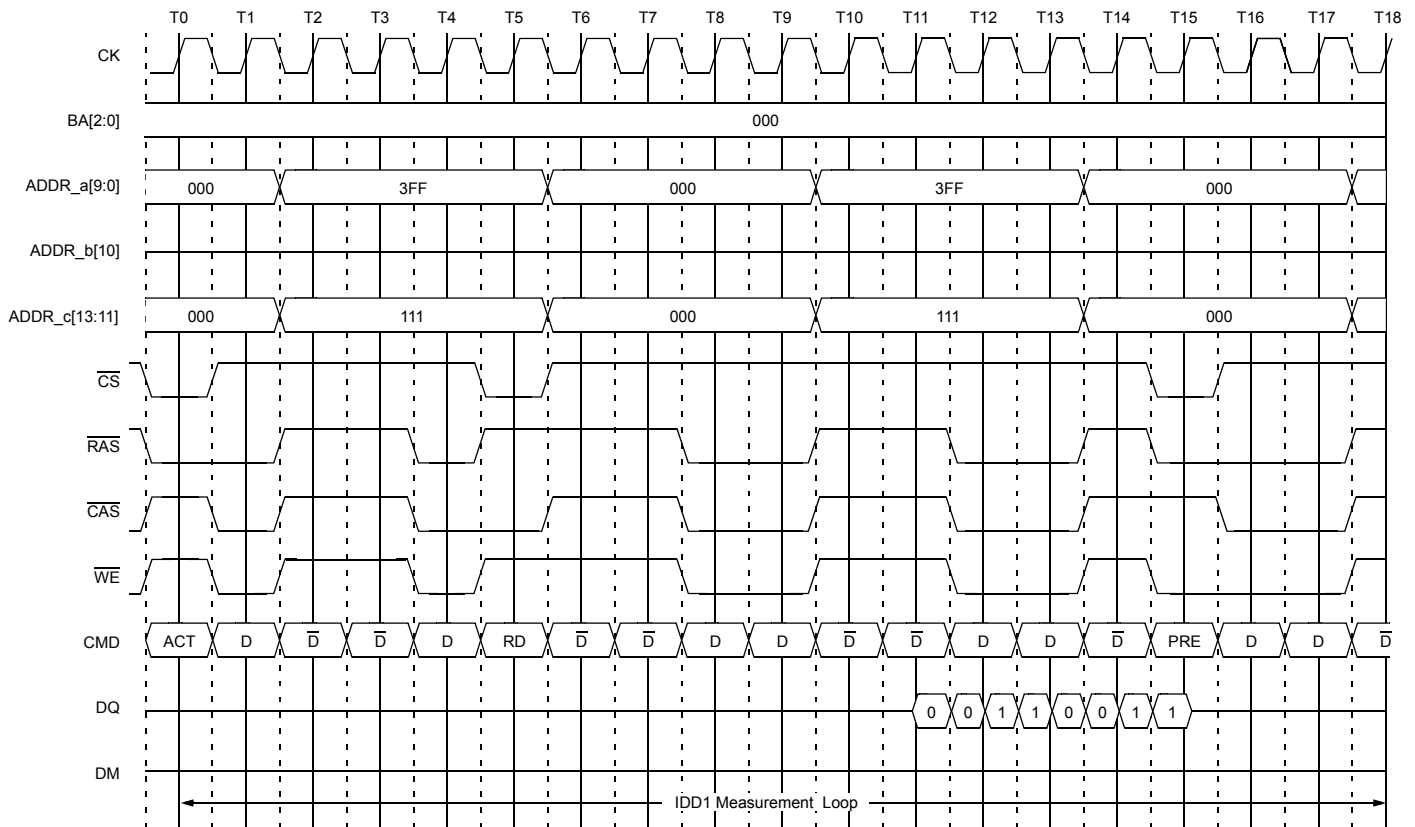


Figure 20.

IDD1 Example (DDR3-800-666, 1Gb x8): Data DQ is shown but the output buffer should be switched off (per MR1 Bit A12 = "1") to achieve  $I_{out} = 0mA$ . Address inputs are split into 3 parts.

[ Table 35 ] IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q

| Current  | IDD2N                             | IDD2P(1) a   | IDD2P(0)   | IDD2Q                           |
|--|-----------------------------------|--|--|---------------------------------|
| Name   | Precharge Standby Current         | Precharge Power Down Current<br>Fast Exit -<br>MRS A12 Bit = 1 | Precharge Power Down Current<br>Slow Exit -<br>MRS A12 Bit = 0                       | Precharge Quiet Standby Current |
| <b>Measurement Condition</b>                               |                                   |  |  |                                 |
| Timing Diagram Example                                     | Figure 2                          |  |  |                                 |
| CKE  | HIGH                              | LOW  | LOW  | LOW                             |
| External Clock   | on                                | on   | on   | on                              |
| t <sub>CK</sub>  | t <sub>CKmin</sub> (IDD)          | t <sub>CKmin</sub> (IDD)                                       | t <sub>CKmin</sub> (IDD)   | t <sub>CKmin</sub> (IDD)        |
| t <sub>RC</sub>  | n.a.                              | n.a.   | n.a.   | n.a.                            |
| t <sub>RAS</sub>   | n.a.                              | n.a.   | n.a.   | n.a.                            |
| t <sub>RCD</sub>   | n.a.                              | n.a.   | n.a.   | n.a.                            |
| t <sub>RRD</sub>   | n.a.                              | n.a.   | n.a.   | n.a.                            |
| CL   | n.a.                              | n.a.   | n.a.   | n.a.                            |
| AL   | n.a.                              | n.a.   | n.a.   | n.a.                            |
| $\overline{\text{CS}}$                                     | HIGH                              | STABLE   | HIGH   | STABLE                          |
| Bank Address, Row Addr. and Command Inputs                 | SWITCHING as described in Table 2 | STABLE   | STABLE   | STABLE                          |
| Data inputs  | SWITCHING                         | FLOATING   | FLOATING   | FLOATING                        |
| Output Buffer DQ,DQS / MR1 bit A12                         | off / 1                           | off / 1  | off / 1  | off / 1                         |
| Rtt_NOM, Rtt_WE  | disabled                          | disabled   | disabled   | disabled                        |
| Burst length   | n.a.                              | n.a.   | n.a.   | n.a.                            |
| Active banks   | none                              | none   | none   | none                            |
| Idle banks   | all                               | all  | all  | all                             |
| Precharge Power Down Mode / Mode Register Bit <sup>a</sup> | n.a.                              | Fast Exit / 1<br>(any valid command after t <sub>XP1</sub> )   | Slow Exit / 0<br>Slow exit (RD and ODT commands must satisfy t <sub>XPDLL-AL</sub> ) | n.a.                            |

Note :

- In DDR3 the MRS Bit 12 defines DLL on/off behavior ONLY for precharge power down. There are 2 different Precharge Power Down states possible : one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).
- Because it is an exit after precharge power down the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh.

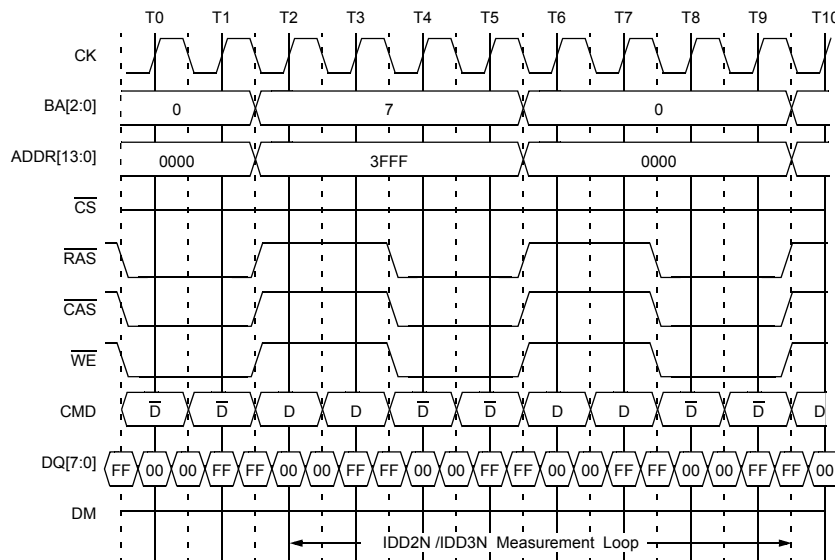


Figure 21. IDD2N /IDD3N Example (DDR3-800-666, 1Gb X8)

[ Table36 ] IDD Measurement Conditions for IDD3N and IDD3P(fast exit)

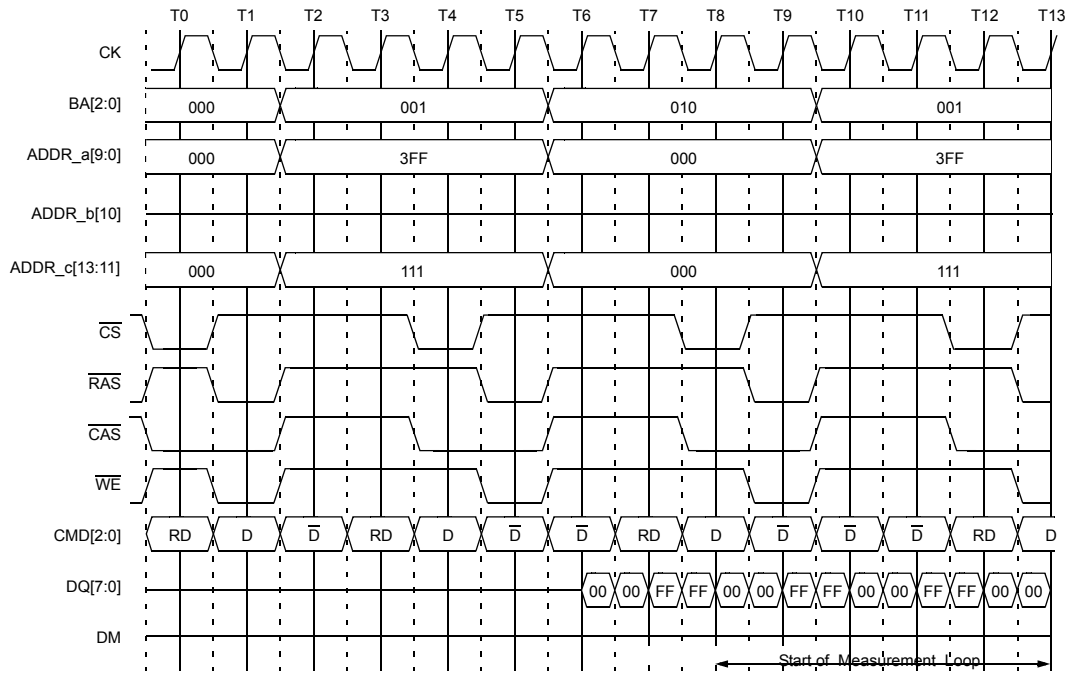
| Current   | IDD3N                             | IDD3P   |
|---|-----------------------------------|---|
| Name  | Active Standby Current            | Active Power-Down Current <sup>a</sup><br>Always Fast Exit        |
| <b>Measurement Condition</b>                                  |                                   |   |
| Timing Diagram Example  | Figure 2                          |   |
| CKE   | HIGH                              | LOW   |
| External Clock  | on                                | on  |
| t <sub>CK</sub>   | t <sub>CKmin</sub> (IDD)          | t <sub>CKmin</sub> (IDD)  |
| t <sub>RC</sub>   | n.a.                              | n.a.  |
| t <sub>RAS</sub>  | n.a.                              | n.a.  |
| t <sub>RCD</sub>  | n.a.                              | n.a.  |
| t <sub>RRD</sub>  | n.a.                              | n.a.  |
| CL  | n.a.                              | n.a.  |
| AL  | n.a.                              | n.a.  |
| $\overline{\text{CS}}$  | HIGH                              | STABLE  |
| Addr. and cmd Inputs  | SWITCHING as described in Table 2 | STABLE  |
| Data inputs   | SWITCHING as described in Table 3 | FLOATING  |
| Output Buffer DQ,DQS / MR1 bit A12                            | off / 1                           | off / 1   |
| Rtt_NOM, Rtt_WE   | disabled                          | disabled  |
| Burst length  | n.a.                              | n.a.  |
| Active banks  | all                               | all   |
| Idle banks  | none                              | none  |
| Precharge Power<br>Down Mode / Mode Register Bit <sup>a</sup> | n.a.                              | n.a. (Active Power Down<br>Mode is always "Fast Exit" with DLL on |

Note :

1. DDR3 will offer only ONE active power down mode with DLL on (-> fast exit). MRS bit 12 will not be used for active power down. Instead bit A12 will be used to switch between two different precharge power down modes.

[ Table 37 ] IDD Measurement Conditions for IDD4R, IDD4W and IDD7

| Current   | IDD4R   | IDD4W   | IDD7   |
|---|---|---|--|
| Name  | Operating Current Burst Read  | Operating Current Burst Write   | All Bank Interleave Read Current   |
| <b>Measurement Condition</b>  |   |   |  |
| Timing Diagram Example  | Figure 3  |   |  |
| CKE   | HIGH  | HIGH  | HIGH   |
| External Clock  | on  | on  | on   |
| t <sub>CK</sub>   | t <sub>CKmin</sub> (IDD)  | t <sub>CKmin</sub> (IDD)  | t <sub>CKmin</sub> (IDD)   |
| t <sub>RC</sub>   | n.a.  | n.a.  | t <sub>RCmin</sub> (IDD)   |
| t <sub>RAS</sub>  | n.a.  | n.a.  | t <sub>RASmin</sub> (IDD)  |
| t <sub>RCD</sub>  | n.a.  | n.a.  | t <sub>RCDmin</sub> (IDD)  |
| t <sub>RRD</sub>  | n.a.  | n.a.  | t <sub>RRDmin</sub> (IDD)  |
| CL  | CL(IDD)   | CL(IDD)   | CL(IDD)  |
| AL  | 0   | 0   | t <sub>RCDmin</sub> -1t <sub>CK</sub>  |
| $\overline{CS}$   | HIGH btw. valid cmds  | HIGH btw. valid cmds  | HIGH btw. valid cmds   |
| Command Inputs<br>( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ ) | SWITCHING as described in Table 2;<br>exceptions are Read commands =><br>IDD4R Pattern:<br>R0DDDR1DDDR3DDDR3DDDR4 .....<br>Rx = Read from bank x;<br>Definition of D and D: see Table 2   | SWITCHING as described in Table 2;<br>exceptions are Write commands =><br>IDD4W Pattern:<br>W0DDDW1DDDW2DDDW3DDDW4 ...<br>Wx = Write to bank x;<br>Definition of D and D: see Table 2 | For patterns see Table 9   |
| Row, Column Addresses   | column addresses<br>SWITCHING as described in Table 2;<br>Address Input A10 must be LOW all the time!   | column addresses<br>SWITCHING as described in Table 2;<br>Address Input A10 must be LOW all the time!   | STABLE during DESELECTs  |
| Bank Addresses  | bank address cycling (0 ->1 -> 2 -> 3 ...)  | bank address cycling (0 ->1 -> 2 -> 3 ...)  | bank address cycling (0 ->1 -> 2 -> 3 ...),<br>see pattern in Table 9  |
| DQ I/O  | Seamless Read Data Burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle.<br>To achieve I <sub>out</sub> = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1". | Seamless Write Data Burst (BL8): input data switches every clock, which means that Write data is stable during one clock cycle.<br>DM is low all the time.                            | Read Data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle.<br>To achieve I <sub>out</sub> = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1". |
| Output Buffer DQ,DQS / MR1 bit A12  | off / 1   | off / 1   | off / 1  |
| Rtt_NOM, Rtt_WE   | disabled  | disabled  | disabled   |
| Burst length  | 8 fixed / MR0 Bits [A1, A0] = {0,0}   | 8 fixed / MR0 Bits [A1, A0] = {0,0}   | 8 fixed / MR0 Bits [A1, A0] = {0,0}  |
| Active banks  | all   | all   | all  |
| Idle banks  | none  | none  | none   |
| Precharge Power Down Mode / Mode Register Bit   | n.a.  | n.a.  | n.a.   |



**Figure 22**  
**IDD4R Example (DDR3-800-666,1Gb x8): data DQ is shown but the output buffer should be switched off (per MR1 Bit A12="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.**

[ Table 38 ] IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions

| Speed<br>Mb/s | Bin | Org.  | tFAW | tFAW  | tRRD | tRRD  | IDD7 Pattern <sup>a</sup>  |
|---------------|-----|-------|------|-------|------|-------|--|
|               |     |       | [ns] | [CLK] | [ns] | [CLK] |  |
| 800           | all | x4/x8 | 40   | 16    | 10   | 4     | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7D D  |
|               | all | x16   | 50   | 20    | 10   | 4     | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD D D D D A4 RA4 D D A5 RA5 D D A6 RA6 DD A7 RA7 D D D D D D  |
| 1066          | all | x4/x8 | 37.5 | 20    | 7.5  | 4     | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD D D D D A4 RA4 D D A5 RA5 D D A6 RA6 DD A7 RA7 D D D D D D  |
|               | all | x16   | 50   | 27    | 10   | 6     | A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D DD D A3 RA3 D D D D D D A4 RA4 D D D D A5RA5 D D D D A6 RA6 D D D D A7 RA7 D D D DD D D D D D D                               |
| 1333          | all | x4/x8 | 30   | 20    | 6    | 4     | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD D D D D A4 RA4 D D A5 RA5 D D A6 RA6 DD A7 RA7 D D D D D D  |
|               | all | x16   | 45   | 30    | 7.5  | 5     | A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D A3RA3 D D D D D D D D D D D D A4 RA4 D D DA5 RA5 D D D A6 RA6 D D D A7 RA7 D D D DD D D D D D D D D D D                   |
| 1600          | all | x4/x8 | 30   | 24    | 6    | 5     | A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3RA3 D D D D D D D D A4 RA4 D D D A5 RA5 D DD A6 RA6 D D D A7 RA7 D D D D D D D D  |
|               | all | x16   | 40   | 32    | 7.5  | 6     | A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D DD D A3 RA3 D D D D D D D D D D D D D D A4 RA4D D D D A5 RA5 D D D D A6 RA6 D D D D A7RA7 D D D D D D D D D D D D D D D D D D |

Note :  
 1. A0 = Activation of Bank 0; RA0 = Read with Auto-Precharge of Bank 0; D = Deselect

[ Table 39 ] IDD Measurement Conditions for IDD5B

| Current                                       | IDD5B                                      |
|---|--|
| Name  | Burst Refresh Current                      |
| <b>Measurement Condition</b>                  |  |
| CKE   | HIGH                                       |
| External Clock                                | on   |
| $t_{CK}$                                      | $t_{CKmin}(IDD)$                           |
| $t_{RC}$                                      | n.a.                                       |
| $t_{RAS}$                                     | n.a.                                       |
| $t_{RCD}$                                     | n.a.                                       |
| $t_{RRD}$                                     | n.a.                                       |
| $t_{RFC}$                                     | $t_{RFCmin}(IDD)$                          |
| CL  | n.a.                                       |
| AL  | n.a.                                       |
| $\overline{CS}$                               | HIGH btw. valid cmds                       |
| Addr. and cmd Inputs                          | SWITCHING                                  |
| Data inputs                                   | SWITCHING                                  |
| Output Buffer DQ,DQS / MR1 bit A12            | off / 1                                    |
| Rtt_NOM, Rtt_WE                               | disabled                                   |
| Burst length                                  | n.a.                                       |
| Active banks                                  | Refresh command every $t_{RFC}=t_{RFCmin}$ |
| Idle banks                                    | none                                       |
| Precharge Power Down Mode / Mode Register Bit | n.a.                                       |

[ Table 40 ] IDD Measurement Conditions for IDD6 and IDD6ET

| Current   | IDD6   | IDD6ET   |
|---|--|--|
| Name  | Self-Refresh Current Normal Temperature Range<br>TCASE = 0 .. 85°C | Self-Refresh Current Extended Temperature<br>Range a TCASE = 0 .. 95°C |
| <b>Measurement Condition</b>  |  |  |
| Temperature   | TCASE = 85°C   | TCASE = 95°C   |
| Auto Self Refresh(ASR) / MR2 Bit A6   | Disabled / "0"   | Disabled / "0"   |
| Self Refresh Temperature Range<br>(SRT) / MR2 Bit A7  | Normal / "0"   | Enabled / "1"  |
| CKE   | LOW  | LOW  |
| External Clock  | OFF; CK and $\overline{CK}$ at LOW                                 | OFF; CK and $\overline{CK}$ at LOW                                     |
| $t_{CK}$  | n.a.   | n.a.   |
| $t_{RC}$  | n.a.   | n.a.   |
| $t_{RAS}$   | n.a.   | n.a.   |
| $t_{RCD}$   | n.a.   | n.a.   |
| $t_{RRD}$   | n.a.   | n.a.   |
| CL  | n.a.   | n.a.   |
| AL  | n.a.   | n.a.   |
| $\overline{CS}$   | FLOATING   | FLOATING   |
| Command Inputs<br>( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ ) | FLOATING   | FLOATING   |
| Row, Column Addresses   | FLOATING   | FLOATING   |
| Bank Addresses  | FLOATING   | FLOATING   |
| Data I/O  | FLOATING   | FLOATING   |
| Output Buffer DQ,DQS / MR1 bit A12  | off / 1  | off / 1  |
| Rtt_NOM, Rtt_WR   | disabled   | disabled   |
| Burst length  | n.a.   | n.a.   |
| Active banks  | all during self-refresh actions                                    | all during self-refresh actions  |
| Idle banks  | all btw. Self-Refresh actions                                      | all btw. Self-Refresh actions  |
| Precharge Power Down Mode<br>/ Mode Register Bit 12   | n.a.   | n.a.   |

Note :

1 .Users should refer to the DRAM supplier datasheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options referred to in this material

[ Table 41 ] IDD6 current definition

| Symbol | Parameter/Condition   |
|--------|---|
| IDD6   | Normal Temperature Range Self-Refresh Current : CKE< 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 setting A6=0 and A7=0.  |
| IDD6ET | Extended Temperature Range Self-Refresh Current: CKE<0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6=0 and A7=1. |

## 10.2 IDD Specifications

(IDD values are for full operating range of Voltage and Temperature)

| Symbol | Conditions  | Units | Notes |
|--------|---|-------|-------|
| IDD0   | <b>Operating one bank active-precharge current;</b><br>$t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RAS} = t_{RASmin}(IDD)$ ;<br>CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;<br>Address bus inputs are SWITCHING; Data bus inputs are SWITCHING   | mA    |       |
| IDD1   | <b>Operating one bank active-read-precharge current;</b><br>$I_{OUT} = 0mA$ ; BL = 8, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RAS} = t_{RASmin}(IDD)$ , $t_{RCD} = t_{RCD}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;<br>Address bus inputs are SWITCHING; Data pattern is same as IDD4W  | mA    |       |
| IDD2P  | <b>Precharge power-down current;</b><br>All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is LOW;<br>Other control and address bus inputs are STABLE; Data bus inputs are FLOATING   | mA    |       |
| IDD2Q  | <b>Precharge quiet standby current;</b><br>All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH;<br>Other control and address bus inputs are STABLE; Data bus inputs are FLOATING  | mA    |       |
| IDD2N  | <b>Precharge standby current;</b><br>All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH;<br>Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | mA    |       |
| IDD3P  | <b>Active power-down current;</b><br>All banks open; $t_{CK} = t_{CK}(IDD)$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING   | mA    |       |
| IDD3N  | <b>Active standby current;</b><br>All banks open; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RASmax}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ;<br>CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;<br>Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | mA    |       |
| IDD4W  | <b>Operating burst write current;</b><br>All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RASmax}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | mA    |       |
| IDD4R  | <b>Operating burst read current;</b><br>All banks open, Continuous burst reads, $I_{OUT} = 0mA$ ; BL = 8, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RASmax}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W  | mA    |       |
| IDD5B  | <b>Burst refresh current;</b><br>$t_{CK} = t_{CK}(IDD)$ ; Refresh command at every $t_{RFC}(IDD)$ interval;<br>CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;<br>Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | mA    |       |
| IDD6   | <b>Self refresh current;</b><br>CK and $\overline{CK}$ at 0V; $CKE \leq 0.2V$ ;<br>Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING  | mA    |       |
| IDD6ET | <b>Extended Temperature Range Self-Refresh Current;</b><br>CK and $\overline{CK}$ at 0V; $CKE \leq 0.2V$ ;<br>Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6=0 and A7=1  | mA    |       |
| IDD7   | <b>Operating bank interleave read current;</b><br>All bank interleaving reads, $I_{OUT} = 0mA$ ; BL = 8, CL = CL(IDD), AL = $t_{RCD}(IDD) - 1 * t_{CK}(IDD)$ ; $t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RRD} = t_{RRD}(IDD)$ , $t_{RCD} = 1 * t_{CK}(IDD)$ ;<br>CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;<br>Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; | mA    |       |

[ Table 42 ] IDD Specification

1Gb DDR3 SDRAM E-die IDD Spec Table

| Symbol  | 256Mx4 (K4B1G0446C) |          |       |          |       | Unit | Notes |
|---------|---------------------|----------|-------|----------|-------|------|-------|
|         | 800Mbps             | 1066Mbps |       | 1333Mbps |       |      |       |
|         | 6-6-6               | 7-7-7    | 8-8-8 | 8-8-8    | 9-9-9 |      |       |
| IDD0    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD1    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2P-F | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2P-S | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2N   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2Q   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD3P-F | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD3N   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD4R   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD4W   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD5    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD6    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD6ET  | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD7    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |

| Symbol  | 128Mx8 (K4B1G0846C) |          |       |          |       | Unit | Notes |
|---------|---------------------|----------|-------|----------|-------|------|-------|
|         | 800Mbps             | 1066Mbps |       | 1333Mbps |       |      |       |
|         | 6-6-6               | 7-7-7    | 8-8-8 | 8-8-8    | 9-9-9 |      |       |
| IDD0    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD1    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2P-F | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2P-S | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2N   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2Q   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD3P-F | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD3N   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD4R   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD4W   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD5    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD6    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD6ET  | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD7    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |

| Symbol  | 64Mx16 (K4B1G1646C) |          |       |          |       | Unit | Notes |
|---------|---------------------|----------|-------|----------|-------|------|-------|
|         | 800Mbps             | 1066Mbps |       | 1333Mbps |       |      |       |
|         | 6-6-6               | 7-7-7    | 8-8-8 | 8-8-8    | 9-9-9 |      |       |
| IDD0    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD1    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2P-F | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2P-S | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2N   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD2Q   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD3P-F | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD3N   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD4R   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD4W   | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD5    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD6    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD6ET  | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |
| IDD7    | TBD                 | TBD      | TBD   | TBD      | TBD   | mA   |       |

[ Table 43 ] IDD Specification for 1Gb DDR3 C-die

## 11.0 Input/Output Capacitance

| Parameter   | Symbol      | DDR3-800 |      | DDR3-1066 |      | DDR3-1333 |      | DDR3-1600 |      | Units | Notes    |
|---|-------------|----------|------|-----------|------|-----------|------|-----------|------|-------|----------|
|   |             | Min      | Max  | Min       | Max  | Min       | Max  | Min       | Max  |       |          |
| Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$ , TDQS, $\overline{TDQS}$ )       | CIO         | 1.5      | 3.0  | 1.5       | 3.0  | 1.5       | 2.5  | TBD       | TBD  | pF    | 1,2,3    |
| Input capacitance (CK and $\overline{CK}$ )   | CCK         | 0.8      | 1.6  | 0.8       | 1.6  | 0.8       | 1.4  | 0.8       | 1.4  | pF    | 2,3,5    |
| Input capacitance delta (CK and $\overline{CK}$ )   | CDCK        | 0        | 0.15 | 0         | 0.15 | 0         | 0.15 | 0         | 0.15 | pF    | 2,3,4    |
| Input capacitance (All other input-only pins)   | CI          | 0.75     | 1.5  | 0.75      | 1.5  | 0.75      | 1.3  | 0.75      | 1.3  | pF    | 2,3,6    |
| Input capacitance delta (DQS and $\overline{DQS}$ )                                       | CDDQS       | 0        | 0.2  | 0         | 0.2  | 0         | 0.15 | 0         | 0.15 | pF    | 2,3,12   |
| Input capacitance delta (All control input-only pins)                                     | CDI_CTRL    | -0.5     | 0.3  | -0.5      | 0.3  | -0.4      | 0.2  | -0.4      | 0.2  | pF    | 2,3,7,8  |
| Input capacitance delta (all ADD and CMD input-only pins)                                 | CDI_ADD_CMD | -0.5     | 0.5  | -0.5      | 0.5  | -0.4      | 0.4  | -0.4      | 0.4  | pF    | 2,3,9,10 |
| Input/output capacitance delta (DQ, DM, DQS, $\overline{DQS}$ , TDQS, $\overline{TDQS}$ ) | CDIO        | -0.5     | 0.3  | -0.5      | 0.3  | -0.5      | 0.3  | -0.5      | 0.3  | pF    | 2,3,11   |
| Input/output capacitance of ZQ pin  | CZQ         | -        | 3    | -         | 3    | -         | 3    | -         | 3    | pF    | 2, 3, 13 |

[ Table 44 ] Input / Output Capacitance

Note :

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS

2. This parameter is not subject to production test. It is verified by design and characterization.

The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER( VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.

3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

4. Absolute value of CCK-CCK#

5. Absolute value of CIO(DQS)-CIO(DQS#)

6. CI applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.

7. CDI\_CTRL applies to ODT, CS# and CKE

8. CDI\_CTRL=CI(CTRL)-0.5\*(CI(CLK)+CI(CLK#))

9. CDI\_ADD\_CMD applies to A0-A15, BA0-BA2, RAS#, CAS# and WE#

10. CDI\_ADD\_CMD=CI(ADD\_CMD) - 0.5\*(CI(CLK)+CI(CLK#))

11. CDIO=CIO(DQ,DM) - 0.5\*(CIO(DQS)+CIO(DQS#))

## 12.0 Electrical Characteristics and AC timing for DDR3-800 to DDR3-1600

### 12.1 Clock specification

| Parameter            | Symbol   | DDR3-800          |                   | DDR3-1066         |                   | DDR3-1333         |                   | DDR3-1600         |                   | Units |
|----------------------|----------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
|                      |          | min               | max               | min               | max               | min               | max               | min               | max               |       |
| Average clock period | tCK(avg) | 2500              | 3333              | 1875              | 3333              | 1500              | 3333              | 1250              | 3333              | ps    |
| Clock period         | tCK(abs) | tCK(avg)min       | tCK(avg)max       | tCK(avg)min       | tCK(avg)max       | tCK(avg)min       | tCK(avg)max       | tCK(avg)min       | tCK(avg)max       | ps    |
|                      |          | +<br>tJIT(per)min | +<br>tJIT(per)max | +<br>tJIT(per)min | +<br>tJIT(per)max | +<br>tJIT(per)min | +<br>tJIT(per)max | +<br>tJIT(per)min | +<br>tJIT(per)max |       |

[ Table 45 ] Clock specification

#### Add note for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$\sum \left( \begin{matrix} N \\ j=1 \end{matrix} tCK_j \right) / N \quad N=200$$

#### Add note for tCK(abs)

tCK(abs) is the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

## 12.2 Clock Jitter Specification

| Parameter  | Symbol        | DDR3-800 |      | DDR3-1066 |      | DDR3-1333 |      | DDR3-1600 |      | Units    |
|--|---------------|----------|------|-----------|------|-----------|------|-----------|------|----------|
|  |               | min      | max  | min       | max  | min       | max  | min       | max  |          |
| Clock period jitter  | tJIT(per)     | -100     | 100  | -90       | 90   | -80       | 80   | -70       | 70   | ps       |
| Clock period jitter during DLL locking period                | tJIT(per,lck) | -90      | 90   | -80       | 80   | -70       | 70   | -60       | 60   | ps       |
| Cycle to cycle clock period jitter                           | tJIT(cc)      | 200      |      | 180       |      | 160       |      | 140       |      | ps       |
| Cycle to cycle clock period jitter during DLL locking period | tJIT(cc,lck)  | 180      |      | 160       |      | 140       |      | 120       |      | ps       |
| Cumulative error across n cycles                             | tERR(nper)    | TBD      | TBD  | TBD       | TBD  | TBD       | TBD  | TBD       | TBD  | ps       |
| Average high pulse width                                     | tCH(avg)      | 0.47     | 0.53 | 0.47      | 0.53 | 0.47      | 0.53 | 0.47      | 0.53 | tCK(avg) |
| Average low pulse width                                      | tCL(avg)      | 0.47     | 0.53 | 0.47      | 0.53 | 0.47      | 0.53 | 0.47      | 0.53 | tCK(avg) |
| Duty cycle jitter  | tJIT(duty)    | -100     | 100  | -75       | 75   | -60       | 60   | -50       | 50   | ps       |

[ Table 46 ] Clock Jitter specification

Note : The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 SDRAM device.

**Add note for tCH(avg) and tCL(avg)**

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses:

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses:

$$\left( \sum_{j=1}^N tCH_j \right) / N \times tCK(avg) \quad N=200 \qquad \left( \sum_{j=1}^N tCL_j \right) / N \times tCK(avg) \quad N=200$$

**Add note for tJIT(duty)**

tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg)

tJIT(duty) = min/max of {tJIT(CH), tJIT(CL)}, where:

tJIT(CH) = {tCHi-tCH(avg) where i=1 to 200}, tJIT(CL) = {tCLi-tCL(avg) where i=1 to 200},

**Add note for tJIT(per), tJIT(per,lck)**

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). tJIT(per) = min/max of {tCKi-tCK(avg) where i=1 to 200}

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing

**Add note for tJIT(cc), tJIT(cc,lck)**

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of {tCKi+1-tCKi}

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing

**Add note for tERR(nper)**

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). This definition is TBD.

## 12.3 Refresh Parameters by Device Density

| Parameter                                   | Symbol | 512Mb                             | 1Gb | 2Gb | 4Gb | 8Gb | Units |
|---|--------|-----------------------------------|-----|-----|-----|-----|-------|
| All Bank Refresh to active/refresh cmd time | tRFC   | 90                                | 110 | 160 | 300 | 350 | ns    |
| Average periodic refresh interval           | tREFI  | 0 °C ≤ T <sub>CASE</sub> ≤ 85 °C  | 7.8 | 7.8 | 7.8 | 7.8 | μs    |
|   |        | 85 °C < T <sub>CASE</sub> ≤ 95 °C | 3.9 | 3.9 | 3.9 | 3.9 | μs    |

[ Table 47 ] Refresh parameters by device density

## 12.4 Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include t<sub>CK</sub>, t<sub>RCD</sub>, t<sub>RP</sub>, t<sub>RAS</sub> and t<sub>RC</sub> for each corresponding bin.

[ Table 48 ] DDR3-800 Speed Bins

| Speed                                    |                      | DDR3-800  |         | Units           | Note    |
|--|----------------------|-----------|---------|-----------------|---------|
| CL-nRCD-nRP                              |                      | 6 - 6 - 6 |         |                 |         |
| Parameter                                | Symbol               | min       | max     |                 |         |
| Internal read command to first data      | t <sub>AA</sub>      | 15        | 20      | ns              |         |
| ACT to internal read or write delay time | t <sub>RCD</sub>     | 15        | -       | ns              |         |
| PRE command period                       | t <sub>RP</sub>      | 15        | -       | ns              |         |
| ACT to ACT or REF command period         | t <sub>RC</sub>      | 52.5      | -       | ns              |         |
| ACT to PRE command period                | t <sub>RAS</sub>     | 37.5      | 9*tREFI | ns              | 8       |
| CL = 5 / CWL = 5                         | t <sub>CK(AVG)</sub> | Reserved  |         | ns              | 1,2,3,4 |
| CL = 6 / CWL = 5                         | t <sub>CK(AVG)</sub> | 2.5       | 3.3     | ns              | 1,2,3   |
| Supported CL Settings                    |                      | 6         |         | n <sub>CK</sub> |         |
| Supported CWL Settings                   |                      | 5         |         | n <sub>CK</sub> |         |

[ Table 49 ] DDR3-1066 Speed Bins

| Speed                                    |                  | DDR3-1066 |         | DDR3-1066 |         | Units           | Note      |
|--|------------------|-----------|---------|-----------|---------|-----------------|-----------|
| CL-nRCD-nRP                              |                  | 7 - 7 - 7 |         | 8 - 8 - 8 |         |                 |           |
| Parameter                                | Symbol           | min       | max     | min       | max     |                 |           |
| Internal read command to first data      | t <sub>AA</sub>  | 13.125    | 20      | 15        | 20      | ns              |           |
| ACT to internal read or write delay time | t <sub>RCD</sub> | 13.125    | -       | 15        | -       | ns              |           |
| PRE command period                       | t <sub>RP</sub>  | 13.125    | -       | 15        | -       | ns              |           |
| ACT to ACT or REF command period         | t <sub>RC</sub>  | 50.625    | -       | 52.5      | -       | ns              |           |
| ACT to PRE command period                | t <sub>RAS</sub> | 37.5      | 9*tREFI | 37.5      | 9*tREFI | ns              | 8         |
| CL = 5                                   | CWL = 5          | Reserved  |         | Reserved  |         | ns              | 1,2,3,4,6 |
|  | CWL = 6          | Reserved  |         | Reserved  |         | ns              | 4         |
| CL = 6                                   | CWL = 5          | 2.5       | 3.3     | 2.5       | 3.3     | ns              | 1,2,3,6   |
|  | CWL = 6          | Reserved  |         | Reserved  |         | ns              | 1,2,3,4   |
| CL = 7                                   | CWL = 5          | Reserved  |         | Reserved  |         | ns              | 4         |
|  | CWL = 6          | 1.875     | <2.5    | Reserved  |         | ns              | 1,2,3,4   |
| CL = 8                                   | CWL = 5          | Reserved  |         | Reserved  |         | ns              | 4         |
|  | CWL = 6          | 1.875     | <2.5    | 1.875     | <2.5    | ns              | 1,2,3     |
| Supported CL Settings                    |                  | 6,7,8     |         | 6,8       |         | n <sub>CK</sub> |           |
| Supported CWL Settings                   |                  | 5,6       |         | 5,6       |         | n <sub>CK</sub> |           |

[ Table 50 ] DDR3-1333 Speed Bins

| Speed                                    |           | DDR3-1333     |          | DDR3-1333 |          | Units  | Note |                 |  |
|--|-----------|---------------|----------|-----------|----------|--------|------|-----------------|--|
| CL-nRCD-nRP                              |           | 8 - 8 - 8     |          | 9 - 9 - 9 |          |        |      |                 |  |
| Parameter                                | Symbol    | min           | max      | min       | max      |        |      |                 |  |
| Internal read command to first data      | $t_{AA}$  | 12            | 20       | 13.5      | 20       | ns     |      |                 |  |
| ACT to internal read or write delay time | $t_{RCD}$ | 12            | -        | 13.5      | -        | ns     |      |                 |  |
| PRE command period                       | $t_{RP}$  | 12            | -        | 13.5      | -        | ns     |      |                 |  |
| ACT to ACT or REF command period         | $t_{RC}$  | 48            | -        | 49.5      | -        | ns     |      |                 |  |
| ACT to PRE command period                | $t_{RAS}$ | 36            | 9*tREFI  | 36        | 9*tREFI  | ns     | 8    |                 |  |
| CL = 5                                   | CWL = 5   | $t_{CK(AVG)}$ | 2.5      | 3.3       | Reserved |        | ns   | 1,2,3,4,7       |  |
|  | CWL = 6,7 | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 4               |  |
| CL = 6                                   | CWL = 5   | $t_{CK(AVG)}$ | 2.5      | 3.3       | 2.5      | 3.3    | ns   | 1,2,3,7         |  |
|  | CWL = 6   | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 1,2,3,4,7       |  |
|  | CWL = 7   | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 4               |  |
| CL = 7                                   | CWL = 5   | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 4               |  |
|  | CWL = 6   | $t_{CK(AVG)}$ | 1.875    | <2.5      | Reserved |        | ns   | 1,2,3,4,7       |  |
|  | CWL = 7   | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 1,2,3,4         |  |
| CL = 8                                   | CWL = 5   | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 4               |  |
|  | CWL = 6   | $t_{CK(AVG)}$ | 1.875    | <2.5      | 1.875    | <2.5   | ns   | 1,2,3,7         |  |
|  | CWL = 7   | $t_{CK(AVG)}$ | 1.5      | <1.875    | Reserved |        | ns   | 1,2,3,4         |  |
| CL = 9                                   | CWL = 5,6 | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 4               |  |
|  | CWL = 7   | $t_{CK(AVG)}$ | 1.5      | <1.875    | 1.5      | <1.875 | ns   | 1,2,3,4         |  |
| CL = 10                                  | CWL = 5,6 | $t_{CK(AVG)}$ | Reserved |           | Reserved |        | ns   | 4               |  |
|  | CWL = 7   | $t_{CK(AVG)}$ | 1.5      | <1.875    | 1.5      | <1.875 | ns   | 1,2,3           |  |
| Supported CL Settings                    |           |               |          | 5,6,7,8,9 |          | 6,8,9  |      | n <sub>CK</sub> |  |
| Supported CWL Settings                   |           |               |          | 5,6,7     |          | 5,6,7  |      | n <sub>CK</sub> |  |

**NOTES:**

Absolute Specification (TOPER;VDDQ=VDD=1.5V +/- 0.075V);

- The CL setting and CWL setting result in t<sub>CK(AVG)</sub>.MIN and t<sub>CK(AVG)</sub>.MAX requirements. When making a selection of t<sub>CK(AVG)</sub>, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- t<sub>CK(AVG)</sub>.MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard t<sub>CK(AVG)</sub> value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / t<sub>CK(AVG)</sub> [ns], rounding up to the next 'Supported CL'.
- t<sub>CK(AVG)</sub>.MAX limits: Calculate t<sub>CK(AVG)</sub> = tAA.MAX / CLSELECTED and round the resulting t<sub>CK(AVG)</sub> down to the next valid speed bin limit (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is t<sub>CK(AVG)</sub>.MAX corresponding to CLSELECTED.
- 'Reserved' settings are not allowed. User must program a different value.
- 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
- Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- tREFI depends on TOPER

## 13.0 Timing Parameters by Speed Grade

[ Table 51 ] Timing Parameters by Speed Bin

| Speed  |                     | DDR3-800   |                                    | DDR3-1066                          |                                    | DDR3-1333                          |                                    | Units         | Note      |
|--|---------------------|--|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|---------------|-----------|
| Parameter  | Symbol              | MIN  | MAX                                | MIN                                | MAX                                | MIN                                | MAX                                |               |           |
| <b>Clock Timing</b>  |                     |  |                                    |                                    |                                    |                                    |                                    |               |           |
| Minimum Clock Cycle Time (DLL off mode)  | $t_{CK(DLL\_OFF)}$  | 8  | -                                  | 8                                  | -                                  | 8                                  | -                                  | ns            | 6         |
| Average Clock Period   | $t_{CK(ave)}$       | See Speed Bins Table   |                                    |                                    |                                    |                                    |                                    | ps            | f         |
| Clock Period   | $t_{CK(abs)}$       | $t_{CK(ave)min} + t_{JIT(per)min}$   | $t_{CK(ave)max} + t_{JIT(per)max}$ | $t_{CK(ave)min} + t_{JIT(per)min}$ | $t_{CK(ave)max} + t_{JIT(per)max}$ | $t_{CK(ave)min} + t_{JIT(per)min}$ | $t_{CK(ave)max} + t_{JIT(per)max}$ | ps            |           |
| Average high pulse width   | $t_{CH(ave)}$       | 0.47   | 0.53                               | 0.47                               | 0.53                               | 0.47                               | 0.53                               | $t_{CK(ave)}$ | f         |
| Average low pulse width  | $t_{CL(ave)}$       | 0.47   | 0.53                               | 0.47                               | 0.53                               | 0.47                               | 0.53                               | $t_{CK(ave)}$ | f         |
| Clock Period Jitter  | $t_{JIT(per)}$      | -100   | 100                                | -90                                | 90                                 | -80                                | 80                                 | ps            |           |
| Clock Period Jitter during DLL locking period  | $t_{JIT(per, lck)}$ | -90  | 90                                 | -80                                | 80                                 | -70                                | 70                                 | ps            |           |
| Cycle to Cycle Period Jitter   | $t_{JIT(cc)}$       | 200  |                                    | 180                                |                                    | 160                                |                                    | ps            |           |
| Cycle to Cycle Period Jitter during DLL locking period                               | $t_{JIT(cc, lck)}$  | 180  |                                    | 160                                |                                    | 140                                |                                    | ps            |           |
| Cumulative error across 2 cycles   | $t_{ERR(2per)}$     | -147   | 147                                | -132                               | 132                                | -118                               | 118                                | ps            |           |
| Cumulative error across 3 cycles   | $t_{ERR(3per)}$     | -175   | 175                                | -157                               | 157                                | -140                               | 140                                | ps            |           |
| Cumulative error across 4 cycles   | $t_{ERR(4per)}$     | -194   | 194                                | -175                               | 175                                | -155                               | 155                                | ps            |           |
| Cumulative error across 5 cycles   | $t_{ERR(5per)}$     | -209   | 209                                | -188                               | 188                                | -168                               | 168                                | ps            |           |
| Cumulative error across 6 cycles   | $t_{ERR(6per)}$     | -222   | 222                                | -200                               | 200                                | -177                               | 177                                | ps            |           |
| Cumulative error across 7 cycles   | $t_{ERR(7per)}$     | -232   | 232                                | -209                               | 209                                | -186                               | 186                                | ps            |           |
| Cumulative error across 8 cycles   | $t_{ERR(8per)}$     | -241   | 241                                | -217                               | 217                                | -193                               | 193                                | ps            |           |
| Cumulative error across 9 cycles   | $t_{ERR(9per)}$     | -249   | 249                                | -224                               | 224                                | -200                               | 200                                | ps            |           |
| Cumulative error across 10 cycles  | $t_{ERR(10per)}$    | -257   | 257                                | -231                               | 231                                | -205                               | 205                                | ps            |           |
| Cumulative error across 11 cycles  | $t_{ERR(11per)}$    | -263   | 263                                | -237                               | 237                                | -210                               | 210                                | ps            |           |
| Cumulative error across 12 cycles  | $t_{ERR(12per)}$    | -269   | 269                                | -242                               | 242                                | -215                               | 215                                | PS            |           |
| Cumulative error across n = 13, 14 ... 49, 50 cycles                                 | $t_{ERR(nper)}$     | $t_{ERR(nper)min} = (1 + 0.68\ln(n)) \cdot t_{JIT(per)min}$<br>$t_{ERR(nper)max} = (1 + 0.68\ln(n)) \cdot t_{JIT(per)max}$ |                                    |                                    |                                    |                                    |                                    |               |           |
| Absolute clock HIGH pulse width  | $t_{CH(abs)}$       | 0.43   |                                    | 0.43                               |                                    | 0.43                               |                                    | $t_{CK(ave)}$ | 25        |
| Absolute clock Low pulse width   | $t_{CL(abs)}$       | 0.43   |                                    | 0.43                               |                                    | 0.43                               |                                    | $t_{CK(ave)}$ | 26        |
| <b>Data Timing</b>   |                     |  |                                    |                                    |                                    |                                    |                                    |               |           |
| DQS, $\overline{DQS}$ to DQ skew, per group, per access                              | $t_{DQSQ}$          | -  | 200                                | -                                  | 150                                | -                                  | 125                                | ps            | 12,13     |
| DQ output hold time from DQS, $\overline{DQS}$                                       | $t_{QH}$            | 0.38   | -                                  | 0.38                               | -                                  | 0.38                               | -                                  | $t_{CK(ave)}$ | 12,13     |
| DQ low-impedance time from CK, $\overline{CK}$                                       | $t_{LZ(DQ)}$        | -800   | 400                                | -600                               | 300                                | -500                               | 250                                | ps            | 13,14, a  |
| DQ high-impedance time from CK, $\overline{CK}$                                      | $t_{HZ(DQ)}$        | -  | 400                                | -                                  | 300                                | -                                  | 250                                | ps            | 13,14, a  |
| Data setup time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels         | $t_{DS(base)}$      | 75   | -                                  | 25                                 | -                                  | -10                                | -                                  | ps            | d, 17     |
| Data hold time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels          | $t_{DH(base)}$      | 150  | -                                  | 100                                | -                                  | 65                                 | -                                  | ps            | d, 17     |
| <b>Data Strobe Timing</b>  |                     |  |                                    |                                    |                                    |                                    |                                    |               |           |
| DQS, $\overline{DQS}$ READ Preamble  | $t_{RPRE}$          | 0.9  | -                                  | 0.9                                | -                                  | 0.9                                | -                                  | $t_{CK}$      | 13, 19, b |
| DQS, $\overline{DQS}$ differential READ Postamble                                    | $t_{RPST}$          | 0.3  | NOTE1                              | 0.3                                | NOTE1                              | 0.3                                | NOTE1                              | $t_{CK}$      | 11, 13, b |
| DQS, $\overline{DQS}$ output high time   | $t_{QSH}$           | 0.38   | -                                  | 0.38                               | -                                  | 0.4                                | -                                  | $t_{CK(ave)}$ | 13, b     |
| DQS, $\overline{DQS}$ output low time  | $t_{QSL}$           | 0.38   | -                                  | 0.38                               | -                                  | 0.4                                | -                                  | $t_{CK(ave)}$ | 13, b     |
| DQS, $\overline{DQS}$ WRITE Preamble   | $t_{WPRE}$          | 0.9  | -                                  | 0.9                                | -                                  | 0.9                                | -                                  | $t_{CK}$      | 1         |
| DQS, $\overline{DQS}$ WRITE Postamble  | $t_{WPST}$          | 0.3  | -                                  | 0.3                                | -                                  | 0.3                                | -                                  | $t_{CK}$      | 1         |
| DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$ | $t_{DQSCK}$         | -400   | 400                                | -300                               | 300                                | -255                               | 255                                | ps            | 12,13     |
| DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)                      | $t_{LZ(DQS)}$       | -800   | 400                                | -600                               | 300                                | -500                               | 250                                | ps            | 12,13,14  |
| DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)                  | $t_{HZ(DQS)}$       | -  | 400                                | -                                  | 300                                | -                                  | 250                                | ps            | 12,13,14  |
| DQS, $\overline{DQS}$ differential input low pulse width                             | $t_{DQSL}$          | 0.4  | 0.6                                | 0.4                                | 0.6                                | 0.4                                | 0.6                                | $t_{CK}$      |           |
| DQS, $\overline{DQS}$ differential input high pulse width                            | $t_{DQSH}$          | 0.4  | 0.6                                | 0.4                                | 0.6                                | 0.4                                | 0.6                                | $t_{CK}$      |           |
| DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge                 | $t_{DQSS}$          | -0.25  | 0.25                               | -0.25                              | 0.25                               | -0.25                              | 0.25                               | $t_{CK(ave)}$ | c         |
| DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge     | $t_{DSS}$           | 0.2  | -                                  | 0.2                                | -                                  | 0.2                                | -                                  | $t_{CK(ave)}$ | c         |
| DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge      | $t_{DSH}$           | 0.2  | -                                  | 0.2                                | -                                  | 0.2                                | -                                  | $t_{CK(ave)}$ | c         |

[ Table 51 ] Timing Parameters by Speed Bin (Cont.)

| Speed   |                | DDR3-800                                |        | DDR3-1066                        |        | DDR3-1333                        |        | Units         | Note  |
|---|----------------|---|--------|----------------------------------|--------|----------------------------------|--------|---------------|-------|
| Parameter   | Symbol         | MIN                                     | MAX    | MIN                              | MAX    | MIN                              | MAX    |               |       |
| <b>Command and Address Timing</b>   |                |   |        |                                  |        |                                  |        |               |       |
| DLL locking time  | $t_{DLLK}$     | 512                                     | -      | 512                              | -      | 512                              | -      | nCK           |       |
| internal READ Command to PRECHARGE Command delay  | $t_{RTP}$      | max<br>( $4t_{CK}, 7.5ns$ )             | -      | max<br>( $4t_{CK}, 7.5ns$ )      | -      | max<br>( $4t_{CK}, 7.5ns$ )      | -      |               | e     |
| Delay from start of internal write transaction to internal read command                                 | $t_{WTR}$      | max<br>( $4t_{CK}, 7.5ns$ )             | -      | max<br>( $4t_{CK}, 7.5ns$ )      | -      | max<br>( $4t_{CK}, 7.5ns$ )      | -      |               | e, 18 |
| WRITE recovery time   | $t_{WR}$       | 15                                      | -      | 15                               | -      | 15                               | -      | ns            | e     |
| Mode Register Set command cycle time  | $t_{MRD}$      | 4                                       | -      | 4                                | -      | 4                                | -      | $t_{CK(ave)}$ |       |
| Mode Register Set command update delay  | $t_{MOD}$      | max<br>( $12t_{CK}, 15ns$ )             | -      | max<br>( $12t_{CK}, 15ns$ )      | -      | max<br>( $12t_{CK}, 15ns$ )      | -      |               |       |
| CAS# to CAS# command delay  | $t_{CCD}$      | 4                                       | -      | 4                                | -      | 4                                | -      | nCK           |       |
| Auto precharge write recovery + precharge time  | $t_{DAL(min)}$ | WR + roundup ( $t_{RP} / t_{CK(AVG)}$ ) |        |                                  |        |                                  |        | nCK           |       |
| Multi-Purpose Register Recovery Time  | $t_{MPRR}$     | 1                                       | -      | 1                                | -      | 1                                | -      | nCK           |       |
| ACTIVE to PRECHARGE command period  | $t_{RAS}$      | 37.5                                    | 70,000 | 37.5                             | 70,000 | 36                               | 70,000 | ns            | e     |
| ACTIVE to ACTIVE command period for 1KB page size   | $t_{RRD}$      | max<br>( $4t_{CK}, 10ns$ )              | -      | max<br>( $4t_{CK}, 7.5ns$ )      | -      | max<br>( $4t_{CK}, 6ns$ )        | -      |               | e     |
| ACTIVE to ACTIVE command period for 2KB page size   | $t_{RRD}$      | max<br>( $4t_{CK}, 10ns$ )              | -      | max<br>( $4t_{CK}, 10ns$ )       | -      | max<br>( $4t_{CK}, 7.5ns$ )      | -      |               | e     |
| Four activate window for 1KB page size  | $t_{FAW}$      | 40                                      | -      | 37.5                             | -      | 30                               | -      | ns            | e     |
| Four activate window for 2KB page size  | $t_{FAW}$      | 50                                      | -      | 50                               | -      | 45                               | -      | ns            | e     |
| Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH(ac)}$ / $V_{IL(ac)}$ levels  | $t_{IS(base)}$ | 200                                     | -      | 125                              | -      | 65                               | -      | ps            | b, 16 |
| Command and Address hold time from CK, $\overline{CK}$ referenced to $V_{IH(ac)}$ / $V_{IL(ac)}$ levels | $t_{IH(base)}$ | 275                                     | -      | 200                              | -      | 140                              | -      | ps            | b, 16 |
| <b>Refresh Timing</b>   |                |   |        |                                  |        |                                  |        |               |       |
| 512Mb REFRESH to REFRESH OR REFRESH to ACTIVE command interval  | $t_{RFC}$      | 90                                      | -      | 90                               | -      | 90                               | -      | ns            |       |
| 1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval  | $t_{RFC}$      | 110                                     | -      | 110                              | -      | 110                              | -      | ns            |       |
| 2Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval  | $t_{RFC}$      | 160                                     | -      | 160                              | -      | 160                              | -      | ns            |       |
| 4Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval  | $t_{RFC}$      | 300                                     | -      | 300                              | -      | 300                              | -      | ns            |       |
| 8Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval  | $t_{RFC}$      | 350                                     | -      | 350                              | -      | 350                              | -      | ns            |       |
| Average periodic refresh interval ( $0^{\circ}C \leq TCASE \leq 85^{\circ}C$ )                          | $t_{REFI}$     | 7.8                                     |        | 7.8                              |        | 7.8                              |        | us            |       |
| Average periodic refresh interval ( $85^{\circ}C \leq TCASE \leq 95^{\circ}C$ )                         | $t_{REFI}$     | 3.9                                     |        | 3.9                              |        | 3.9                              |        | us            |       |
| <b>Calibration Timing</b>   |                |   |        |                                  |        |                                  |        |               |       |
| Power-up and RESET calibration time   | $t_{ZQinit}$   | 512                                     | -      | 512                              | -      | 512                              | -      | $t_{CK}$      |       |
| Normal operation Full calibration time  | $t_{ZQoper}$   | 256                                     | -      | 256                              | -      | 256                              | -      | $t_{CK}$      |       |
| Normal operation short calibration time   | $t_{ZQCS}$     | 64                                      | -      | 64                               | -      | 64                               | -      | $t_{CK}$      | 23    |
| <b>Reset Timing</b>   |                |   |        |                                  |        |                                  |        |               |       |
| Exit Reset from CKE HIGH to a valid command   | $t_{XPR}$      | max( $5t_{CK}, t_{RFC} + 10ns$ )        | -      | max( $5t_{CK}, t_{RFC} + 10ns$ ) | -      | max( $5t_{CK}, t_{RFC} + 10ns$ ) | -      |               |       |
| <b>Self Refresh Timing</b>  |                |   |        |                                  |        |                                  |        |               |       |
| Exit Self Refresh to commands not requiring a locked DLL  | $t_{XS}$       | max( $5t_{CK}, t_{RFC} + 10ns$ )        | -      | max( $5t_{CK}, t_{RFC} + 10ns$ ) | -      | max( $5t_{CK}, t_{RFC} + 10ns$ ) | -      |               |       |
| Exit Self Refresh to commands requiring a locked DLL  | $t_{XSDLL}$    | $t_{DLLK(min)}$                         | -      | $t_{DLLK(min)}$                  | -      | $t_{DLLK(min)}$                  | -      | $t_{CK}$      |       |
| Minimum CKE low width for Self refresh entry to exit timing   | $t_{CKESR}$    | $t_{CKE(min)} + 1t_{CK}$                | -      | $t_{CKE(min)} + 1t_{CK}$         | -      | $t_{CKE(min)} + 1t_{CK}$         | -      |               |       |
| Valid Clock Requirement after Self Refresh Entry (SRE)  | $t_{CKSRE}$    | max( $5t_{CK}, 10ns$ )                  | -      | max( $5t_{CK}, 10ns$ )           | -      | max( $5t_{CK}, 10ns$ )           | -      |               |       |
| Valid Clock Requirement before Self Refresh Exit (SRX)  | $t_{CKSRX}$    | max( $5t_{CK}, 10ns$ )                  | -      | max( $5t_{CK}, 10ns$ )           | -      | max( $5t_{CK}, 10ns$ )           | -      |               |       |

[ Table 51 ] Timing Parameters by Speed Bin (Cont.)

| Speed  |               | DDR3-800                     |                    | DDR3-1066                     |                    | DDR3-1333                     |                    | Units         | Note  |
|--|---------------|------------------------------|--------------------|-------------------------------|--------------------|-------------------------------|--------------------|---------------|-------|
| Parameter  | Symbol        | MIN                          | MAX                | MIN                           | MAX                | MIN                           | MAX                |               |       |
| <b>Power Down Timing</b>   |               |                              |                    |                               |                    |                               |                    |               |       |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | $t_{XP}$      | max<br>( $3t_{CK}, 7.5ns$ )  | -                  | max<br>( $3t_{CK}, 7.5ns$ )   | -                  | max<br>( $3t_{CK}, 6ns$ )     | -                  |               |       |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL   | $t_{XPDLL}$   | max<br>( $10t_{CK}, 24ns$ )  | -                  | max<br>( $10t_{CK}, 24ns$ )   | -                  | max<br>( $10t_{CK}, 24ns$ )   | -                  |               | 2     |
| CKE minimum pulse width  | $t_{CKE}$     | max<br>( $3t_{CK}, 7.5ns$ )  | -                  | max<br>( $3t_{CK}, 5.625ns$ ) | -                  | max<br>( $3t_{CK}, 5.625ns$ ) | -                  |               |       |
| Command pass disable delay   | $t_{CPDED}$   | 1                            | -                  | 1                             | -                  | 1                             | -                  | nCK           |       |
| Power Down Entry to Exit Timing  | $t_{PD}$      | $t_{CKE}(min)$               | $9 \cdot t_{REFI}$ | $t_{CKE}(min)$                | $9 \cdot t_{REFI}$ | $t_{CKE}(min)$                | $9 \cdot t_{REFI}$ | $t_{CK}$      | 15    |
| Timing of ACT command to Power Down entry  | $t_{ACTPDEN}$ | 1                            | -                  | 1                             | -                  | 1                             | -                  | nCK           | 20    |
| Timing of PRE command to Power Down entry  | $t_{PRPDEN}$  | 1                            | -                  | 1                             | -                  | 1                             | -                  | nCK           | 20    |
| Timing of RD/RDA command to Power Down entry   | $t_{RDPDEN}$  | RL + 4 + 1                   | -                  | RL + 4 + 1                    | -                  | RL + 4 + 1                    | -                  |               |       |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)  | $t_{WRPDEN}$  | WL + 4 + ( $t_{WR}/t_{CK}$ ) | -                  | WL + 4 + ( $t_{WR}/t_{CK}$ )  | -                  | WL + 4 + ( $t_{WR}/t_{CK}$ )  | -                  | nCK           | 9     |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)   | $t_{WRAPDEN}$ | WL + 4 + WR + 1              | -                  | WL + 4 + WR + 1               | -                  | WL + 4 + WR + 1               | -                  | nCK           | 10    |
| Timing of WR command to Power Down entry (BL4MRS)  | $t_{WRPDEN}$  | WL + 2 + ( $t_{WR}/t_{CK}$ ) | -                  | WL + 2 + ( $t_{WR}/t_{CK}$ )  | -                  | WL + 2 + ( $t_{WR}/t_{CK}$ )  | -                  | nCK           | 9     |
| Timing of WRA command to Power Down entry (BL4MRS)   | $t_{WRAPDEN}$ | WL + 2 + WR + 1              | -                  | WL + 2 + WR + 1               | -                  | WL + 2 + WR + 1               | -                  | nCK           | 10    |
| Timing of REF command to Power Down entry  | $t_{REFPDEN}$ | 1                            | -                  | 1                             | -                  | 1                             | -                  |               | 20,21 |
| Timing of MRS command to Power Down entry  | $t_{MRSPDEN}$ | $t_{MOD}(min)$               | -                  | $t_{MOD}(min)$                | -                  | $t_{MOD}(min)$                | -                  | $t_{CK}$      |       |
| <b>ODT Timing</b>  |               |                              |                    |                               |                    |                               |                    |               |       |
| ODT high time without write command or with write command and BC4  | ODTH4         | 4                            | -                  | 4                             | -                  | 4                             | -                  | nCK           |       |
| ODT high time with Write command and BL8   | ODTH8         | 6                            | -                  | 6                             | -                  | 6                             | -                  | nCK           |       |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen)  | $t_{AONPD}$   | 1                            | 9                  | 1                             | 9                  | 1                             | 9                  | ns            |       |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen)   | $t_{AOFPD}$   | 1                            | 9                  | 1                             | 9                  | 1                             | 9                  | ns            |       |
| ODT turn-on  | $t_{AON}$     | -400                         | 400                | -300                          | 30                 | -250                          | 250                | ps            | 7,12  |
| RTT_NOM and RTT_WR turn-off time from ODTLoff reference  | $t_{AOF}$     | 0.3                          | 0.7                | 0.3                           | 0.7                | 0.3                           | 0.7                | $t_{CK}(avg)$ | 8,12  |
| RTT dynamic change skew  | $t_{ADC}$     | 0.3                          | 0.7                | 0.3                           | 0.7                | 0.3                           | 0.7                | $t_{CK}(avg)$ | 12    |
| <b>Write Leveling Timing</b>   |               |                              |                    |                               |                    |                               |                    |               |       |
| First DQS pulse rising edge after tDQSS margining mode is programmed   | $t_{WLMRD}$   | 40                           | -                  | 40                            | -                  | 40                            | -                  | $t_{CK}$      | 3     |
| DQS/DQS delay after tDQSS margining mode is programmed   | $t_{WLDQSEN}$ | 25                           | -                  | 25                            | -                  | 25                            | -                  | $t_{CK}$      | 3     |
| Setup time for tDQSS latch   | $t_{WLS}$     | 325                          | -                  | 245                           | -                  | 195                           | -                  | ps            |       |
| Hold time of tDQSS latch   | $t_{WLH}$     | 325                          | -                  | 245                           | -                  | 195                           | -                  | ps            |       |
| Write leveling output delay  | $t_{WLO}$     | 0                            | 9                  | 0                             | 9                  | 0                             | 9                  | ns            |       |
| Write leveling output error  | $t_{WLOE}$    | 0                            | 2                  | 0                             | 2                  | 0                             | 2                  | ns            |       |

## Jitter Notes

### Specific Note a

When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{ERR}(mper),act$  of the input clock, where  $2 \leq m \leq 12$ . (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has  $t_{ERR}(mper),act,min} = -172$  ps and  $t_{ERR}(mper),act,max} = +193$  ps, then  $t_{DQSCK,min}(derated) = t_{DQSCK,min} - t_{ERR}(mper),act,max} = -400$  ps - 193 ps = -593 ps and  $t_{DQSCK,max}(derated) = t_{DQSCK,max} - t_{ERR}(mper),act,min} = 400$  ps + 172 ps = +572 ps. Similarly,  $t_{LZ}(DQ)$  for DDR3-800 derates to  $t_{LZ}(DQ),min(derated) = -800$  ps - 193 ps = -993 ps and  $t_{LZ}(DQ),max(derated) = 400$  ps + 172 ps = +572 ps. (Caution on the min/max usage!)

Note that  $t_{ERR}(mper),act,min}$  is the minimum measured value of  $t_{ERR}(nper)$  where  $2 \leq n \leq 12$ , and  $t_{ERR}(mper),act,max}$  is the maximum measured value of  $t_{ERR}(nper)$  where  $2 \leq n \leq 12$ .

### Specific Note b

When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT}(per),act$  of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has  $t_{CK}(avg),act} = 2500$  ps,  $t_{JIT}(per),act,min} = -72$  ps and  $t_{JIT}(per),act,max} = +93$  ps, then  $t_{RPRE,min}(derated) = t_{RPRE,min} + t_{JIT}(per),act,min} = 0.9 \times t_{CK}(avg),act} + t_{JIT}(per),act,min} = 0.9 \times 2500$  ps - 72 ps = +2178 ps. Similarly,  $t_{QH,min}(derated) = t_{QH,min} + t_{JIT}(per),act,min} = 0.38 \times t_{CK}(avg),act} + t_{JIT}(per),act,min} = 0.38 \times 2500$  ps - 72 ps = +878 ps. (Caution on the min/max usage!)

### Specific Note c

These parameters are measured from a data strobe signal ( $DQS(L/U)$ ,  $\overline{DQS}(L/U)$ ) crossing to its respective clock signal ( $CK$ ,  $\overline{CK}$ ) crossing. The spec values are not affected by the amount of clock jitter applied (i.e.  $t_{JIT}(per)$ ,  $t_{JIT}(cc)$ , etc.), as these are relative to the clock signal crossing.

That is, these parameters should be met whether clock jitter is present or not.

### Specific Note d

These parameters are measured from a data signal ( $DM(L/U)$ ,  $DQ(L/U)0$ ,  $DQ(L/U)1$ , etc.) transition edge to its respective data strobe signal ( $DQS(L/U)$ ,  $\overline{DQS}(L/U)$ ) crossing.

### Specific Note e

For these parameters, the DDR3 SDRAM device supports  $t_{nPARAM} [nCK] = RU \{ t_{PARAM} [ns] / t_{CK}(avg) [ns] \}$ , which is in clock cycles, assuming all input clock jitter specifications are satisfied.

For example, the device will support  $t_{nRP} = RU \{ t_{RP} / t_{CK}(avg) \}$ , which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which  $t_{RP} = 15$ ns, the device will support  $t_{nRP} = RU \{ t_{RP} / t_{CK}(avg) \} = 6$ , as long as the input clock jitter specifications are met, i.e. Precharge command at  $T_m$  and Active command at  $T_m+6$  is valid even if  $(T_m+6 - T_m)$  is less than 15ns due to input clock jitter.

## Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON see "Device Operation"
8. For definition of RTT turn-off time tAOF see "Device Operation".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0
11. The maximum postamble is bound by tHZDQS(max)
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter <TBD> for definition and measurement method.
15. tREFI depends on TOPER
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK,  $\overline{\text{CK}}$  differential slew rate, Note for DQ and DM signals, VREF(DC) = VrefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC). See "Address/ Command Setup, Hold and Derating" on page 53.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS,  $\overline{\text{DQS}}$  differential slew rate. Note for DQ and DM signals, VREF(DC)= VrefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC). See "Data Setup, Hold and Slew Rate Derating" on page 59.
18. Start of internal write transaction is defined as follows ;  
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.  
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL  
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
19. The maximum preamble is bound by tLZDQS(max)
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation".
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other applicationspecific One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:  

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$
- where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) For example, if TSens = 1.5% /°C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:  

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$
24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

**Address / Command Setup, Hold and Derating:**

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 53) to the ΔtIS and ΔtIH derating value (see Table 54) respectively.

Example: tIS (total setup time) = tIS(base) + ΔtIS Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value (see Figure 23). If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 25).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value (see Figure 24). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see Figure 26).

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see Table 55).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in Table 54, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[ Table 53 ] ADD/CMD Setup and Hold Base-Values for 1V/ns

| [ps]            | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | reference |
|-----------------|----------|-----------|-----------|-----------|-----------|
| tIS(base)       | 200      | 125       | 65        | TBD       | VIH/L(ac) |
| tIH(base)       | 275      | 200       | 140       | TBD       | VIH/L(dc) |
| tIS(base)-AC150 | -        | -         | 65+125    | TBD+125   | VIH/L(ac) |

**Note :** AC/DC referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate

**Note :** The tIS(base)-AC150 specifications are further adjusted to add an additional 100ps of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mv-150mV)/1 V/ns].

[ Table 54 ] Derating values DDR3-800/1066 tIS/tIH-ac/dc based

| ΔtIS, ΔtIH Derating [ps] AC/DC based<br>AC175 Threshold -> VIH(ac) = VREF(dc) + 175mV, VIL(ac) = VREF(dc) - 175mV |     |                                |      |          |      |          |      |          |      |          |      |         |      |         |      |         |      |
|---|-----|--------------------------------|------|----------|------|----------|------|----------|------|----------|------|---------|------|---------|------|---------|------|
|   |     | CLK,CLK Differential Slew Rate |      |          |      |          |      |          |      |          |      |         |      |         |      |         |      |
|   |     | 4.0 V/ns                       |      | 3.0 V/ns |      | 2.0 V/ns |      | 1.8 V/ns |      | 1.6 V/ns |      | 1.4V/ns |      | 1.2V/ns |      | 1.0V/ns |      |
|   |     | ΔtIS                           | ΔtIH | ΔtIS     | ΔtIH | ΔtIS     | ΔtIH | ΔtIS     | ΔtIH | ΔtIS     | ΔtIH | ΔtIS    | ΔtIH | ΔtIS    | ΔtIH | ΔtIS    | ΔtIH |
| CMD/<br>ADD<br>Slew<br>rate<br>V/ns   | 2.0 | 88                             | 50   | 88       | 50   | 88       | 50   | 96       | 58   | 104      | 66   | 112     | 74   | 120     | 84   | 128     | 100  |
|   | 1.5 | 59                             | 34   | 59       | 34   | 59       | 34   | 67       | 42   | 75       | 50   | 83      | 58   | 91      | 68   | 99      | 74   |
|   | 1.0 | 0                              | 0    | 0        | 0    | 0        | 0    | 8        | 8    | 16       | 16   | 24      | 24   | 32      | 34   | 40      | 50   |
|   | 0.9 | -2                             | -4   | -2       | -4   | -2       | -4   | 6        | 4    | 14       | 12   | 20      | 20   | 30      | 30   | 38      | 46   |
|   | 0.8 | -6                             | -10  | -6       | -10  | -6       | -10  | 2        | -2   | 10       | 6    | 13      | 14   | 26      | 24   | 34      | 40   |
|   | 0.7 | -11                            | -16  | -11      | -16  | -11      | -16  | -3       | -8   | 5        | 0    | 13      | 8    | 21      | 18   | 29      | 34   |
|   | 0.6 | -17                            | -26  | -17      | -26  | -17      | -26  | -9       | -18  | -1       | -10  | 7       | -2   | 15      | 8    | 23      | 24   |
|   | 0.5 | -35                            | -40  | -35      | -40  | -35      | -40  | -27      | -32  | -19      | -24  | -11     | -16  | -2      | -6   | 6       | 10   |
|   | 0.4 | -62                            | -60  | -62      | -60  | -60      | -60  | -54      | -52  | -46      | -44  | -38     | -36  | -30     | -26  | -22     | -10  |

[ Table 55 ] Derating values DDR3-1333/1600 tIS/tIH-ac/dc based - Alternate AC150 Threshold

| $\Delta tIS, \Delta tIH$ Derating [ps] AC/DC based<br>Alternate AC150 Threshold $\rightarrow V_{IH}(ac) = V_{REF}(dc) + 150mV, V_{IL}(ac) = V_{REF}(dc) - 150mV$ |     |  |              |              |              |              |              |              |              |              |              |              |              |              |              |              |              |
|--|-----|--|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
|  |     | CLK, $\overline{CLK}$ Differential Slew Rate |              |              |              |              |              |              |              |              |              |              |              |              |              |              |              |
|  |     | 4.0 V/ns                                     |              | 3.0 V/ns     |              | 2.0 V/ns     |              | 1.8 V/ns     |              | 1.6 V/ns     |              | 1.4V/ns      |              | 1.2V/ns      |              | 1.0V/ns      |              |
|  |     | $\Delta tIS$                                 | $\Delta tIH$ | $\Delta tIS$ | $\Delta tIH$ | $\Delta tIS$ | $\Delta tIH$ | $\Delta tIS$ | $\Delta tIH$ | $\Delta tIS$ | $\Delta tIH$ | $\Delta tIS$ | $\Delta tIH$ | $\Delta tIS$ | $\Delta tIH$ | $\Delta tIS$ | $\Delta tIH$ |
| CMD/<br>ADD<br>Slew<br>rate<br>V/ns  | 2.0 | 70   | 50           | 75           | 50           | 75           | 50           | 83           | 58           | 91           | 66           | 99           | 74           | 107          | 84           | 115          | 100          |
|  | 1.5 | 50   | 34           | 50           | 34           | 50           | 34           | 58           | 42           | 66           | 50           | 74           | 58           | 82           | 68           | 90           | 84           |
|  | 1.0 | 0  | 0            | 0            | 0            | 0            | 0            | 8            | 8            | 16           | 16           | 24           | 24           | 32           | 34           | 40           | 50           |
|  | 0.9 | 0  | -4           | 0            | -4           | 0            | -4           | 8            | 4            | 16           | 12           | 24           | 20           | 32           | 30           | 40           | 46           |
|  | 0.8 | 0  | -10          | 0            | -10          | 0            | -10          | 8            | -2           | 16           | 6            | 24           | 14           | 32           | 24           | 40           | 40           |
|  | 0.7 | 0  | -16          | 0            | -16          | 0            | -16          | 8            | -8           | 16           | 0            | 24           | 8            | 32           | 18           | 40           | 34           |
|  | 0.6 | -1   | -26          | -1           | -26          | -1           | -26          | 7            | -18          | 15           | -10          | 23           | -2           | 31           | 8            | 39           | 24           |
|  | 0.5 | -10  | -40          | -10          | -40          | -10          | -40          | -2           | -32          | 6            | -24          | 14           | -16          | 22           | -6           | 30           | 10           |
|  | 0.4 | -25  | -60          | -25          | -60          | -25          | -60          | -17          | -52          | -9           | -44          | -1           | -36          | 7            | -26          | 15           | -10          |

[ Table 56 ] Required time  $t_{VAC}$  above  $V_{IH}(ac)$  {blow  $V_{IL}(ac)$ } for valid transition

| Slew Rate[V/ns] | $t_{VAC} @175mV$ [ps] |     | $t_{VAC} @50mV$ [ps] |     |
|-----------------|-----------------------|-----|----------------------|-----|
|                 | min                   | max | min                  | max |
| >2.0            | 75                    | -   | 175                  | -   |
| 2.0             | 57                    | -   | 170                  | -   |
| 1.5             | 50                    | -   | 167                  | -   |
| 1.0             | 38                    | -   | 163                  | -   |
| 0.9             | 34                    | -   | 162                  | -   |
| 0.8             | 29                    | -   | 161                  | -   |
| 0.7             | 22                    | -   | 159                  | -   |
| 0.6             | 13                    | -   | 155                  | -   |
| 0.5             | 0                     | -   | 150                  | -   |
| < 0.5           | 0                     | -   | 150                  | -   |

Note :Clock and Strobe are drawn on a different time scale.

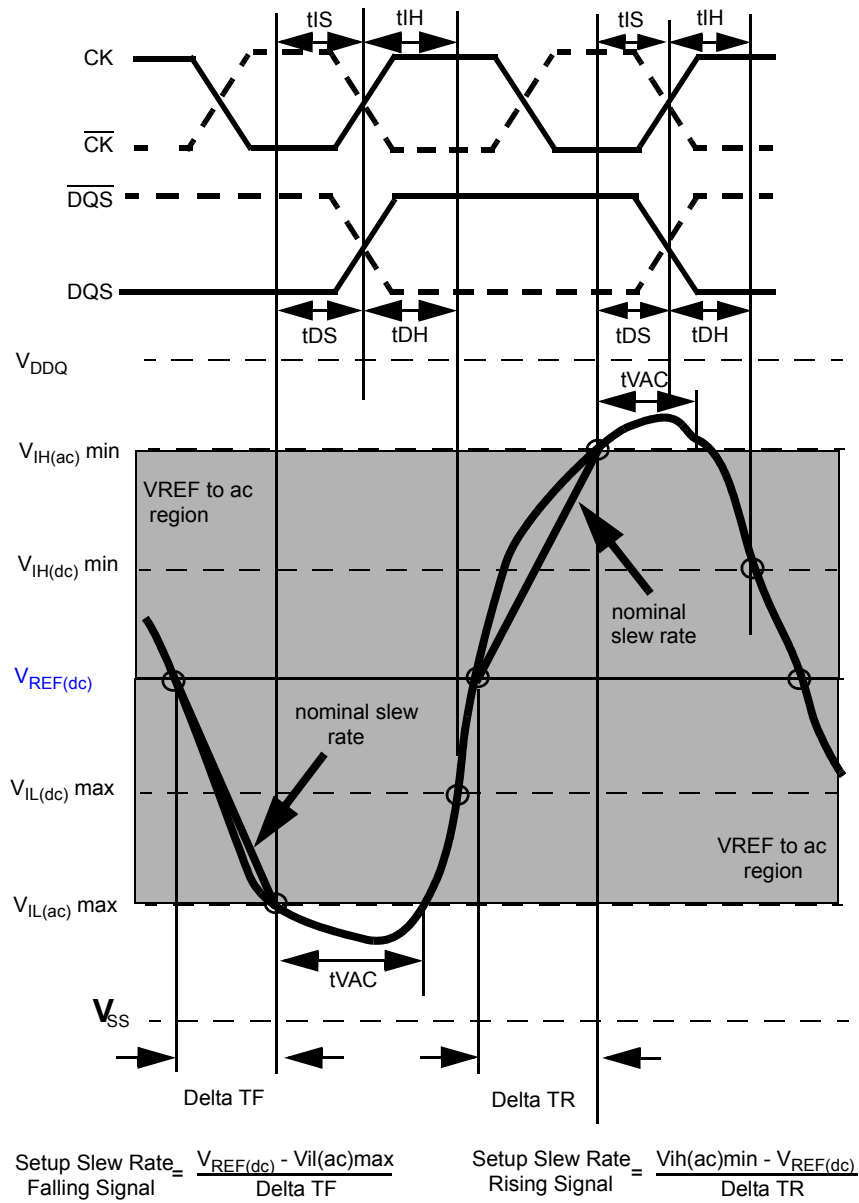


Figure 21 - Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

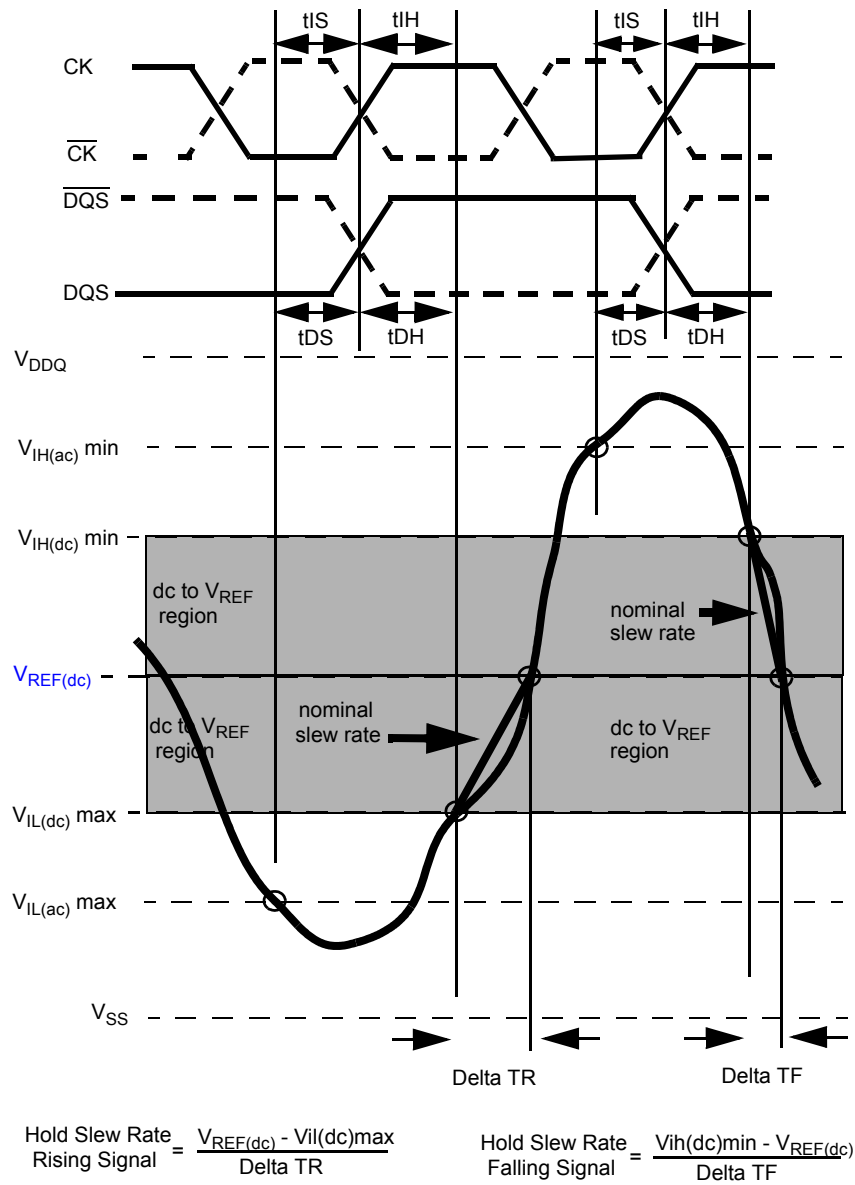


Figure 22 - Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

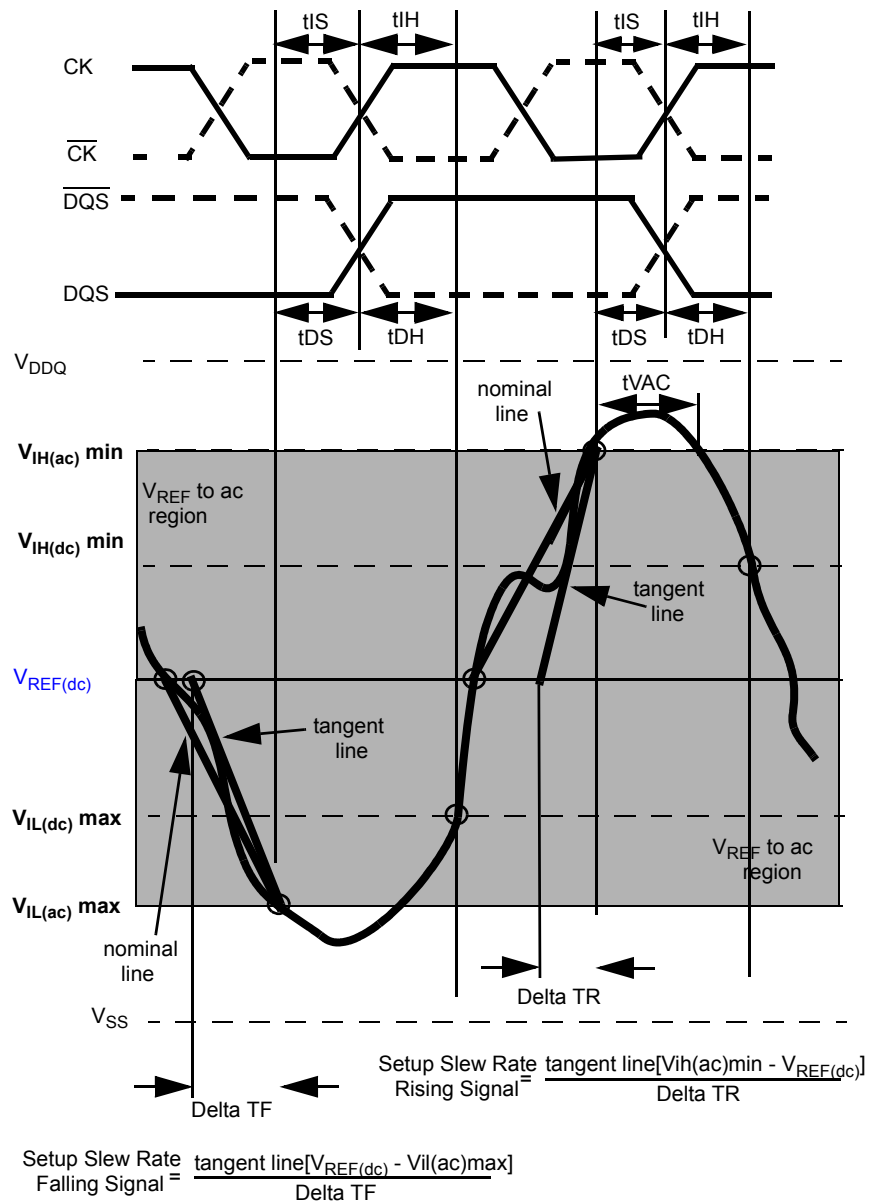


Figure 23. Illustration of tangent line for setup time  $t_{DS}$  (for DQ with respect to strobe) and  $t_{IS}$  (for ADD/CMD with respect to clock)

Note :Clock and Strobe are drawn on a different time scale.

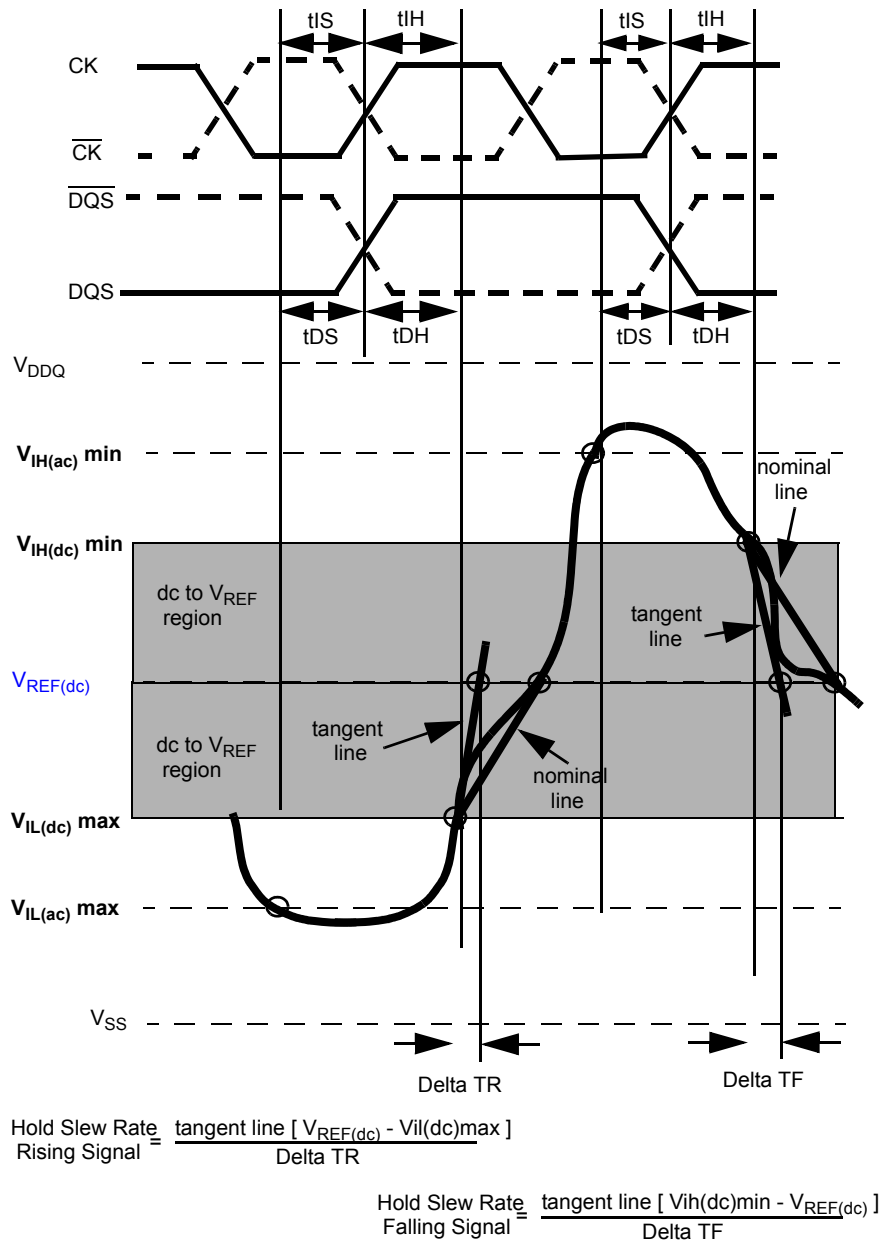


Figure 24 - Illustration of tangent line for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock)

**Data Setup, Hold and Slew Rate Derating:**

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 57) to the  $\Delta tDS$  and  $\Delta tDH$  (see Table 58) derating value respectively. Example: tDS (total setup time) = tDS(base) +  $\Delta tDS$ .

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max (see Figure 27). If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 29).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc) (see Figure 28). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see Figure 30).

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see Table 59).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the tables the derating values may be obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization

**[ Table 57 ] Data Setup and Hold Base-Value**

| [ps]      | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | reference |
|-----------|----------|-----------|-----------|-----------|-----------|
| tDS(base) | 75       | 25        | -10       | TBD       | VIH/L(ac) |
| tDH(base) | 150      | 100       | 65        | TBD       | VIH/L(dc) |

Note : AC/DC referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

**[ Table 58 ] Derating values DDR3-800/1066 tIS/tIH-ac/dc based**

| $\Delta tDS, \Delta tDH$ Derating [ps] AC/DC based <sup>a</sup> |     |                                |              |              |              |              |              |              |              |              |              |              |              |              |              |              |              |
|---|-----|--------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
|   |     | DQS,DQS Differential Slew Rate |              |              |              |              |              |              |              |              |              |              |              |              |              |              |              |
|   |     | 4.0 V/ns                       |              | 3.0 V/ns     |              | 2.0 V/ns     |              | 1.8 V/ns     |              | 1.6 V/ns     |              | 1.4V/ns      |              | 1.2V/ns      |              | 1.0V/ns      |              |
|   |     | $\Delta tDS$                   | $\Delta tDH$ | $\Delta tDS$ | $\Delta tDH$ | $\Delta tDS$ | $\Delta tDH$ | $\Delta tDS$ | $\Delta tDH$ | $\Delta tDS$ | $\Delta tDH$ | $\Delta tDS$ | $\Delta tDH$ | $\Delta tDS$ | $\Delta tDH$ | $\Delta tDS$ | $\Delta tDH$ |
| DQ Slew rate V/ns   | 2.0 | 88                             | 50           | 88           | 50           | 88           | 50           | -            | -            | -            | -            | -            | -            | -            | -            | -            | -            |
|   | 1.5 | 59                             | 34           | 59           | 34           | 59           | 34           | 67           | 45           | -            | -            | -            | -            | -            | -            | -            | -            |
|   | 1.0 | 0                              | 0            | 0            | 0            | 0            | 0            | 8            | 8            | 16           | 16           | -            | -            | -            | -            | -            | -            |
|   | 0.9 | -                              | -            | -2           | -4           | -2           | -4           | 6            | 4            | 14           | 12           | 22           | 20           | -            | -            | -            | -            |
|   | 0.8 | -                              | -            | -            | -            | -6           | -10          | 2            | -2           | 10           | 6            | 18           | 14           | 26           | 24           | -            | -            |
|   | 0.7 | -                              | -            | -            | -            | -            | -            | -3           | -8           | 5            | 0            | 13           | 8            | 21           | 18           | 29           | 34           |
|   | 0.6 | -                              | -            | -            | -            | -            | -            | -            | -            | -1           | -10          | 7            | -2           | 15           | 8            | 23           | 24           |
|   | 0.5 | -                              | -            | -            | -            | -            | -            | -            | -            | -            | -            | -11          | -16          | -2           | -6           | 6            | 10           |
|   | 0.4 | -                              | -            | -            | -            | -            | -            | -            | -            | -            | -            | -            | -            | -30          | -26          | -22          | -10          |

Note : a. Cell contents shaded in red are defined as 'not supported'.

**[ Table 59 ] Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition**

| Slew Rate[V/ns] | tVAC[ps] |     |
|-----------------|----------|-----|
|                 | min      | max |
| >2.0            | 75       | -   |
| 2.0             | 57       | -   |
| 1.5             | 50       | -   |
| 1.0             | 38       | -   |
| 0.9             | 34       | -   |
| 0.8             | 29       | -   |
| 0.7             | 22       | -   |
| 0.6             | 13       | -   |
| 0.5             | 0        | -   |
| <0.5            | 0        | -   |

Note :Clock and Strobe are drawn on a different time scale.

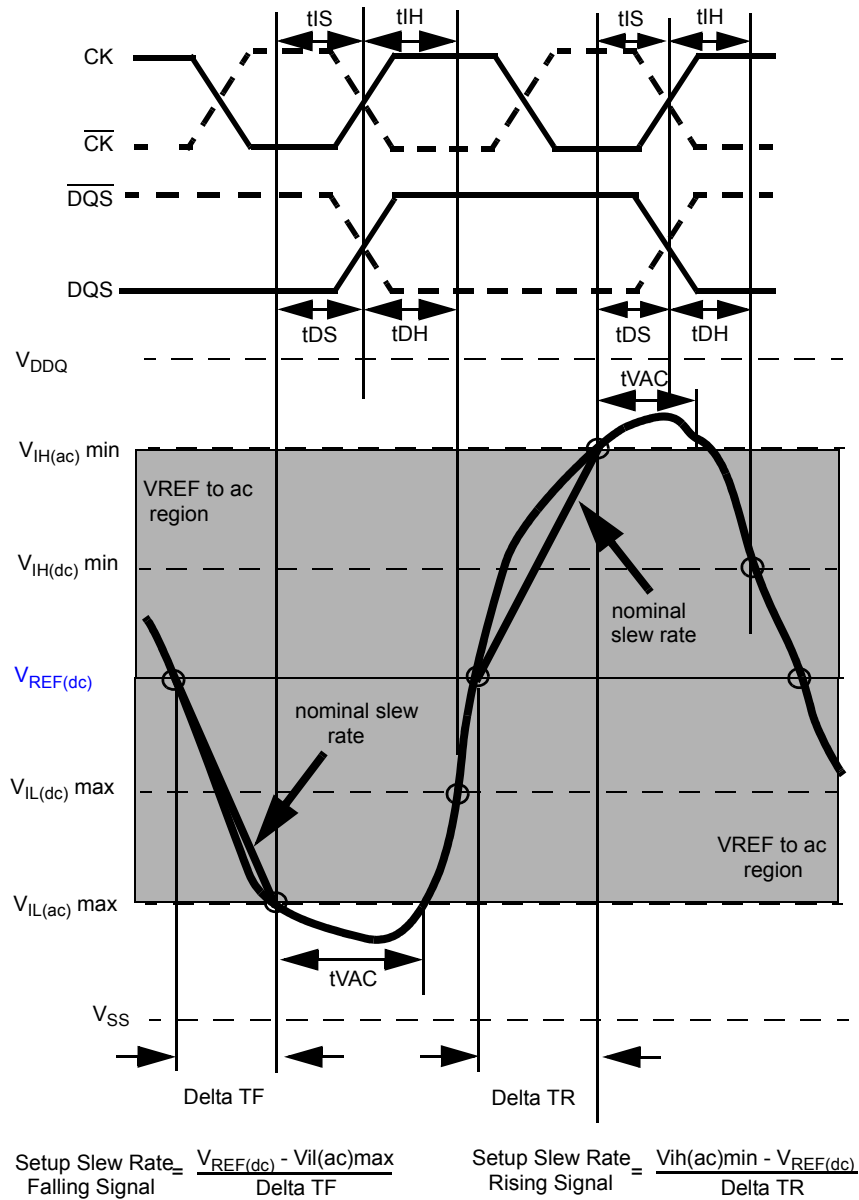


Figure 27 - Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

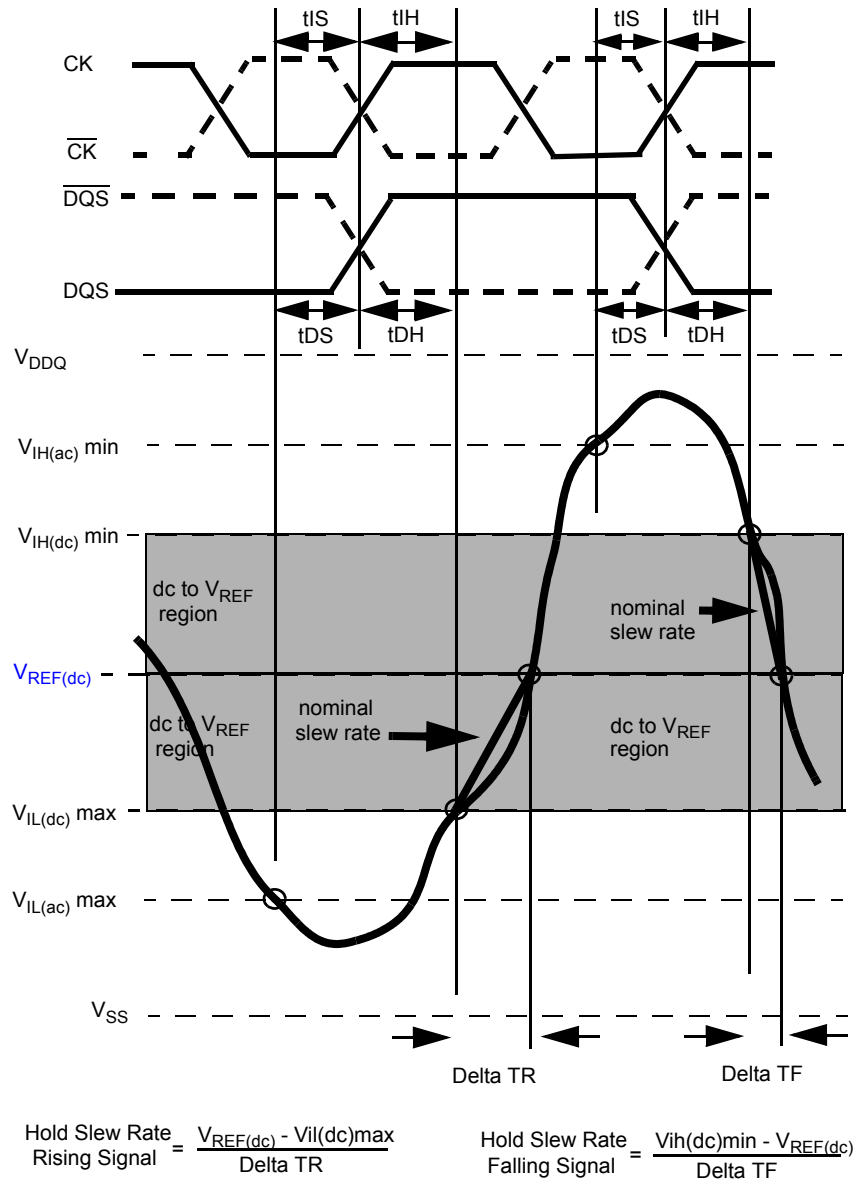


Figure 28 - Illustration of nominal slew rate for hold time  $t_{DH}$  (for DQ with respect to strobe) and  $t_{IH}$  (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

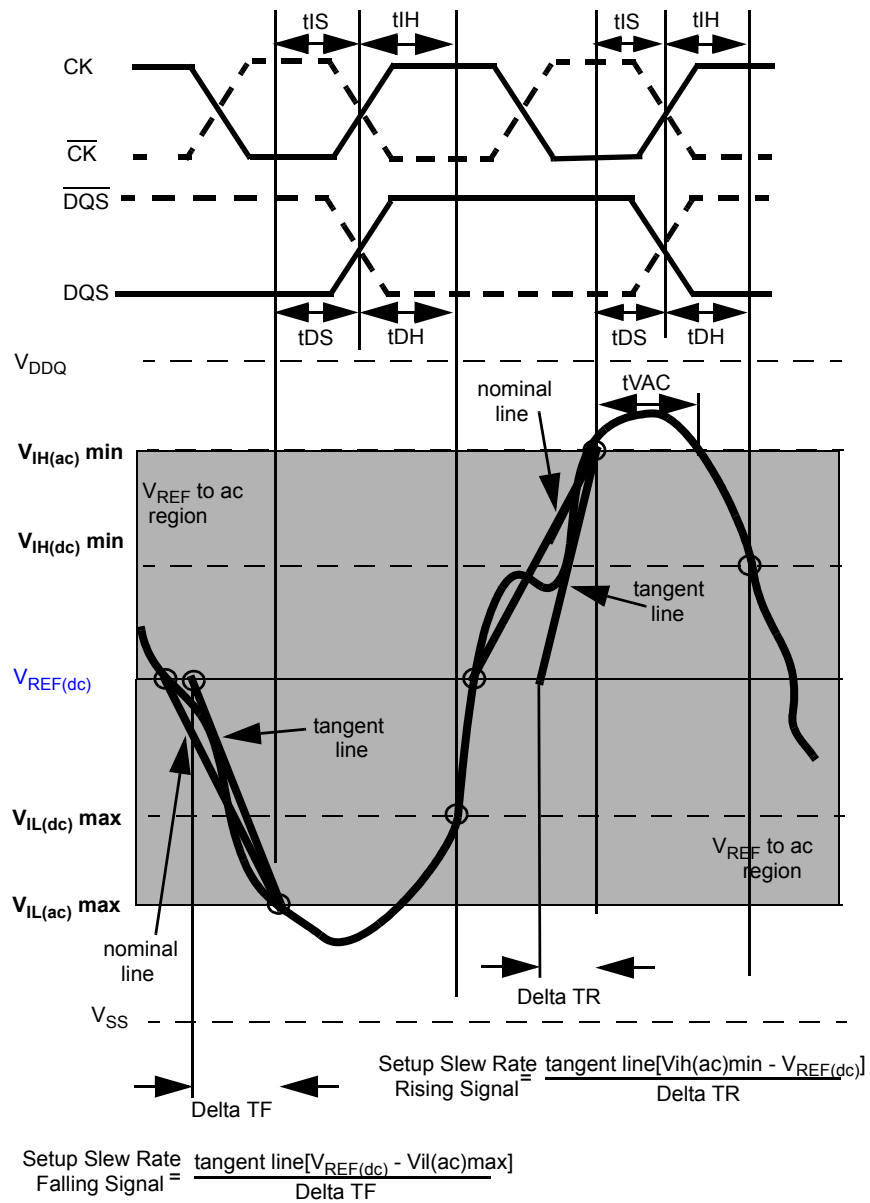


Figure 29 - Illustration of tangent line for setup time  $t_{DS}$  (for DQ with respect to strobe) and  $t_{IS}$  (for ADD/CMD with respect to clock)

Note :Clock and Strobe are drawn on a different time scale.

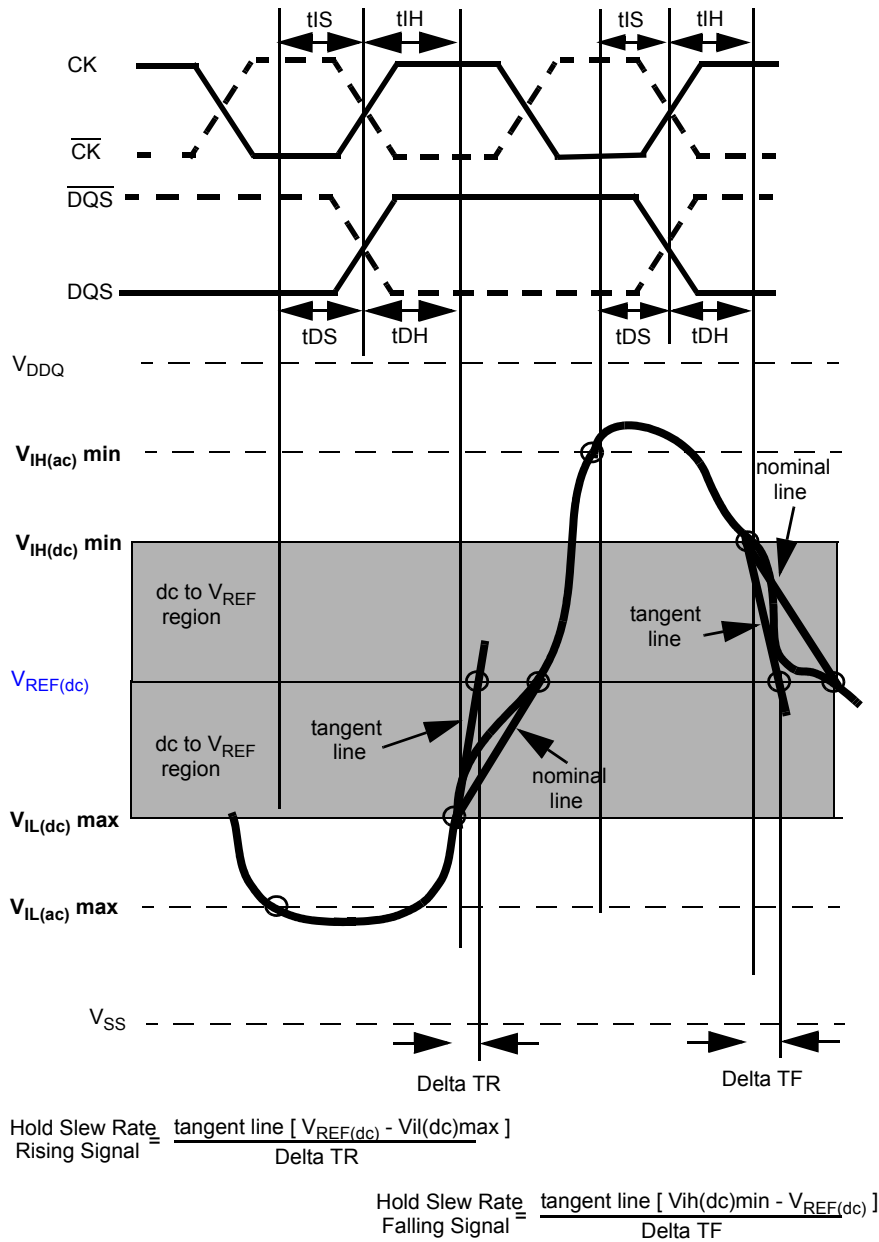


Figure 30 - Illustration of tangent line for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock)