DISCONTINUED

SED1635

LCD COMMON DRIVER

■ DESCRIPTION

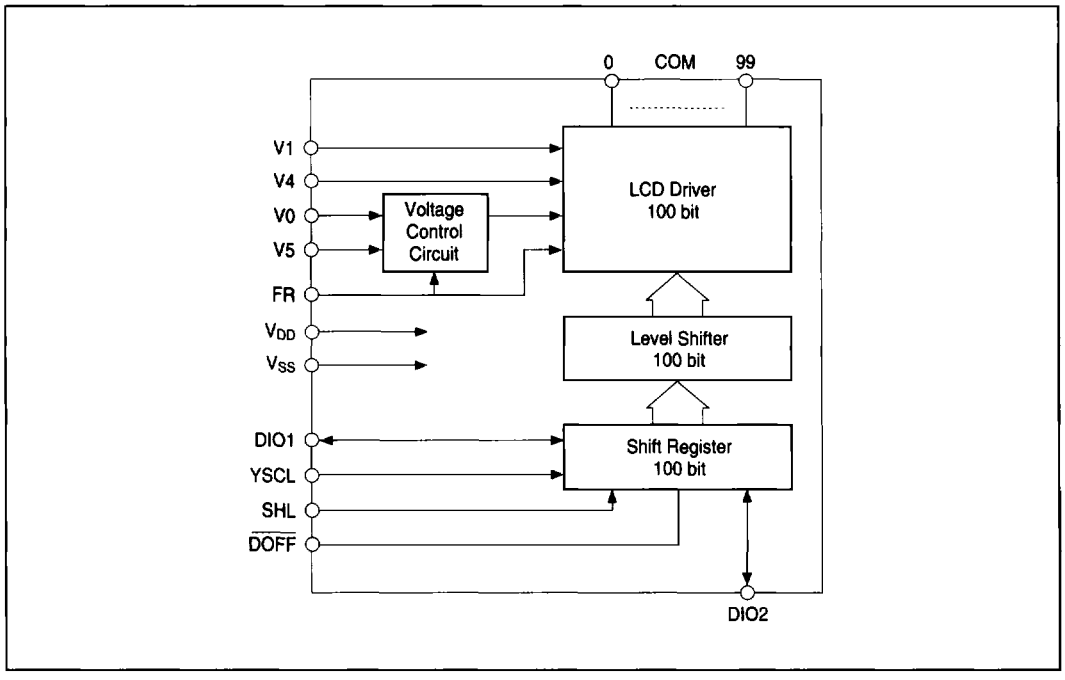
The SED1635 is a dot matrix LCD common (row) driver for use with high-capacity, high duty cycle LCD panels. The SED1635 has 100 common driver outputs and can operate at a duty cycle of up to 1/300. The driver is used with the SED1640D. The driver is designed to work over a wide range of LCD drive voltages and has its maximum drive voltage, V0, isolated from V_{DD} for flexibility of bias voltage generation.

The driver's pad layout is designed for easy mounting on boards and the bi-direction of driver output order can be selected. The driver has 100 LCD outputs with high resistance voltage and low output impedance. As a result, the driver achieves the maximum driver usage for the 1/200 duty panel.

■ FEATURES

- 100 common drive outputs
- Output resistance:
  500Ω typical, at V1 and V4 levels
  700Ω typical, at V0 and V5 levels
- Duty ratio from 1/64 to 1/300
- Maximum configuration: 640 × 480 pixels when used with the SED1640D
- Selectable shift direction
- Adjustable offset bias of LCD power for V_{DD} level
- Wide range of LCD drive voltages: 12 ~ 28V (absolute maximum rated voltage is 30V)
- Logic power supply: −2.7V to −5.5V
- CMOS Si-Gate process
- Package chip
  SED1635D_{1A}: Al pad
  SED1635D_{1B}: Gold bump

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Shift Register

The shift register shifts common data bi-directionally through the driver.

● Level Shifter

This is the level interface circuit that converts a signal voltage level from the logic level to the LCD driver level.

● LCD Driver and Voltage Control Circuit

The LCD driver voltage is output.

The relationship among the blanking control signal ($\overline{DOFF}$), shift register contents, the LCD AC-drive waveform (FR) and the common output level are given in the table below.

$\overline{DOFF}$	Shift Register Data	FR	COM Output Level	
H	H	H	V5	(Selected level)
		L	V0	
	L	H	V1	(Not selected level)
		L	V4	
L	Fixed to L	—	V0	

■ PIN DESCRIPTION

Pin Name	I/O	Functions	No. of pins
COM0 to COM99	O	LCD drive common low. Changes with YSCL falling edge.	100
DIO1, DIO2	I/O	Serial data I/O of 100-bit bidirectional shift register. Serial data input/output pin. Configured by SHL. Output changes with YSCL falling edge.	2
YSCL	I	Serial data shift clock input. Data is shifted into the driver on the falling edge of this signal.	1
SHL	I	Shift direction and input/output selection input. SHL: L → COM data shift direction: 0 → 99, DIO1: Input, DIO2: Output SHL: H → COM data shift direction: 99 → 0, DIO1: Output, DIO2: Input	1
$\overline{DOFF}$	I	Active low blanking control input. The shift register contents are cleared by low-level input, and all common output instantly changes to the V0 level.	1
FR	I	LCD AC drive signal input.	1
V_{DD}, V_{SS}	Power supply	Logic power input. V_{DD}: 0V (GND) Vss: –5.0V	2
V0, V1, V4, V5	Power supply	LCD drive power input. V5: –12V ~ –28V $V_{DD} \geq V- \geq V1 \geq V4 \geq V5$	4

Total 112

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Supply voltage 1	V_{SS}	–7.0 to +0.3	V
Supply voltage 2	V5	–30.0 to +0.3	V
Supply voltage 3	V0, V1, V4	V5 – 3.0 to +0.3	V
Input voltage	V_I	Vss – 0.3 to +0.3	V
Output voltage	V_O	Vss – 0.3 to +0.3	V
Output current 1	V0	20	mA
Output current 2	I_{OCOM}	20	mA
Power dissipation	PD	300	mW
Operating temperature	T_{OPR}	–40 to +85	°C
Storage temperature	T_{STG}	–65 to +150	°C

1. All voltages are given relative to V_{DD} = 0V.
2. V0, V1, and V4 must satisfy the condition $V_{DD} \geq V0 \geq V1 \geq V4 \geq 5$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Function operation under these conditions is not implied.

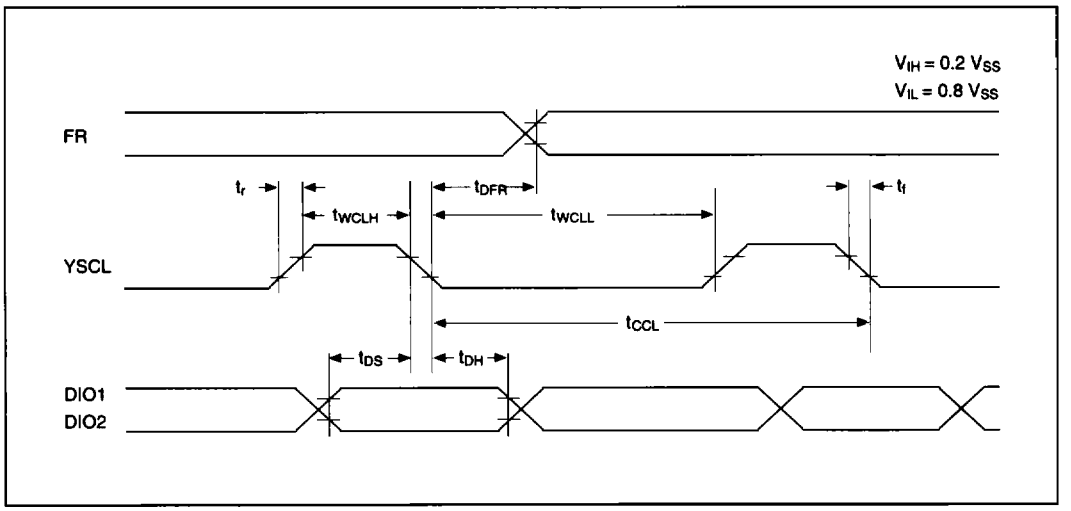
● DC Electrical Characteristics

Unless otherwise stated, V_{DD} = V0 = 0V, V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Pin	Min	Typ	Max	Unit
Supply voltage 1	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5	V_{SS} = –2.7 to –5.5V	V5	–28.0	—	–12.0	V
Minimum operating voltage	V5		V5	—	—	–8.0	V
Supply voltage 2	V0	Recommended value	V0	–2.5	—	0	V
Supply voltage 3	V1	Recommended value	V1	2/9 × V5	—	V_{DD}	V
Supply voltage 4	V4	Recommended value	V4	V5	—	7/9 × V5	V
High-level output voltage	V_{IH}	V_{SS} = –2.7 to –5.5V	DIO1, DIO2, YSCL, SHL, $\overline{DOFF}$, FR	0.2 × V_{SS}	—	—	V
Low-level output voltage	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.3 mA	DIO1, DIO2	–0.4	—	—	V
		I_{OH} = –0.2 mA (V_{SS} = –2.7 to –4.5V)					
Low-level output voltage	V_{OH}	I_{OL} = –0.3 mA		—	—	V_{SS} + 0.4	V
		I_{OL} = –0.2 mA (V_{SS} = –2.7 to –4.5V)					
Input, I/O leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	YSCL, SHL, $\overline{DOFF}$, FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	DIO1, DIO2	—	—	5.0	µA
Static current	I_{DDS}	V5 = –12.0 to –28.0, V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	#VON = 0.5V, V5 = –20.0V	V1, V4 Output Level, COM0 to COM99	—	0.40	0.80	KΩ
		#VON = 0.5V, V5 = –14.0V		—	0.50	1.00	
		#VON = 0.5V, (V5 = –8.0V)		—	(0.60)	(1.20)	
		#VON = 0.5V, V5 = –20.0V	V0, V5 Output Level, COM0 to COM99	—	0.60	1.20	
		#VON = 0.5V, V5 = –14.0V		—	0.70	1.40	
		#VON = 0.5V, (V5 = –8.0V)		—	(0.90)	(1.80)	
Current consumption (1)	I_{SS1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12 kHz, Frame frequency = 60 Hz, Input data: "H" every 1/200 no-load	V_{SS}	—	7	15	µA
		V_{SS} = –3.0V		—	5	10	
Current consumption (2)	I_{SS2}	V_{SS} = –5V, V1 = –2V, V4 = –18V, V5 = –20V, other conditions are same as I_{SS1}	V5	—	7	15	µA
Input capacitance	C_I	T_a = 25°C	YSCL, SHL, $\overline{DOFF}$, FR	—	—	8	pF
	$C_{I/O}$		DIO1, DIO2	—	—	15	pF

● AC Electrical Characteristics

○ Input Timing



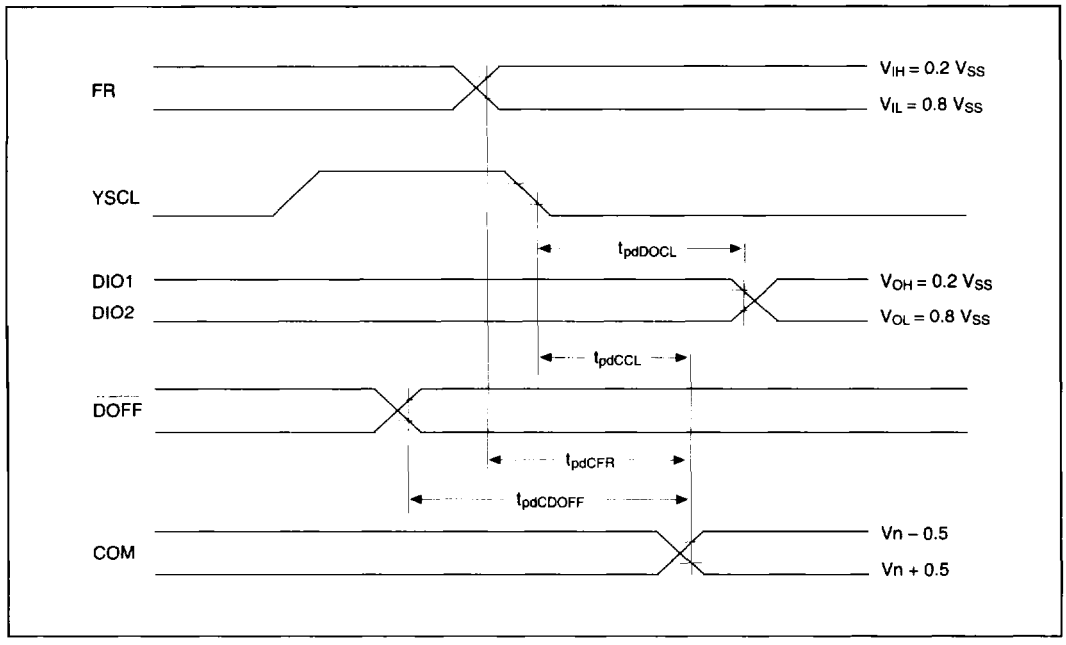
V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns
YSCL period	t_{CCL}		500	—	—	ns
YSCL "H" pulse width	t_{WCLH}		70	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns

V_{SS} = –2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns
YSCL period	t_{CCL}		1000	—	—	ns
YSCL "H" pulse width	t_{WCLH}		160	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		200	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns

○ **Output Timing**



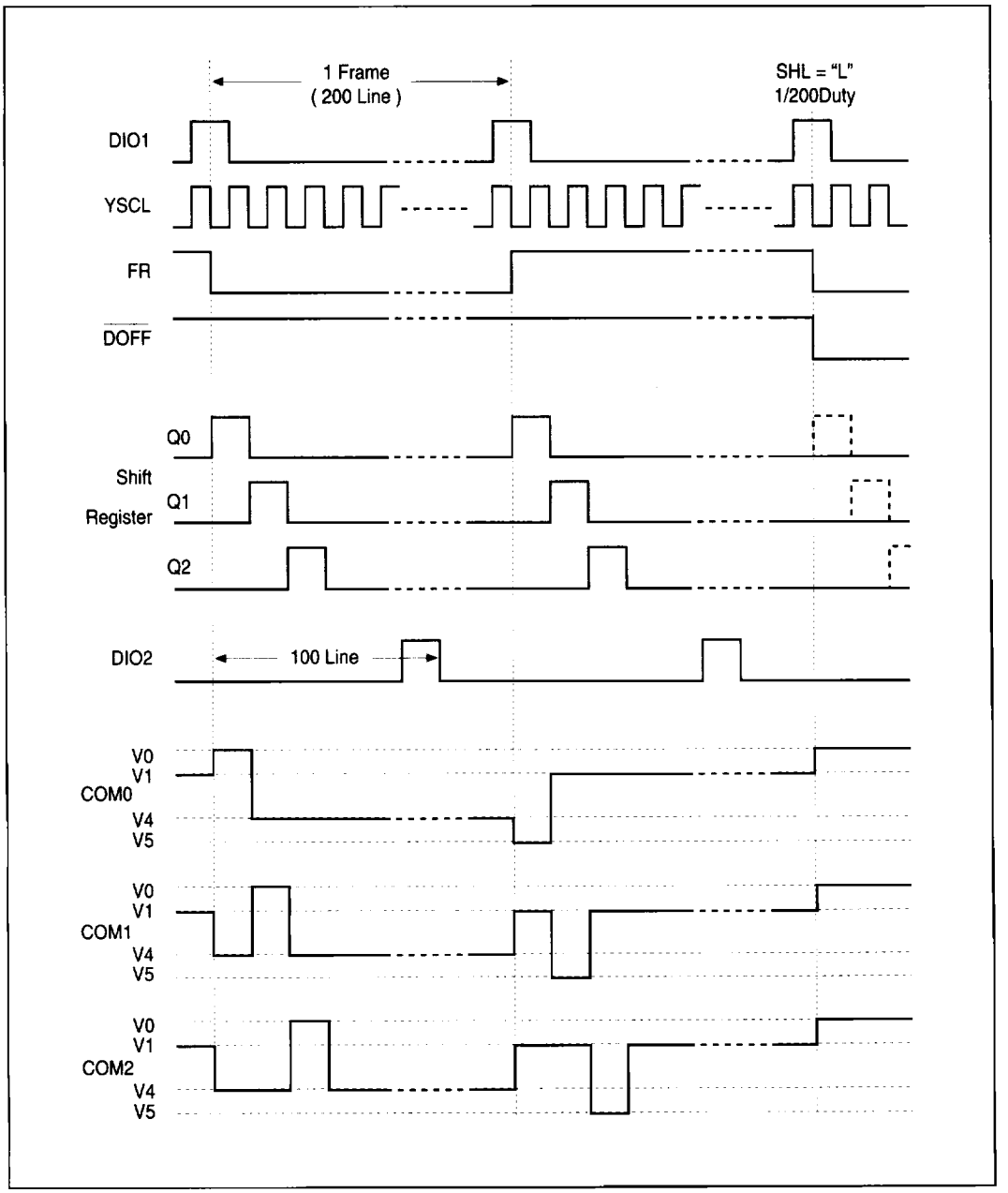
V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL fall edge to DIO delay	t_{pdDOCL}	CL = 15pF	30	—	300	ns
YSCL fall edge to COM delay	t_{pdCCL}	V5 = –12.0 to –28.0V CL = 100pF	—	—	3.0	µs
$\overline{DOFF}$ to COM delay	$t_{pdCDOFF}$					
FR to COM delay	t_{pdCFR}		—	—	3.0	µs

V_{SS} = –2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL fall edge to DIO delay	t_{pdDOCL}	CL = 15pF	60	—	400	ns
YSCL fall edge to COM delay	t_{pdCCL}	V5 = –12.0 to –28.0V CL = 100pF	—	—	3.0	µs
$\overline{DOFF}$ to COM delay	$t_{pdCDOFF}$					
FR to COM delay	t_{pdCFR}		—	—	3.0	µs

● **Timing Chart**



■ LCD DRIVER POWER SUPPLY

● Generating LCD Drive Voltages

The easiest way to generate LCD drive voltage is by the split resistors. To obtain a high quality display, it is mandatory that voltage levels be precise and stable. Set the split resistor values as low as the system's power capacity allows. In particular, when low power is required, set the split resistors high and, instead, drive each level with the voltage follower using the operation amplifier. To use an operation amplifier, V0 and V_{DD} are separated in this device. (V0 is the maximum potential level for the LCD driver.) However, if the V0 potential falls below the V_{DD} potential and, as a result, the potential difference is large, the LCD driver capability decreases. To avoid this, set the V_{DD} and V0 within 0V to 2.5V. If an operation amplifier is not used, connect the V0 and V_{DD}.

● System Power-Up

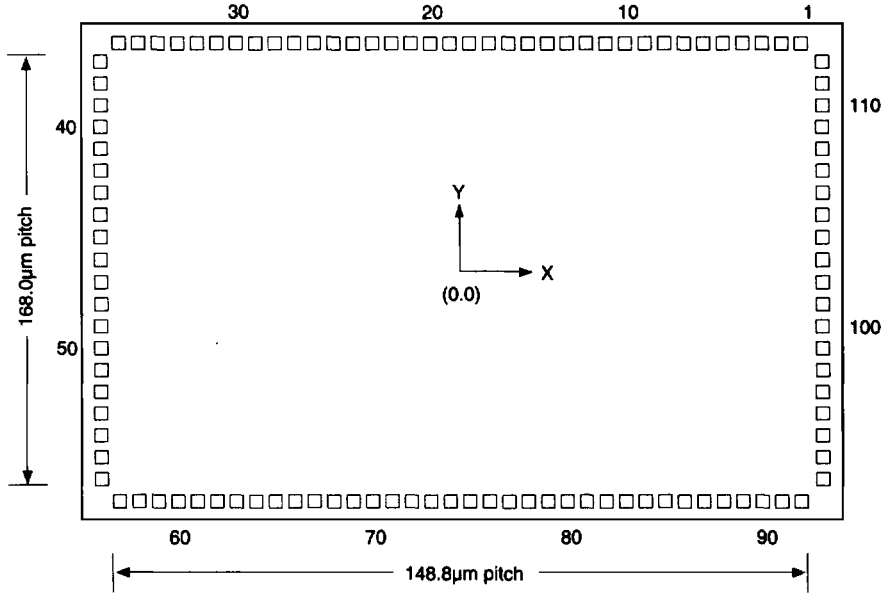
This LSI has high LCD drive voltage. As a result, if the logic power is being floated and high voltage is applied in the LCD driver, the LSI may be damaged because of the excess current.

Follow the sequence given below when turning power on or off.

To turn on the power – Turn on the logic power → Turn the LCD driver on
(or turn them on simultaneously)

To turn off the power – Turn off the LCD driver → Turn off the logic power
(or turn them off simultaneously)

■ PAD DIMENSIONS



(1) Aluminum pad chip specification

Chip size ..... 6.03 × 4.01 × 0.400 mm
Hole in pad ..... 108 × 110 µm

(2) Gold bumped chip specification (reference)

Chip size ..... 6.03 × 4.01 × 0.525 mm
Bumping size ..... 117 × 105 µm (±20 µm)
Bumping height ..... 20 +10µm
−5 µm

■ PAD COORDINATES

● SED1635D0A PAD COORDINATES

Unit: μm

Pad No.	Pin Name	X	Y
1	COM5	2604	1839
2	COM6	2455	1839
3	COM7	2306	1839
4	COM8	2158	1839
5	COM9	2009	1839
6	COM10	1860	1839
7	COM11	1711	1839
8	COM12	1562	1839
9	COM13	1414	1839
10	COM14	1265	1839
11	COM15	1116	1839
12	COM16	967	1839
13	COM17	818	1839
14	COM18	670	1839
15	COM19	521	1839
16	COM20	372	1839
17	COM21	223	1839
18	COM22	74	1839
19	COM23	−74	1839
20	COM24	−223	1839
21	COM25	−372	1839
22	COM26	−521	1839
23	COM27	−670	1839
24	COM28	−818	1839
25	COM29	−967	1839
26	COM30	−1116	1839
27	COM31	−1265	1839
28	COM32	−1414	1839
29	COM33	−1562	1839
30	COM34	−1711	1839
31	COM35	−1860	1839
32	COM36	−2009	1839
33	COM37	−2158	1839
34	COM38	−2306	1839
35	COM39	−2455	1839
36	COM40	−2604	1839
37	COM41	−2847	1596
38	COM42	−2847	1428
39	COM43	−2847	1260
40	COM44	−2847	1092
41	COM45	−2847	924
42	COM46	−2847	756
43	COM47	−2847	588
44	COM48	−2847	420
45	COM49	−2847	252
46	COM50	−2847	84
47	COM51	−2847	−84
48	COM52	−2847	−252
49	COM53	−2847	−420
50	COM54	−2847	−588
51	COM55	−2847	−756
52	COM56	−2847	−924
53	COM57	−2847	−1092
54	COM58	−2847	−1260
55	COM59	−2847	−1428
56	COM60	−2847	−1596
57	COM61	−2604	−1839
58	COM62	−2455	−1839
59	COM63	−2306	−1839
60	COM64	−2158	−1839
61	COM65	−2009	−1839
62	COM66	−1860	−1839
63	COM67	−1711	−1839
64	COM68	−1562	−1839
65	COM69	−1414	−1839
66	COM70	−1265	−1839
67	COM71	−1116	−1839
68	COM72	−967	−1839
69	COM73	−818	−1839
70	COM74	−670	−1839
71	COM75	−521	−1839
72	COM76	−372	−1839
73	COM77	−223	−1839
74	COM78	−74	−1839
75	COM79	74	−1839
76	COM80	223	−1839
77	COM81	372	−1839
78	COM82	521	−1839
79	COM83	670	−1839
80	COM84	818	−1839
81	COM85	967	−1839
82	COM86	1116	−1839
83	COM87	1265	−1839
84	COM88	1414	−1839
85	COM89	1562	−1839
86	COM90	1711	−1839
87	COM91	1860	−1839
88	COM92	2009	−1839
89	COM93	2158	−1839
90	COM94	2306	−1839
91	COM95	2455	−1839
92	COM96	2604	−1839
93	COM97	2847	−1596
94	COM98	2847	−1428
95	COM99	2847	−1260
96	DIO2	2847	−1092
97	DOFF	2847	−924
98	FR	2847	−756
99	YSCL	2847	−588
100	SHL	2847	−420
101	VDD	2847	−252
102	VSS	2847	−84
103	V0	2847	84
104	V1	2847	252
105	V4	2847	420
106	V5	2847	588
107	DIO1	2847	756
108	COM0	2847	924
109	COM1	2847	1092
110	COM2	2847	1260
111	COM3	2847	1428
112	COM4	2847	1596

● SED1635D0B PAD COORDINATES

Unit: μm

Pad No.	Pin Name	X	Y
1	COM5	2604	1834
2	COM6	2455	1834
3	COM7	2306	1834
4	COM8	2158	1834
5	COM9	2009	1834
6	COM10	1860	1834
7	COM11	1711	1834
8	COM12	1562	1834
9	COM13	1414	1834
10	COM14	1265	1834
11	COM15	1116	1834
12	COM16	967	1834
13	COM17	818	1834
14	COM18	670	1834
15	COM19	521	1834
16	COM20	372	1834
17	COM21	223	1834
18	COM22	74	1834
19	COM23	−74	1834
20	COM24	−223	1834
21	COM25	−372	1834
22	COM26	−521	1834
23	COM27	−670	1834
24	COM28	−818	1834
25	COM29	−967	1834
26	COM30	−1116	1834
27	COM31	−1265	1834
28	COM32	−1414	1834
29	COM33	−1562	1834
30	COM34	−1711	1834
31	COM35	−1860	1834
32	COM36	−2009	1834
33	COM37	−2158	1834
34	COM38	−2306	1834
35	COM39	−2455	1834
36	COM40	−2604	1834
37	COM41	−2847	1596
38	COM42	−2847	1428
39	COM43	−2847	1260
40	COM44	−2847	1092

Pad No.	Pin Name	X	Y
41	COM45	−2847	924
42	COM46	−2847	756
43	COM47	−2847	588
44	COM48	−2847	420
45	COM49	−2847	252
46	COM50	−2847	84
47	COM51	−2847	−84
48	COM52	−2847	−252
49	COM53	−2847	−420
50	COM54	−2847	−588
51	COM55	−2847	−756
52	COM56	−2847	−924
53	COM57	−2847	−1092
54	COM58	−2847	−1260
55	COM59	−2847	−1428
56	COM60	−2847	−1596
57	COM61	−2604	−1834
58	COM62	−2455	−1834
59	COM63	−2306	−1834
60	COM64	−2158	−1834
61	COM65	−2009	−1834
62	COM66	−1860	−1834
63	COM67	−1711	−1834
64	COM68	−1562	−1834
65	COM69	−1414	−1834
66	COM70	−1265	−1834
67	COM71	−1116	−1834
68	COM72	−967	−1834
69	COM73	−818	−1834
70	COM74	−670	−1834
71	COM75	−521	−1834
72	COM76	−372	−1834
73	COM77	−223	−1834
74	COM78	−74	−1834
75	COM79	74	−1834
76	COM80	223	−1834
77	COM81	372	−1834
78	COM82	521	−1834
79	COM83	670	−1834
80	COM84	818	−1834

Pad No.	Pin Name	X	Y
81	COM85	967	−1834
82	COM86	1116	−1834
83	COM87	1265	−1834
84	COM88	1414	−1834
85	COM89	1562	−1834
86	COM90	1711	−1834
87	COM91	1860	−1834
88	COM92	2009	−1834
89	COM93	2158	−1834
90	COM94	2306	−1834
91	COM95	2455	−1834
92	COM96	2604	−1834
93	COM97	2842	−1596
94	COM98	2842	−1428
95	COM99	2842	−1260
96	DIO2	2842	−1092
97	$\overline{\text{DOFF}}$	2842	−924
98	FR	2842	−756
99	YSCL	2842	−588
100	SHL	2842	−420
101	V_{DD}	2842	−252
102	V_{SS}	2842	−84
103	V0	2842	84
104	V1	2842	252
105	V4	2842	420
106	V5	2842	588
107	DIO1	2842	756
108	COM0	2842	924
109	COM1	2842	1092
110	COM2	2842	1260
111	COM3	2842	1428
112	COM4	2842	1596