HM62Y8201H Series

16M High Speed SRAM (2-Mword × 8-bit)

HITACHI

ADE-203-956 (Z)
Preliminary, Rev. 0.0
Sept. 15, 1998

Description

The HM62Y8201H Series is an asynchronous high speed static RAM organized as 2-Mword × 8-bit. It has realized high speed access time by employing the most advanced CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 44-pin plastic TSOPII.

Features

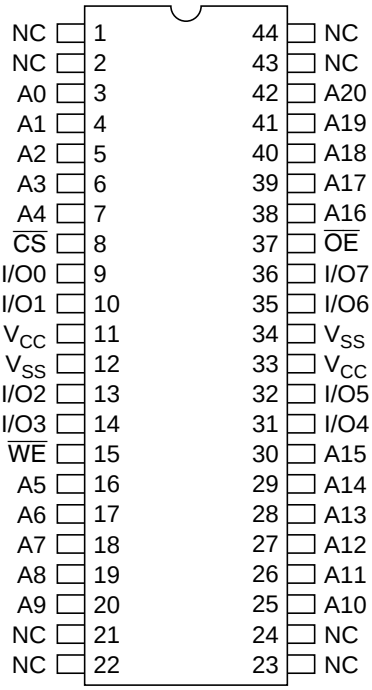
- Single 2.5 V supply: 2.5 V ± 0.2 V
- Access time 12 ns/15 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Operating current: 150 mA/130 mA (max)
- TTL standby current: 60 mA/50 mA (max)
- CMOS standby current: 30 mA/10 mA (max)
  : 3.0 mA /1.5 mA (max) (L-Version)
- Data retention current: 3.0 mA /1.5 mA (max) (L-Version)
- Data retention voltage: 2.0 V (min) (L-Version)
- Center V_{CC} and V_{SS} type pinout

Ordering Information

Type No.	Access time	Package
HM62Y8201HTT-12	12 ns	400-mil 44-pin plastic TSOPII (TTP-44DE)
HM62Y8201HTT-15	15 ns	
HM62Y8201HLTT-12	12 ns	
HM62Y8201HLTT-15	15 ns	

Pin Arrangement

44-pin TSOP

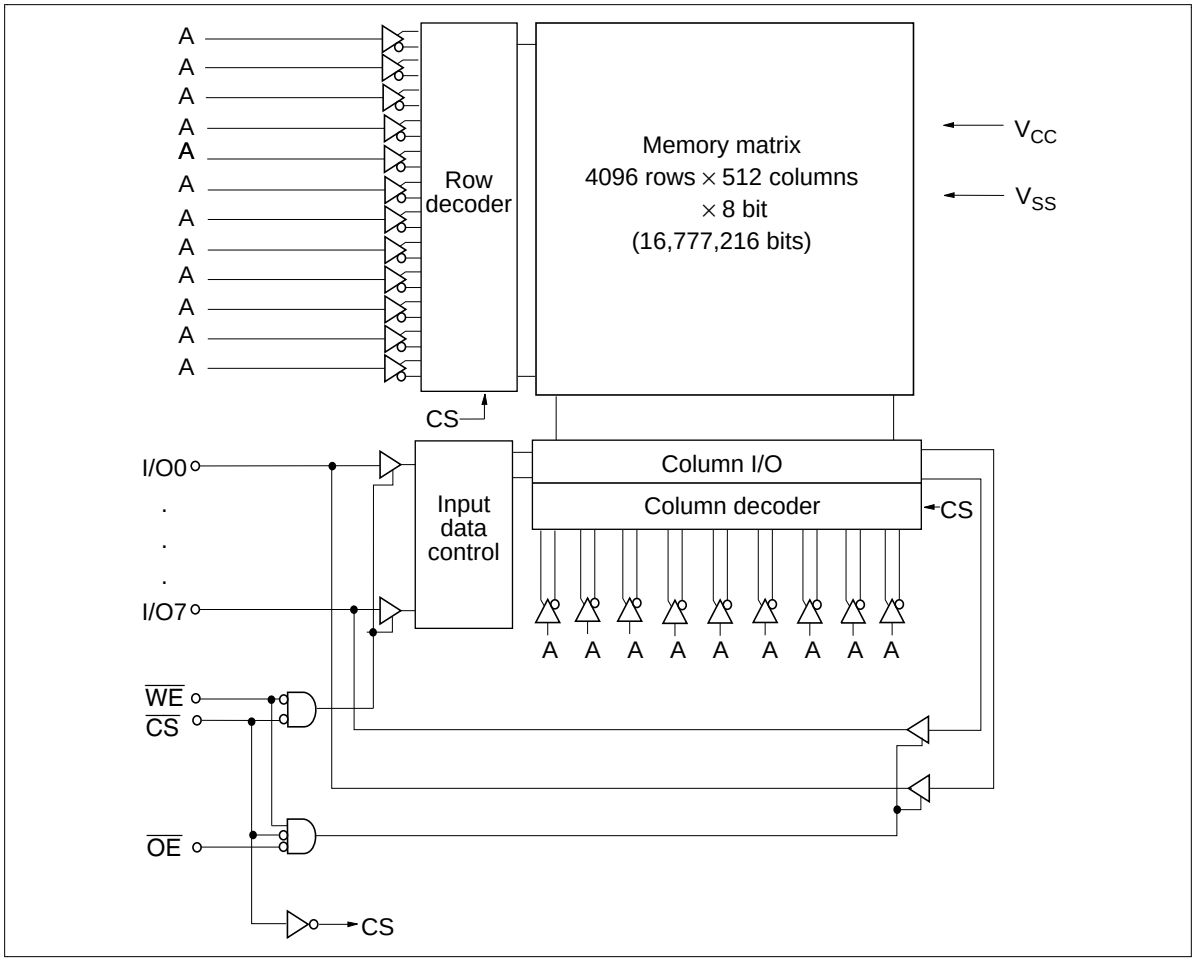


(Top view)

Pin Description

Pin name	Function
A0 to A20	Address input
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Operating Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Operation
H	×	×	High-Z	Standby
L	H	L	Dout	Read
L	L	H	Din	Write
L	L	L	Din	Write
L	H	H	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +3.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC}+0.5*[2](≤ 3.6 V (max))	V
Power dissipation	P_T	1.0	W
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. V_T (min) = –1.5 V for pulse width (under shoot) ≤ 5 ns
2. V_T (max) = V_{CC} +1.5 V for pulse with (over shoot) ≤ 5 ns

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	2.3	2.5	2.7	V	3
	V_{SS}	0	0	0	V	4
Input high voltage	V_{IH}	1.7	—	V_{CC} + 0.3*[2]	V	
Input low voltage	V_{IL}	–0.3*[1]	—	0.7	V	
Ambient temperature	Ta	0	—	70	°C	

Notes: 1. V_{IL} (min) = –1.5 V for pulse width (under shoot) ≤ 5 ns
2. V_{IH} (max) = V_{CC} + 1.5 V for pulse width (over shoot) ≤ 5 ns
3. The supply voltage with all V_{CC} pins must be on the same level.
4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

Parameter		Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Operating current	12 ns cycle	I_{CC}	—	—	150	mA	Min cycle $\overline{CS}$ = V_{IL}, lout = 0 mA Other inputs = V_{IH}/V_{IL}
	15 ns cycle	I_{CC}	—	—	130		
Standby current	12 ns cycle	I_{SB}	—	—	60	mA	Min cycle $\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}
	15 ns cycle	I_{SB}	—	—	50		
	12 ns cycle	I_{SB1}	—	—	30	mA	f = 0 MHz $V_{CC} \geq \overline{CS} \geq V_{CC}$ - 0.2 V, (1) 0 V ≤ Vin ≤ 0.2 V or (2) $V_{CC} \geq$ Vin ≥ V_{CC} - 0.2 V
		I_{SB1}*[2]	—	—	3.0		
	15 ns cycle	I_{SB1}	—	—	10		
		I_{SB1}*[2]	—	—	1.5		
Output high voltage		V_{OH}	1.7	—	—	V	I_{OH} = –2 mA
Output low voltage		V_{OL}	—	—	0.7	V	I_{OL} = 2 mA

Notes: 1. Typical values are at V_{CC} = 2.5 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = +25°C, f = 1.0 MHz)

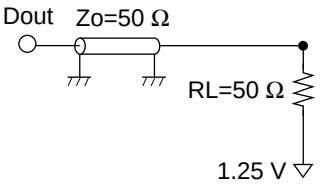
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	6	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.5 V ± 0.2 V)

Test Conditions

- Input pulse levels: V_{IL} = 0 V, V_{IH} = 2.5 V
- Input rise and fall time: 2.5 ns
- Input and output timing reference levels: 1.25 V
- Output load: See figures (Including scope and jig)



Output load (A)

TBD

Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW})

Read Cycle

		HM62Y8201H					
		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	12	—	15	—	ns	
Address access time	t_{AA}	—	12	—	15	ns	
Chip select access time	t_{ACS}	—	12	—	15	ns	
Output enable to output valid	t_{OE}	—	6	—	7	ns	
Output hold from address change	t_{OH}	3	—	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	6	—	7	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	—	7	ns	1

Write Cycle

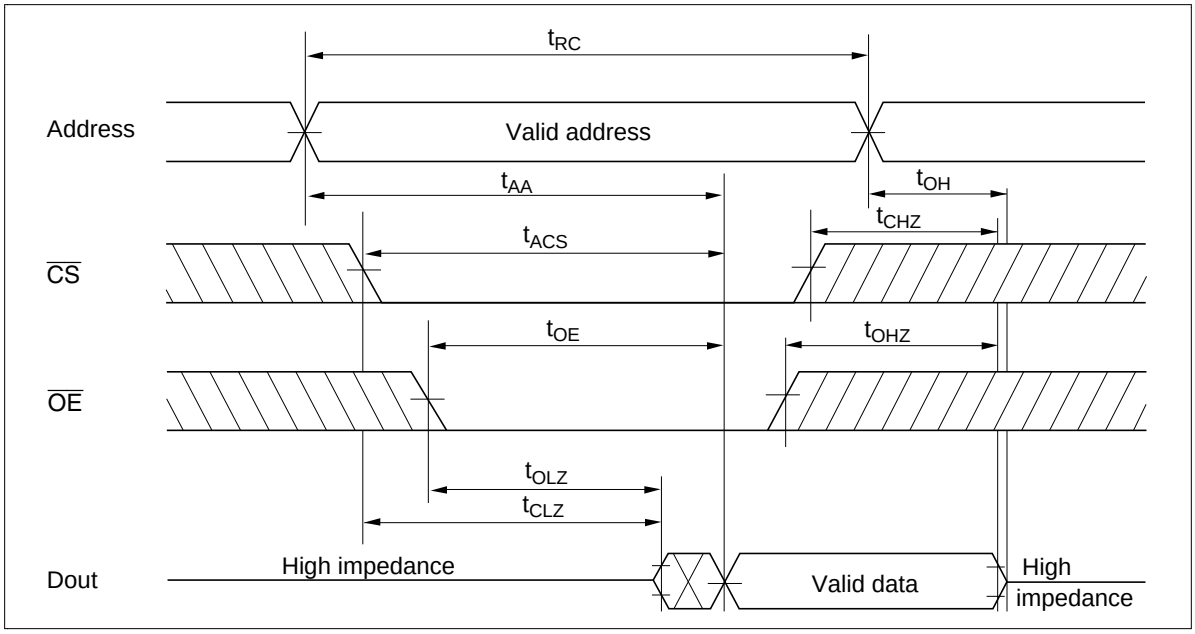
		HM62Y8201H					
		-12		-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	12	—	15	—	ns	
Address valid to end of write	t_{AW}	8	—	10	—	ns	
Chip select to end of write	t_{CW}	8	—	10	—	ns	9
Write pulse width	t_{WP}	8	—	10	—	ns	8
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	6	—	7	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	—	7	ns	1
Write enable to output in high-Z	t_{WHZ}	—	6	—	7	ns	1

Notes: 1. Transition is measured ±200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.

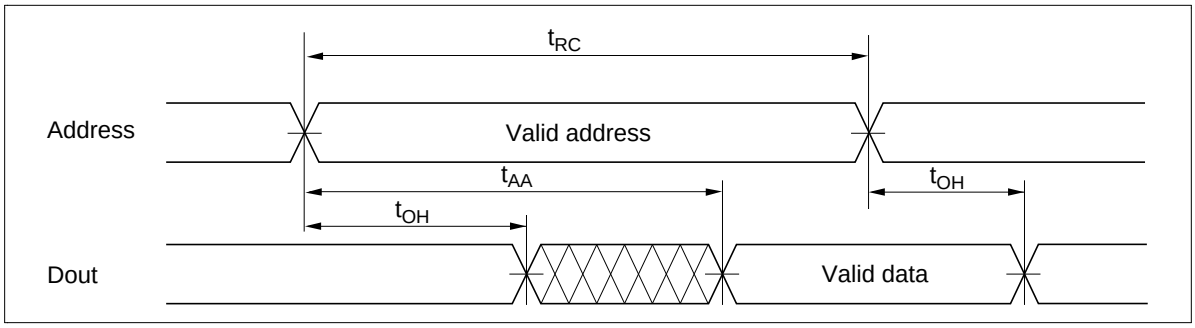
2. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.
4. if $\overline{CS}$ and $\overline{OE}$ are Low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
6. t_{AS} is measured from the latest address transition to the later of $\overline{CS}$ or $\overline{WE}$ going low.
7. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the first address transition.
8. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
9. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.

Timing Waveforms

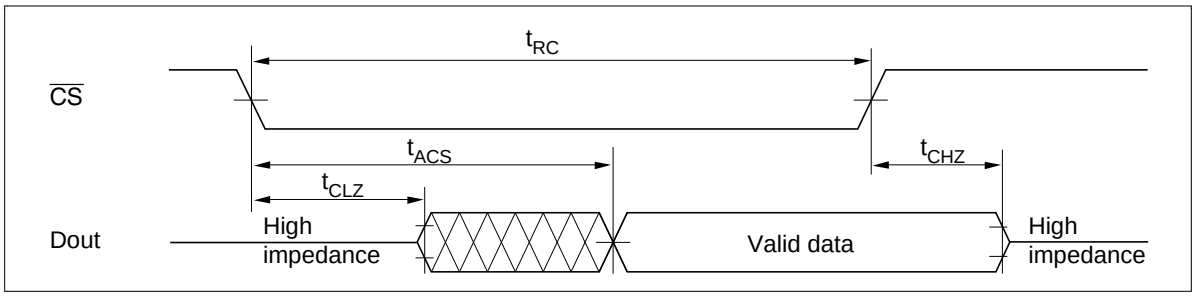
Read Timing Waveform (1) ($\overline{WE}$ = V_{IH})



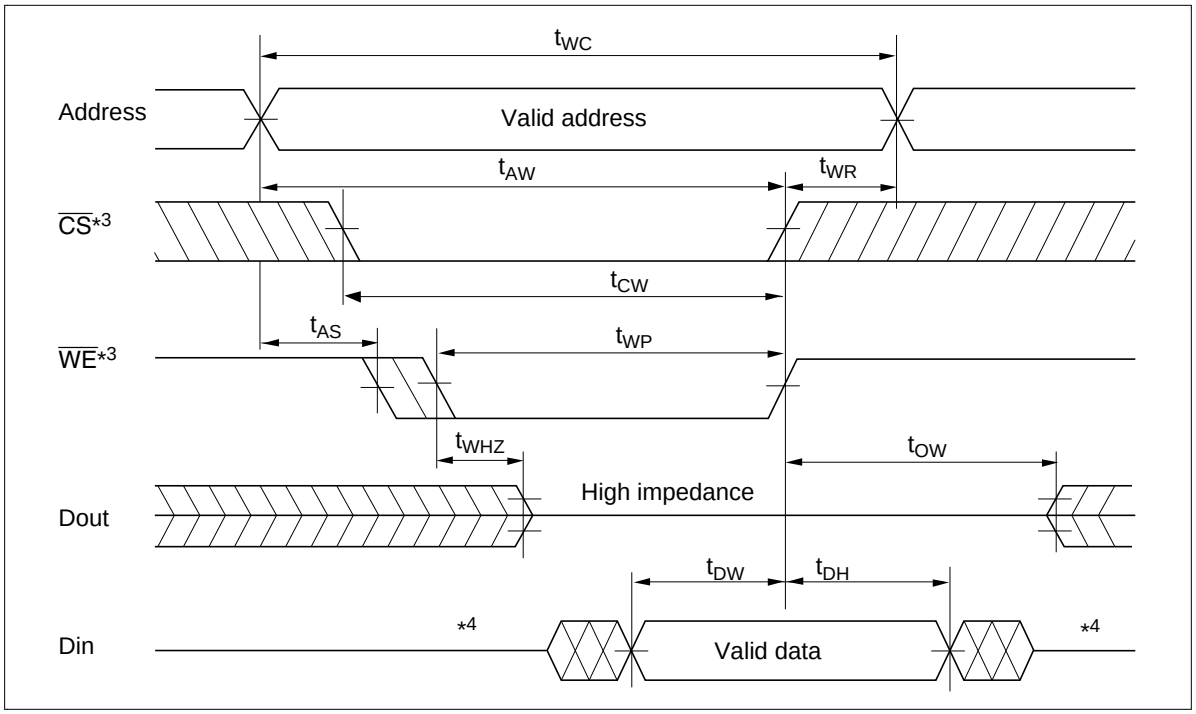
Read Timing Waveform (2) ($\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IL})



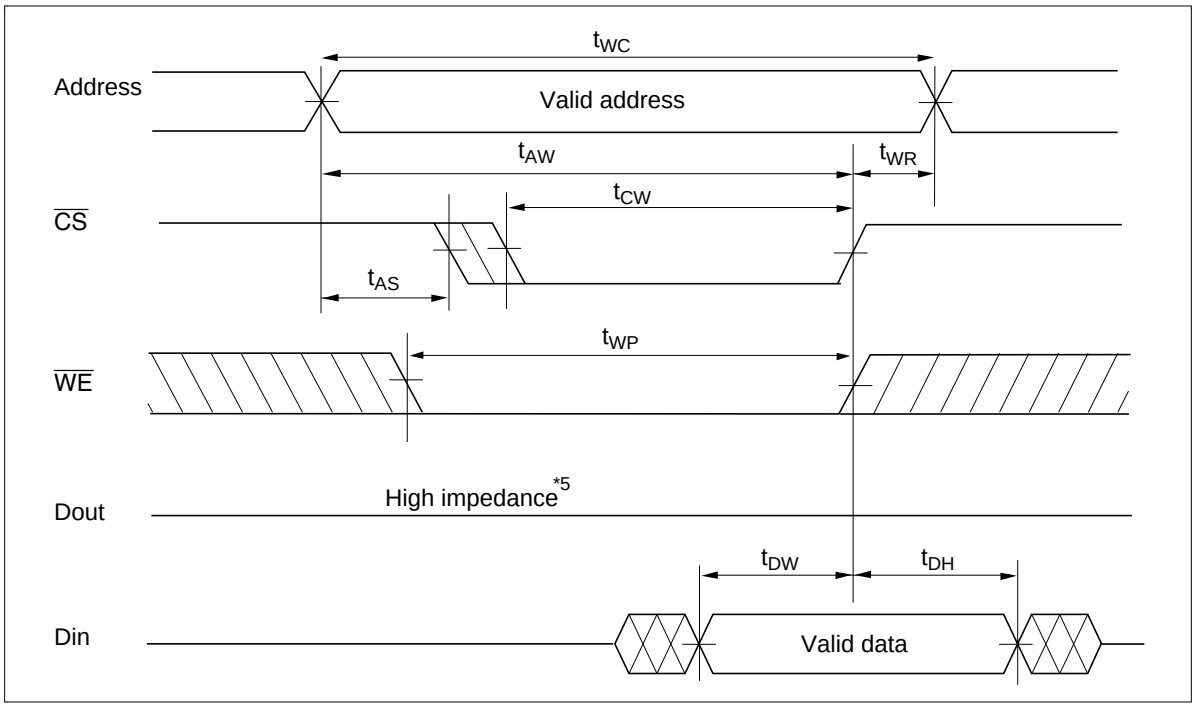
Read Timing Waveform (3) ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})*2



Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



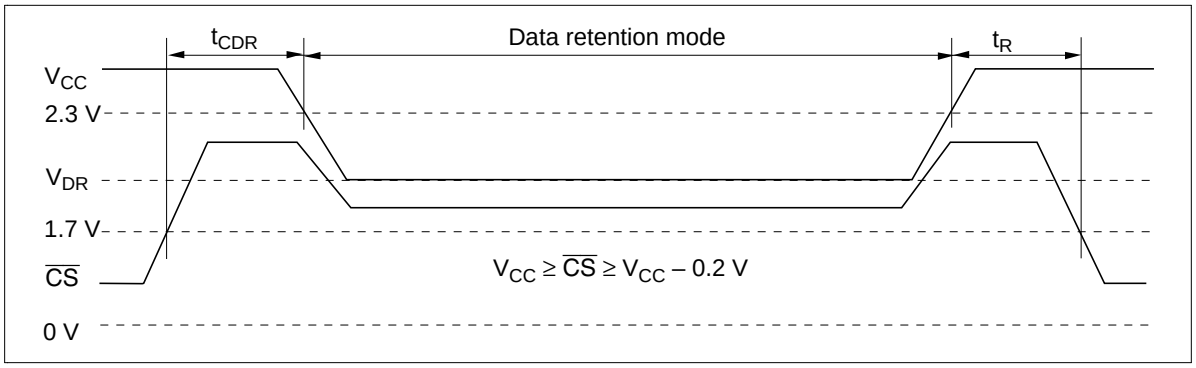
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter		Symbol	Min	Typ*[1]	Max	Unit	Test conditions
V_{CC} for data retention		V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V ≤ Vin ≤ 0.2 V or (2) $V_{CC} \geq$ Vin $\geq V_{CC} - 0.2$ V
Data retention current	12 ns cycle	I_{CCDR}	—	—	3.0	mA	V_{CC} = 2.5 V, $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V ≤ Vin ≤ 0.2 V or (2) $V_{CC} \geq$ Vin $\geq V_{CC} - 0.2$ V
	15 ns cycle	I_{CCDR}	—	—	1.5	mA	
Chip deselect to data retention time		t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time		t_R	5	—	—	ms	

Note: 1. Typical values are at V_{CC} = 2.5 V, Ta = +25°C, and not guaranteed.

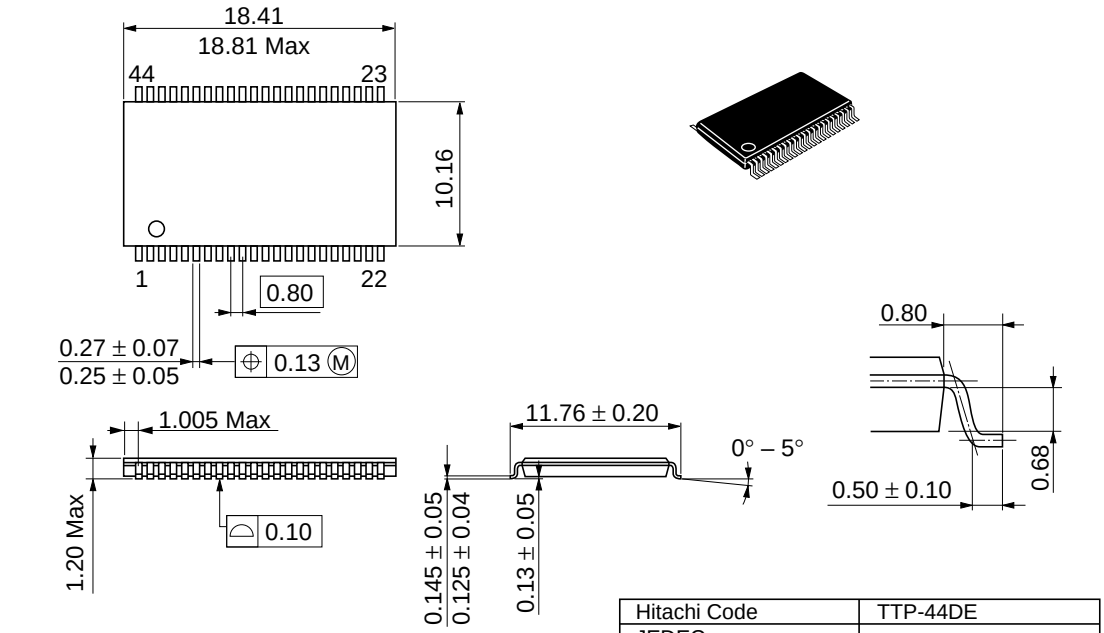
Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM62Y8201HTT/HLTT Series (TTP-44DE)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
EIAJ	—
Weight (reference value)	0.43 g

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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA 94005-1897
Tel: <1> (800) 285-1601
Fax: <1> (303) 297-0447

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Revision Record

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0.0	Sep. 15, 1998	Initial issue		