CD22354, CD22357

Advance Information/ Preliminary Data

CMOS Single-Chip, Full-Feature PCM CODEC

Features:

- *Low power dissipation:*
  80 mW - typical operating
  5 mW - typical standby
- *Meets or exceeds all AT&T D3/D4 specifications and CCITT recommendations*
- *Complete CODEC and filtering systems:*
  No external components for sample-and-hold and auto-zero functions
  Transmit input section includes anti-aliasing prefilter
  Receive output filter with SIN X/X correction
- *Variable data clocks - from 64 kHz to 4.1 MHz*
- *Programmable gain for transmit input*
- *CD22354 - 16-pin μ-law CODEC*
- *CD22357 - 16-pin A-law CODEC*
- *Synchronous and asynchronous operation*
- *TTL or CMOS-compatible logic*
- *±5-V operation*
- *Fast acquisition on power-up*
- *ESD protection on all inputs and outputs*
- *Automatic power-down by removal of both frame syncs*
- *Internal precision voltage reference*

The RCA-CD22354 and CD22357 are monolithic silicon-gate, double-poly CMOS integrated circuits containing the band-limiting filters and the companding A/D and D/A conversion circuits that conform to the AT&T D3/D4 specifications and CCITT recommendations. The CD22354 provides the AT&T μ-law and the CD22357 provides the CCITT A-law companding characteristic.

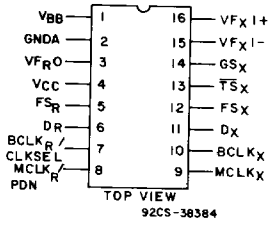
The primary applications for the CD22354 and CD22357 are in telephone systems. These circuits perform the analog and digital conversions between the subscriber loop and the PCM highway in a digital switching system. The functional block diagram is shown in Fig. 1.

With the flexible features, including synchronous and asynchronous operations and variable data rates, the CD22354 and CD22357 are ideally suited for PABX, central office switching system, digital telephones as well as other applications that require accurate A/D and D/A conversions and minimal conversion time.

The CD22354 and CD22357 are supplied in 16-lead dual-in-line plastic packages (E suffix).

Applications:

- *PABX*
- *Central office switching systems*
- *Accurate A/D and D/A conversions*
- *Digital telephones*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE V_{CC}	+6 V
DC SUPPLY-VOLTAGE V_{BB}	-6 V
OPERATING TEMPERATURE RANGE	-25 to +85°C
STORAGE TEMPERATURE RANGE	-65 to+150°C
POWER DISSIPATION AT 25°C	500 mW
DIGITAL INPUT	-0.5 to V_{CC} +0.5 V

File Number **1682**

Table I

Pin Symbol	Pin Names	Pin No.
V_{BB}	Negative power supply	1
GNDA	Ground analog	2
VF_RO	Analog output	3
V_{CC}	Positive power supply	4
FS_R	Frame sync. receive	5
D_R	Receive data input	6
$BCLK_R$/CLKSEL	Bit clock receive/Master clock select	7
$MCLK_R$/PDN	Master clock receive/Power down	8
$MCLK_X$	Master clock transmit	9
$BCLK_X$	Bit clock transmit	10
D_X	PCM data output	11
FS_X	Frame sync. transmit	12
$\overline{TS_X}$	Open drain output (Encoder Indicator)	13
GS_X	Transmit gain adjust	14
VF_XI^-	Inverting input of the input amplifier	15
VF_XI^+	Non-inverting input of the input amplifier	16

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Positive Power Supply	V_{CC}		4.75	5	5.25	V
Negative Power Supply	V_{BB}		-4.75	-5	-5.25	
Power Dissipation (Operating)	P_{OPR}	V_{CC} = 5 V	60	80	90	mW
Power Dissipation (Standby)	P_{STBY}	V_{BB} = -5 V	—	5	—	

Table II - TRANSMIT FILTER TRANSFER CHARACTERISTICS
(V_{CC}=5 V ± 5%, V_{BB}=-5 V ± 5%, $BCLK_X$=$MCLK_R$=1.544 MHz, T_A=25°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Gain (Relative to Gain at 1020 Hz) Input Amplifier Set to Unit Gain	G_{RX}	50 Hz	—	-33	—	dB
		60 Hz	—	-30	—	
		200 Hz	—	-1.1	—	
		300 to 3000 Hz	—	±0.1	—	
		3400 Hz	—	-0.6	—	
		4000 Hz	—	-14.6	—	
		4600 Hz	—	-34	—	

Table III - RECEIVE FILTER TRANSFER CHARACTERISTICS
(V_{CC}=5 V ± 5%, V_{BB}=-5 V ± 5%, $BCLK_R$=$MCLK_X$=1.544 MHz, V_{IN} =0 dBmO@T_A=25°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Receive Gain (Relative to Gain at 1020 Hz) (Includes sin X/X Compensation)	G_{RR}	100 Hz	—	0.01	—	dB
		400 Hz	—	0.01	—	
		2000 Hz	—	0.04	—	
		3000 Hz	—	-0.05	—	
		3400 Hz	—	-0.6	—	
		4000 Hz	—	-14.3	—	
		4600 Hz	—	-33	—	

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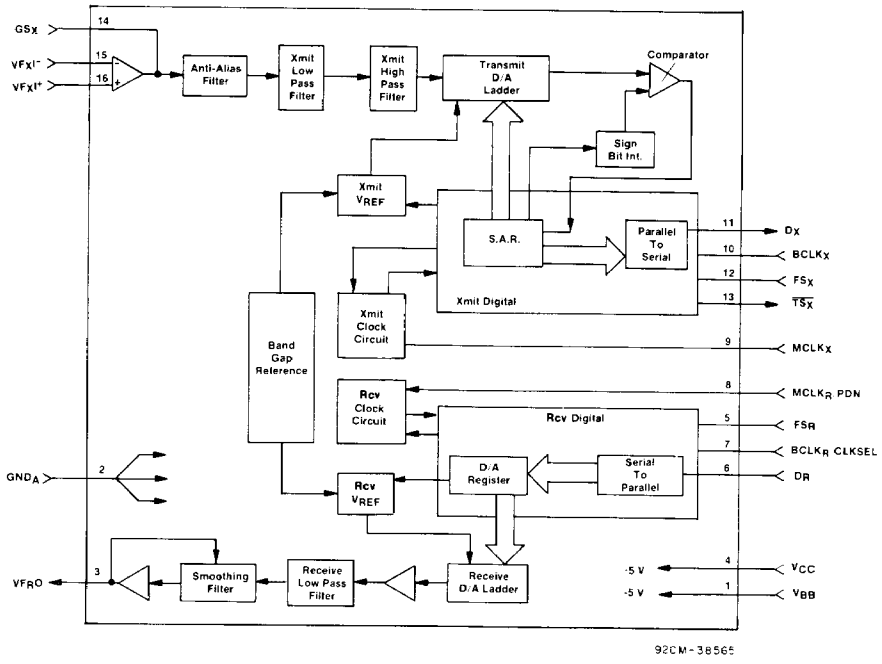

Fig. 1 - Functional block diagram - full-feature PCM CODEC.

LOOP-AROUND FILTER TRANSFER CHARACTERISTICS
(V_{CC}=5 V ± 5%, V_{BB}=-5 V ± 5%, $BCLK_R$=$BCLK_X$=$MCLK_X$=1.544 MHz, V_{IN}=0 dBmO @T_A=25° C)
D_X connected to D_R

CHARACTERISTIC	CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Frequency Response End-to-End Measurement (Loop-around)	50 Hz	—	-33	—	dB
	60 Hz	—	-30	—	
	180 Hz	—	-2.7	—	
	200 Hz	—	-1.1	—	
	300 Hz	—	0.17	—	
	1020 Hz	—	0.01	—	
	3300 Hz	—	0.19	—	
	3400 Hz	—	-1.12	—	
	4 kHz	—	-30	—	
	4.6 kHz	—	-74	—	

DISTORTION CHARACTERISTICS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Signal to Total Distortion Xmit or R_{CV}	STD_X, STD_R	Level +3 dBmO	33	—	—	dBC
		0 to -30 dBmO	36	—	—	
		-40 dBmO	29	—	—	
		-45 dBmO	25	—	—	
Single Frequency Distortion Xmit or R_{CV}	SFD_X, SFD_R		—	-45	—	dBC
Intermodulation (End-to-End Measurement) 2-Tone	IMD		—	-56	—	dB

ABSOLUTE AND ENVELOPE DELAY DISTORTION CHARACTERISTICS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Absolute Delay	t_{DAX}	f = 1600 Hz	—	280	—	μs
Transmit Envelope Delay Relative to D_{AX}	t_{DEX}	f = 500-600 Hz	—	170	—	
		f = 600-1000 Hz	—	70	—	
		f = 1000-2600 Hz	—	70	—	
		f = 2600-2800 Hz	—	90	—	
Receive Absolute Delay	t_{DAR}	f = 1600 Hz	—	180	—	
Receive Envelope Delay Relative to D_{AR}	t_{DER}	f = 500-600 Hz	—	30	—	
		f = 600-1000 Hz	—	30	—	
		f = 1000-2600 Hz	—	60	—	
		f = 2600-2800 Hz	—	110	—	

PIN FUNCTION AND DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1	V_{BB}	Negative power supply, V_{BB} = -5 V ± 5%
2	GND_A	Analog ground. All signals referenced to this pin.
3	VF_RO	Analog output of RECEIVE FILTER
4	V_{CC}	Positive power supply, V_{CC} = +5 V ± 5%
5	FS_R	Receive Frame Sync Pulse which enables $BCLK_R$ to shift PCM Data into D_R. FS_R is an 8-kHz PULSE TRAIN.
6	D_R	Receive Data Input. PCM Data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/CLKSEL	The Bit Clock which shifts data into D_R after the Frame sync leading edge, may vary from 64 kHz to 4.16 MHz. Alternatively, the leading edge may be a logic input which selects either 1.536 MHz or 1.544 MHz or 2.048 MHz for Master Clock in synchronous mode and $BCLK_X$ is used for both Transmit and Receive directions.
8	$MCLK_R$/PDN	Receive Master Clock. Must be 1.536 MHz or 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$ but should be synchronous with $MCLK_X$ for best performance. When this pin is continuously connected low, $MCLK_X$ is selected for all internal timing. When this pin is continuously connected high, the device is power down.
9	$MCLK_X$	Transmit Master Clock. Must be 1.536 MHz or 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The Bit Clock which shifts out the PCM Data on D_X. May vary from 64 kHz to 4.16 MHz but must be synchronous with $MCLK_X$.
11	D_X	The TRI-STATE PCM Data Output which is enabled by FS_X.
12	FS_X	Transmit Frame Sync Pulse input which enables $BCLK_X$ to shift out the data on D_X. FS_X is an 8-kHz PULSE TRAIN.
13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Transmit gain adjust
15	VF_XI^-	Inverting input of the transmit input amplifier
16	VF_XI^+	Non-inverting input of the transmit input amplifier

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FUNCTIONAL DESCRIPTION

CD22354 is pin- and function-compatible to TP3054.

CD22357 is pin- and function-compatible to TP3057.

Power-Up

When power is first applied, the Power-On reset circuitry initializes the CODEC and places it in a Power-Down mode.

To power up the device, there are two modes available.

1. A logical zero at pin 8 will power up the device provided FS_X or FS_R pulses are present.
2. Alternatively, a clock ($MCLK_R$) must be applied to pin 8 and FS_X or FS_R pulses must be present.

Power-Down

Two power-down modes are available.

1. A logical 1 at pin 8 after 1 ms will power down the device.
2. Alternatively, hold both FS_X and FS_R continuously low, the device will power down approximately 1 ms after the last FS_X or FS_R pulse.

Synchronous Operation

The same master clock and bit clock should be used for the receive and transmit sections. $MCLK_X$ (pin 9) is used to provide the master clock for the transmit section. The receive section will use the same master clock if the $MCLK_R$/PDN (pin 8) is grounded (synchronous operation), or at V_{CC} (power-down mode).

The $BCLK_X$ (pin 10) is used to provide the bit clock to the transmit section. In synchronous operation, this bit clock is used for the receive section if $MCLK_R$/PDN (pin 8) is grounded. $BCLK_R$/CLKSEL (pin 7) is then used to select the proper internal frequency division for 1.544 MHz, 1.536 MHz or 2.048 MHz operation. See Table IV for 1.544 MHz operation. The device automatically compensates for the 193rd clock pulse each frame.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the leading edge of the $BCLK_X$. After 8 bit-clock periods, the tristate D_X output is returned to a high impedance state. With a FS_R pulse PCM data is latched via the D_R input on the negative edge of the $BCLK_X$.

FS_X and FS_R must be synchronous with $MCLK_X$. For 1.544-MHz operation, the device automatically compensates for 193rd clock pulse each frame.

Table IV - CLOCKING OPTIONS

$BCLK_R$/ CLKSEL	Master Clock Frequency Selected		$MCLK_R$/ PDN
	CD22354	CD22357	
Clocked	1.536 MHz or 1.544 MHz	2.048 MHz	Clocked/0
0	2.048 MHz	1.536 MHz or 1.544 MHz	0
1(or open circuit)	1.536 MHz or 1.544 MHz	2.048 MHz	0

Asynchronous Operation

For asynchronous operation separate transmit and receive clocks may be applied.

For CD22357, the $MCLK_X$ and $MCLK_R$ must be 2.048 MHz and for CD22354 must be 1.536 MHz or 1.544 MHz. These clocks may not be synchronous. However, for best transmission performance it is recommended that $MCLK_X$ and $MCLK_R$ should be synchronous.

For 1.544-MHz operation the device automatically compensates for the 193rd clock pulse each frame. FS_X must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R must be synchronous with $BCLK_R$.

Short-Frame Synchronous Operation

When the power is first applied, the power initialization circuitry places the CODEC in a short-frame synchronous mode. In this mode both frame sync pulses must be 1 bit-clock period long, with timing relationship shown in Fig. 2.

With FS_X high during falling edge of the $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X tristate output buffer, which will output the sign bit. The following rising seven edges clock out the remaining seven bits, and the next falling edge disables the D_X output.

With FS_R high during the falling edge of the $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge latches in the sign bit. The following seven edges latch in the seven remaining bits.

Long-Frame Synchronous Operation

In this mode of operation, both the frame sync pulses must be three or more bit-clock periods long with timing relationship shown in Fig. 3.

Based on the transmit frame sync FS_X, the CODEC will sense whether short- or long-frame synchronous pulses are being used.

For 64-kHz operation the frame sync pulse must be kept low for a minimum of 160 ns.

The D_X tristate output buffer is enabled with the rising edge of FS_X or the rising edge of the $BCLK_X$, whichever comes later and the first bit clocked out is the sign bit. The following seven rising edges of the $BCLK_X$ clock out the remaining seven bits. The D_X output is disabled by the next falling edge of the $BCLK_X$ following the 8th rising edge or by FS_R going low whichever comes later.

A rising edge on the receive frame sync, FS_R, will cause the PCM data at D_R to be latched in on the next falling edge of the $BCLK_R$. The remaining seven bits are latched on the successive seven falling edges of the bit-clock ($BCLK_X$ in synchronous mode).

Transmit Section

The transmit section consists of a gain-adjustable input op-amp, an anti-aliasing filter, a low-pass filter, a high-pass filter and a compressing A/D converter. The input op-amp drives a RC active anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides 30-dB attenuation (minimum) at the sampling frequency. From this filter the signal enters a 5th order low-pass filter clocked at 128 kHz, followed by a 3rd order high-pass filter clocked at 32 kHz. The output of the high-pass filter directly drives the encoder capacitor ladder at an 8-kHz sampling rate. A precision voltage reference is trimmed in manufacturing to provide an input overload of nominally 2.5-V peak. Transmit frame sync pulse, FS_X, controls the succesive approximation analog to digital conversion process. The 8-bit PCM data is clocked out at D_X by the $BCLK_X$.

$BCLK_X$ can be varied from 64 kHz to 4.1 MHz.

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Receive Section

The receive section consists of an expanding D/A converter and a low-pass filter which fulfills both the AT&T D3/D4 specifications and CCITT recommendations. PCM data enters the receive section at D_R upon the occurrence of FS_R, Receive Frame sync pulse. $BCLK_R$, Receive Data Clock, which can range from 64 kHz to 4.1 MHz, clocks the 8-bit PCM data into the receive data register. A D/A conversion is performed on the 8-bit PCM data and the corresponding analog signal is held on the D/A capacitor ladder. This signal is transferred to a switched capacitor low-pass filter clocked at 128 kHz to smooth the sample-and-hold signal as well as to compensate for the SIN X/X distortion.

The filter is then followed by a second order Sallen and Key active filter capable of driving a 600-Ω load to a level of 7.2 dBm.

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+5 V ± 5%, V_{BB}=-5 V ± 5%

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Analog Input Resistance	R_{INA}		100	—	—	kΩ
Input Capacitance	C_{IN}	All Logic and Analog Inputs	—	5	—	pF
Input Leakage Current	I_I	V_I = 0 V or V_{CC}	—	—	±1	μA
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Input Voltage	V_{IH}		2	—	—	
Low Level Output Voltage	V_{OL}	I_{OL} = 0.8 mA	—	—	0.4	
High Level Output Voltage	V_{OH}	I_{OH} = -40 μA	2.6	—	—	

A.C. CHARACTERISTICS
Unless otherwise specified, the following conditions apply:

V_{CC} = 5 V dc ± 5%, V_{BB} = -5 V dc ± 5%
GND_A, GND_D = 0 V, F_{FX} = 1020 Hz at 0 dBmO
Transmit input amplifier operating in a unity gain configuration
Temperature = 25°C
Receive output is measure single-ended. All output levels are SIN X/X corrected.

DEFINITION

AMPLITUDE RESPONSE
Absolute Levels Definition:
V_{REF} = -2.5 V dc Nominal 0 dBmO level = 4 dBm into 600 Ω
= 1.2276 V (rms)
Maximum Overload Level:
Voltage reference (V_{REF}) of -2.5 V = 2.5 V μ-Law
= 2.49 V A-Law

ENCODING FORMAT AT D_X OUTPUT

	CD22354 μ-LAW								CD22357 A-LAW (INCLUDES EVEN BIT INVERSION)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0 V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = -Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

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GAIN TRACKING

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Gain Tracking Error	GTX	+3 to -40 dBmO	—	—	±0.25	dB
		-40 to -50 dBmO	—	—	±0.5	
		-50 to -55 dBmO	—	—	±1.2	
Receive Gain Tracking Error	GTR	+3 to -40 dBmO	—	—	±0.15	
		-40 to -50 dBmO	—	—	±0.5	
		-50 to -55 dBmO	—	—	±1.2	

NOISE CHARACTERISTICS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Noise	N_X	VF_XI^-=GND_A	—	12	16	dBrncO
		VF_XI^+=GND_A	—	-74	-68	dBmOp
Receive Noise	N_R	D_R=1111111	—	7	11	dBrncO
			—	-81	—	dBmOp
V_{CC} Power Supply Rejection Transmit	PSRR	VF_XI^+=0 V_{CC}=5 V + (100 mV RMS) f=0 to 50 kHz	35	40	—	dBc
V_{BB} Power Supply Rejection Transmit	PSRR	VF_XI^-=0 V V_{BB}=-5 V + (100 mV RMS) f=0 to 50 kHz	35	40	—	dBc
V_{CC} Power Supply Rejection Receive	PSRR	PCM Code ≡ All 1 Code V_{CC}=5 V + (100 mV RMS) f=0 to 4 kHz	35	40	—	dBc
		=4 to 25 kHz	35	40	—	dB
		=25 to 50 kHz	35	36	—	
V_{BB} Power Supply Rejection Receive	PSRR	PCM Code ≡ All 1 Code V_{BB}=-5 V + (100 mV RMS) f=0 to 4 kHz	35	40	—	dBc
		=4 to 25 kHz	35	40	—	dB
		=25 to 50 kHz	35	36	—	
Cross Talk Transmit to Receive	CT_{XR}	VF_XI^-=0 dBmO @ 1020 Hz	—	-80	—	dB
Cross Talk Receive to Transmit	CT_{RX}	D_R ≡ 0 dBmO @ 1020 Hz, VF_XI^-=0 V	—	-75	—	

TIMING SPECIFICATIONS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Frequency of Master Clocks	$1/t_{PM}$	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin	—	1.536	—	MHz
		$MCLK_X$ and $MCLK_R$	—	1.544	—	
			—	2.048	—	
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160	—	—	ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160	—	—	
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$	—	—	50	
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$	—	—	50	
Set-up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First Bit Clock after the Leading Edge of FS_X	100	—	—	
Period of Bit Clock	t_{PB}		485	488	15,725	
Width of Bit Clock High	t_{WBH}	V_{IH} = 2.2 V	160	—	—	
Width of Bit Clock Low	t_{WBL}	V_{IL} = 0.6 V	160	—	—	
Rise Time of Bit Clock	t_{RB}	t_{PB} = 488 ns	—	—	50	
Fall Time of Bit Clock	t_{FB}	t_{PB} = 488 ns	—	—	50	
Holding Time from Bit Clock Low to Frame Sync	t_{HBF}	Long Frame Only	0	—	—	
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short Frame Only	0	—	—	
Set-up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80	—	—	
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load=150 pF plus 2 LSTTL Loads	0	—	180	
Delay Time to TS_X Low	t_{XDP}	Load=150 pF plus 2 LSTTL Loads	—	—	140	
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DZC}		50	—	165	
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	C_L = 0 pF to 150 pF	20	—	165	
Set-up Time from D_R Valid to $BCLK_{R,X}$ Low	t_{SDB}		50	—	—	
Hold Time from $BCLK_{R,X}$ Low D_R Invalid	t_{HBD}		50	—	—	
Set-up Time from $FS_{X,R}$ to $BCLK_{X,R}$ Low	t_{SF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50	—	—	
Hold Time from $BCLK_{X/R}$ Low to $FS_{X,R}$ Low	t_{HF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100	—	—	
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100	—	—	
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64k Bit/s Operating Mode	160	—	—	

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

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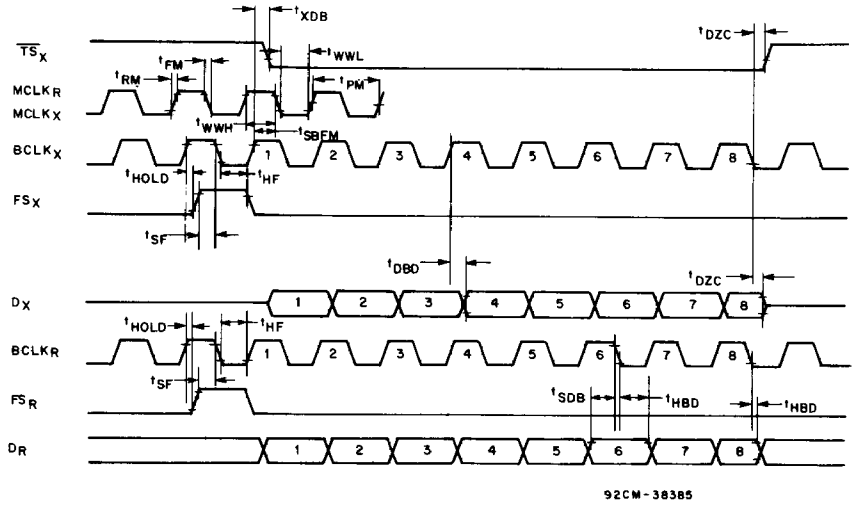

Fig. 2 - Short frame-sync timing.

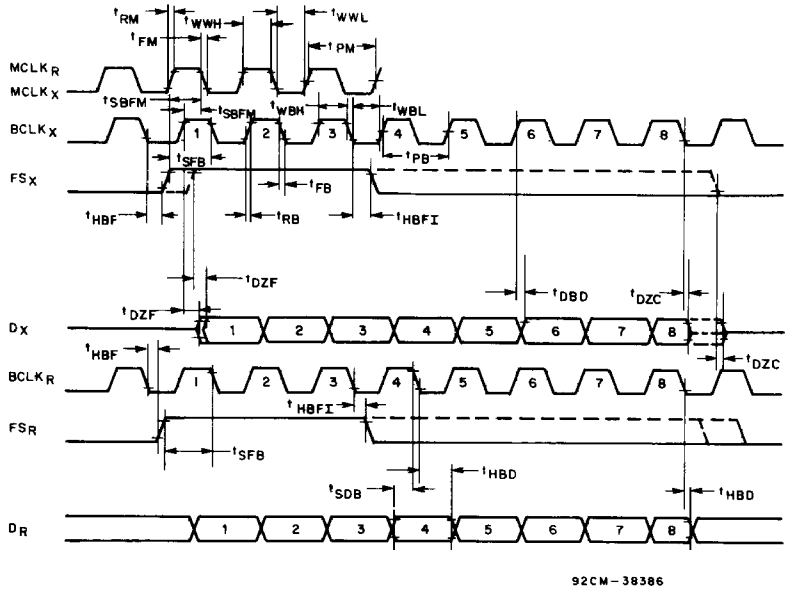

Fig. 3 - Long frame-sync timing.