



ATT1S04 (SEABREEZE) Switch for Ethernet Applications

Features and Benefits

- A circuit switch supporting 12 ports and providing independent connection to 1 of 4 segmented Ethernet environments:
 - Provides collision detection and data path switching for each segment on a per-port basis.
 - All ports are configured via software to allow independent control of port-segment configuration.
- Supports an unlimited number of configurations.
 - Four-bit SEABREEZE identification allows for expansion to 192 ports on four segments (12 ports/board and 16 boards or 24 ports/board and 8 boards are common)
 - Expansion provisions allow for support of more than four segments.
- Integrates miscellaneous board-level circuitry to minimize other components.
 - Provides address decoding for three ATT1RX04 Quad managed repeater devices.
 - Provides a powerup reset, a software-controlled hardware reset to the ATT1RX04s, and/or conditions a system-level hardware reset to the ATT1RX04. Status is provided to indicate when the reset operation is complete.
- Packaged in a 132-pin BQFP.
- Makes **Switched Ethernet A BREEZE** (SEABREEZE) and reduces time to market.

Description

The ATT1RX04 generation of intelligent hubs (multi-channel or switched hubs) will add redundancy (self-healing) and the ability to perform load balancing by controlling the bandwidth available to the desktop. In a nonswitching hub, the 10 Mbits/s bandwidth is shared among all stations connected to the network. This sharing of a single collision domain severely

reduces the bandwidth available to a single user. In a switched hub, several separate Ethernet segments or collision domains are made available, each providing 10 Mbits/s to as few as two stations.

The SEABREEZE provides the circuit switch and collision handling logic for implementing a 12-port, four-segment circuit switch when used in conjunction with the ATT1RX04. In addition, it provides all the miscellaneous board-level circuitry, including the reset circuitry, and board-level address decoding. The SEABREEZE also provides a board-level reset to the ATT1RX04s that can be controlled by software or hardware. The design allows for a 4-bit hardware-configured board ID.

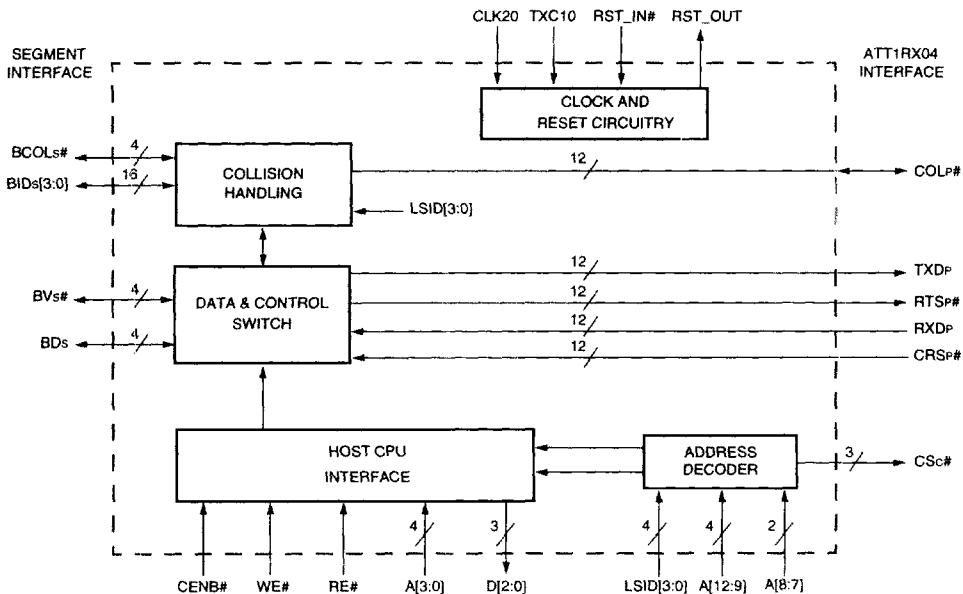
A 12-port, four-segment card would require three ATT1RX04 devices, a SEABREEZE, and the appropriate TP or AUI line interface circuitry (see Figure 2). The host configures the SEABREEZE by using the port configuration registers. The bits in the registers are used to assign the single-port interface signals to the appropriate segment. The address decoder is used to select the device of interest. The interrupt controller advises the host when there is a change in system status. A 24-port, four-segment card would require six ATT1RX04s and two SEABREEZE devices (see Figure 8).

The SEABREEZE is packaged in a 132-pin bumped plastic quad flat pack (BQFP) and is fabricated by using low-power CMOS technology.

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Description (continued)

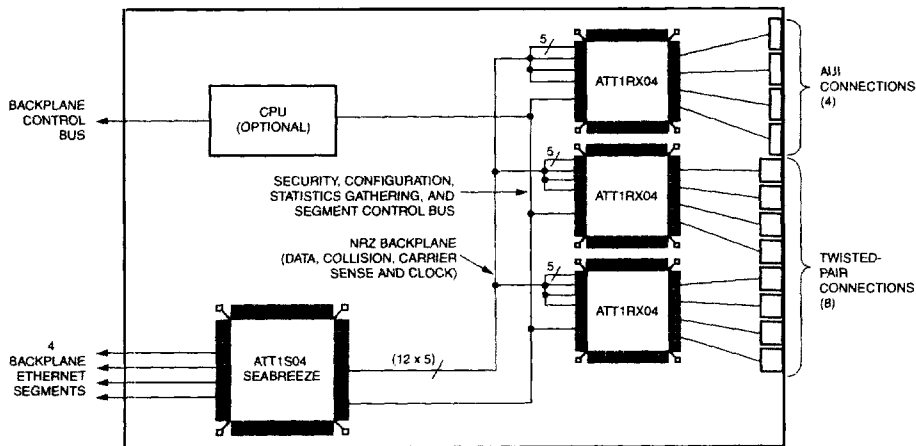


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Legend:
P = 1—12 (1 per port).
S = A—D (1 per segment).
C = 1—3 (1 per ATT1RX04 chip).

Figure 1. Block Diagram

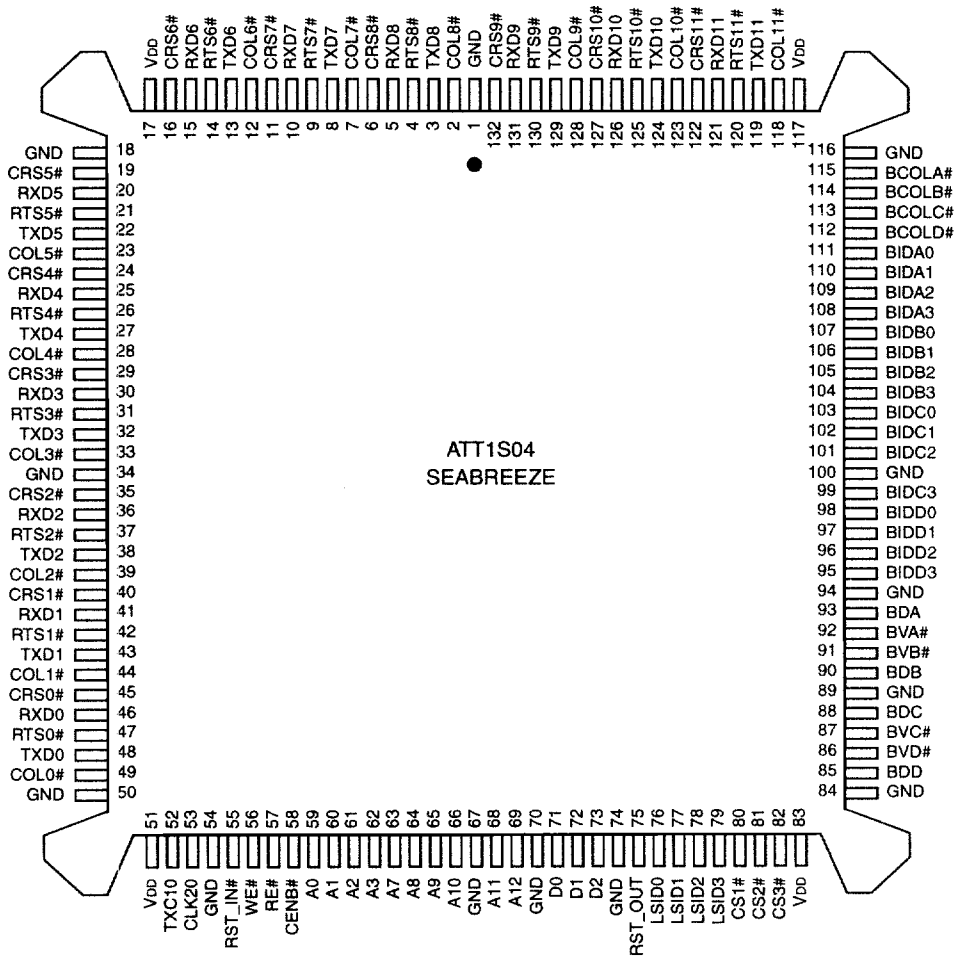


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Figure 2. 12-Port, Four-Segment Card

Pin Information

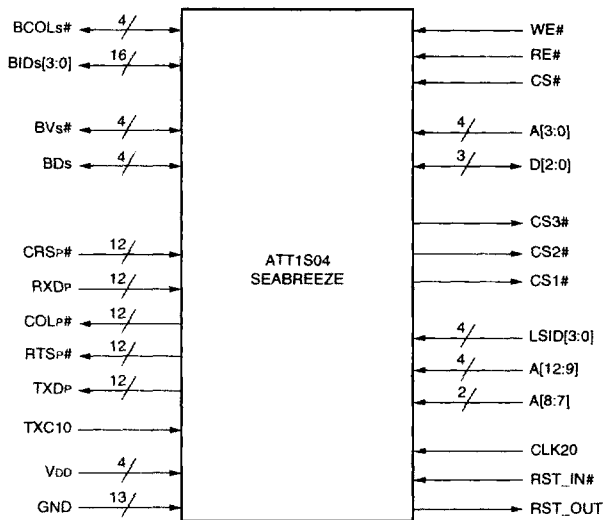
SECTION 2.6



5-3949F

Figure 3. Package Pin Function Diagram (Top View 132-Pin BQFP)

Pin Information (continued)



5-3958C

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Legend:

P = 1—12 (1 per port).

S = A—D (1 per segment).

Figure 4. Pin Configuration (132 Pins)

Table 1. Pin Descriptions—ATT1RX04 Port Interface Pins

Pin	Symbol (p = 1 to 12)	Type (Level)	Name/Function															
80 81 82	CS1# CS2# CS3#	0 (CMOS)	Chip Selects for ATT1RX04. The SEABREEZE decodes A[8:7] when A[12:9] match the LSID[3:0] to generate chip selects for the ATT1RX04s and for the internal registers of the SEABREEZE. <table border="0"> <tr> <td>A8</td> <td>A7</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>— Internal registers of SEABREEZE.</td> </tr> <tr> <td>0</td> <td>1</td> <td>— CS1# is asserted.</td> </tr> <tr> <td>1</td> <td>0</td> <td>— CS2# is asserted.</td> </tr> <tr> <td>1</td> <td>1</td> <td>— CS3# is asserted.</td> </tr> </table>	A8	A7		0	0	— Internal registers of SEABREEZE.	0	1	— CS1# is asserted.	1	0	— CS2# is asserted.	1	1	— CS3# is asserted.
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0	0	— Internal registers of SEABREEZE.																
0	1	— CS1# is asserted.																
1	0	— CS2# is asserted.																
1	1	— CS3# is asserted.																
122 127 132 6 11 16 19 24 29 35 40 45	CRS11# CRS10# CRS9# CRS8# CRS7# CRS6# CRS5# CRS4# CRS3# CRS2# CRS1# CRS0#	1 (CMOS)	Carrier Sense (Active-Low). These pins operate as active-low inputs from the ATT1RX04 to indicate to the switch controller that data is present on RXD and should be accepted for distribution. Under collision conditions, these pins also indicate the presence of receive energy. The signal is sampled on the rising edge of CLK20 when TXC10 is high (see TXC10 pin description below).															

Pin Information (continued)

Table 1. Pin Descriptions—ATT1RX04 Port Interface Pins (continued)

Pin	Symbol (p = 1 to 12)	Type (Level)	Name/Function
121 126 131 5 10 15 20 25 30 36 41 46	RXD11 RXD10 RXD9 RXD8 RXD7 RXD6 RXD5 RXD4 RXD3 RXD2 RXD1 RXD0	I (CMOS)	Receive Data. These pins operate as the receive data from the ATT1RX04 to the switch matrix. The signal is sampled on the rising edge of CLK20 when TXC10 is high (see TXC10 pin description below).
118 123 128 2 7 12 23 28 33 39 44 49	COL11# COL10# COL9# COL8# COL7# COL6# COL5# COL4# COL3# COL2# COL1# COL0#	O (CMOS)	Collision Detected (Active-Low). These pins operate as collision outputs from the switch controller to the ATT1RX04. This signal is driven on the rising edge of CLK20 when TXC10 is high. COLp# is only asserted when RTSp# is asserted and COLp# is asserted for a minimum of 200 ns.
120 125 130 4 9 14 21 26 31 37 42 47	RTS11# RTS10# RTS9# RTS8# RTS7# RTS6# RTS5# RTS4# RTS3# RTS2# RTS1# RTS0#	O (CMOS)	Request to Send (Active-Low). These pins operate as active-low outputs to indicate that the data on TXD is valid and should be transmitted by the repeater. This signal is driven on the rising edge of CLK20 when TXC10 is high.
119 124 129 3 8 13 22 27 32 38 43 48	TXD11 TXD10 TXD9 TXD8 TXD7 TXD6 TXD5 TXD4 TXD3 TXD2 TXD1 TXD0	O (CMOS)	Transmit Data. These pins operate as the transmit data from the SEABREEZE switch matrix to the ATT1RX04. This signal is driven on the rising edge of CLK20 when TXC10 is high.

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Pin Information (continued)

Table 2. Pin Descriptions—Segment Interface Pins

Pin	Symbol	Type	Name/Function
115 114 113 112	BCOLA# BCOLB# BCOLC# BCOLD#	I/O (CMOS)	Backplane Collision (Open-Drain Output). This signal is driven when the collision circuitry determines a collision has occurred. The signal is also sensed to detect collisions reported from other devices. When this signal is low, the SEABREEZE drives COLp# to all ports assigned to that segment.
92 91 87 86	BVA# BVB# BVC# BVD#	I/O (CMOS)	Backplane Data Valid (Open-Drain Output). This is an active-low signal that indicates data on the backplane is valid. The signal is also sensed to determine when other devices are transmitting data. When BVs# is low, RTSp# is driven to all ports assigned to that segment.
93 90 88 85	BDA BDB BDC BDD	I/O (CMOS)	Backplane Data (Open-Drain Output). This is the backplane data. It is clocked on the rising edge of CLK20 when TXC10 is low. Data is sampled from this pin and driven on TXDp to all ports assigned to that segment when BVs# is low.
108—111 104—107 99, 101—103 95—98	BIDA[3:0] BIDB[3:0] BIDC[3:0] BIDD[3:0]	I/O (CMOS)	Backplane Segment ID (Open-Drain Output). This is the ID of the SEABREEZE that is driving data to the backplane. The collision circuitry compares what it drives on this pin with what it inputs on this same pin to determine when a collision is occurring among SEABREEZEs.

Table 3. Pin Descriptions—Reset, Clocks, and Power

Pin	Symbol	Type	Name/Function
55	RST_IN#	I (TTL)	Reset In (Schmitt Trigger). A low on this pin causes the SEABREEZE to reset and causes all outputs except RST_OUT to be 3-stated; RST_OUT is asserted. RST_IN# must be high for normal operation. CLK20 must be free-running during reset. This can be used to invert an active-low system reset and/or to elongate a reset signal to meet the ATT1RX04 reset timing requirements. It can also be used in production tests to hold the ATT1RX04s in RESET for LED tests. (Alternately, software could program each ATT1RX04 to be configured for the LED test mode.) RST_OUT remains high for as long as RST_IN# is low and is held high for 2 μ s after RST_IN# is deasserted. An internal 50 k Ω pull-up resistor is present.
75	RST_OUT	O (CMOS)	Reset Out. This is an active-high output intended to be used to reset the ATT1RX04s. Reset is asserted high with the appropriate timing (see Timing Characteristics section) on powerup, when RST_IN# is asserted, or when a reset is requested by the host processor by writing a value of '101' to the internal register 13 (A[3:0] = 1101). RST_OUT remains high for as long as RST_IN# is low. RST_OUT will be deasserted 2 μ s after RST_IN# is deasserted. Note: Register 13 is self-clearing, i.e., register 13 is configured back to its default value of '010' when RST_OUT has been asserted for a minimum of 2 μ s.
53	CLK20	I (TTL)	System Clock. 20 MHz \pm 0.01%, 50% nominal, 40%/60% worst-case, duty cycle. Data to/from the ATT1RX04 is clocked on the rising edge of CLK20 when TXC10 is high.
52	TXC10	I (TTL)	Data Clock. 10 MHz. Data to/from the ATT1RX04 is clocked on the rising edge of CLK20 when TXC is high.
51, 83, 117, 17	VDD (4)	—	+5 V Digital Supply. All pins must be connected.
1, 18, 34, 50, 54, 67, 70, 74, 84, 89, 94, 100, 116	GND (13)	—	Ground.

Pin Information (continued)

Table 4. Pin Descriptions—Host Interface Pins

Pin	Symbol	Type (Level)	Name/Function															
56	WE#	I (TTL)	Write Enable (Active-Low). A low on this pin when an internal register is selected and CS# is low initiates a transfer of data from the system bus (D2—D0) to the internal register referenced by A3—A0. The data must be valid before the rising edge of WE# and is latched internally on that rising edge.															
57	RE#	I (TTL)	Read Enable (Active-Low). A low on this pin when an internal register is selected and CS# is low initiates a transfer of data from the internal SEABREEZE register referenced by A3—A0 to the system bus (D2—D0). The data on D2—D0 remains valid until after the rising edge of RE#.															
58	CENB#	I (TTL)	Chip Enable. This signal, when low, enables the internal address decoder that is used to generate CS#[3:1] and to select internal registers of the SEABREEZE.															
59 60 61 62	A0 A1 A2 A3	I (TTL)	Host Processor Interface Address Bus. The host processor selects the desired internal ATT1RX04 register for reading or writing via these pins.															
63 64	A7 A8	I (TTL)	Chip Select Decode. The SEABREEZE decodes these pins when CS# is low and A[12:9] match the LSID[3:0] to generate chip selects for the ATT1RX04s and for the internal registers of the SEABREEZE. <table border="0" style="margin-left: 20px;"> <tr> <td>A8</td> <td>A7</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>— Internal registers of SEABREEZE.</td> </tr> <tr> <td>0</td> <td>1</td> <td>— CS1# is asserted.</td> </tr> <tr> <td>1</td> <td>0</td> <td>— CS2# is asserted.</td> </tr> <tr> <td>1</td> <td>1</td> <td>— CS3# is asserted.</td> </tr> </table>	A8	A7		0	0	— Internal registers of SEABREEZE.	0	1	— CS1# is asserted.	1	0	— CS2# is asserted.	1	1	— CS3# is asserted.
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0	0	— Internal registers of SEABREEZE.																
0	1	— CS1# is asserted.																
1	0	— CS2# is asserted.																
1	1	— CS3# is asserted.																
65 66 68 69	A9 A10 A11 A12	I (TTL)	Address Pins. The signals are used in the address decoder section of this device. In order to activate CSc# or address an internal register, A[12:9] must match LSID[3:0] (A12 = LSID3 . . . A9 = LSID0).															
71 72 73	D0 D1 D2	I/O (TTL/CMOS)	Host Processor Interface Data Bus. Data is transferred between the host processor and the internal SEABREEZE registers via these pins.															
76 77 78 79	LSID0 LSID1 LSID2 LSID3	I (CMOS)	Local SEABREEZE ID. These signals are used in the address decoder section of this device. In order to activate CSc# or address an internal register, A[12:9] must match LSID[3:0] (A12 = LSID3 . . . A9 = LSID0). These inputs also define what is driven on BIDs[3:0] when a SEABREEZE port is asserting control signals on a segment.															

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Principles of Operation

Clocks

Two clocks are required for proper operation of the device. There is one 10 MHz clock that is synchronized to the 20 MHz clock. These two clocks must be in phase throughout the system. The 20 MHz clock is input into the clock pin (CLK20) of the ATT1RX04. The 10 MHz clock is input into the TXC10 lead of the device. This clock is used for gating data to and from the ATT1RX04 as well as synchronizing backplane signals, control, and data. All ATT1RX04 interface signals are controlled by the rising edge of CLK20 when TXC10 is high (i.e., data and control are clocked on the rising edge of CLK20). All segment interface signals are controlled by the rising edge of CLK20 when TXC10 is low. The minimum delay from when CRS# is asserted to when RTS# of the same port is asserted is 400 ns. CLK20 must be free-running during reset.

Resets

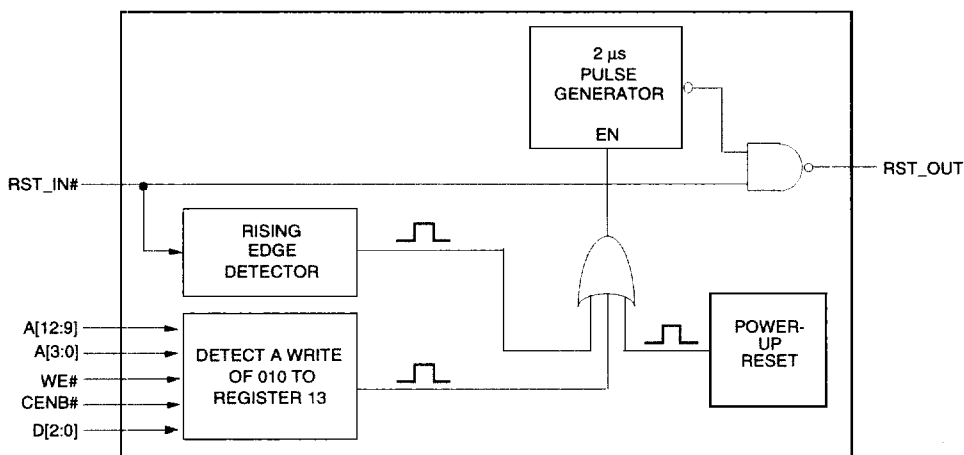
There exist two reset pins on the SEABREEZE, an input and an output. They can be used to invert an active-low system reset and/or to elongate a reset signal to meet the ATT1RX04 reset timing requirements. Figure 5 shows a diagram of the reset functions.

A low on RST_IN# pin causes the SEABREEZE to reset and causes all outputs except RST_OUT to be 3-stated; RST_OUT is asserted when RST_IN# is low. All internal registers of the SEABREEZE are set to their default configurations. That is, all ports default to disabled. RST_IN# must be high for normal operation.

The RST_OUT pin is an active-high output intended to be used to reset the ATT1RX04s. Reset is asserted high with the appropriate timing (see Timing Characteristics section) when RST_IN# is asserted or when a reset is requested by the host processor writing a value of '010' to the internal register 13 (A[3:0] = 1101). Register 13 is self-clearing; that is, bits 2, 1, and 0 are configured to their default value of '101' after RST_OUT is complete. The minimum RST_OUT output is 2 μ s.

RST_OUT remains high for as long as RST_IN# is low. RST_OUT will be deasserted 2 μ s after RST_IN# is deasserted.

CLK20 must be present at all times to allow the device to function properly, including during reset. TXC10 does not have to be present during reset.



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Figure 5. Block Diagram of the Reset Circuit

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Principles of Operation (continued)

Resets (continued)

Two status bits indicate the current state of RST_OUT.

RC0, bit 0 of register 12, indicates the state of the RST_OUT signal. When 1, RST_OUT is high; when 0, RST_OUT is low.

The second status bit, RC1, bit 1 of register 12, is a 1 when RST_OUT is high and stays at 1 for 200 ms after RST_OUT is deasserted. The RC1 status bit can be monitored by software to indicate when the ATT1RX04s are completely reset.

Address Decoder

The SEABREEZE provides address decoding for its own internal register and for up to three ATT1RX04 devices on the same board. Figure 6 shows a block diagram of the address decoding circuitry. The SEABREEZE first determines whether a device associated with its SEABREEZE is being addressed. This is accomplished by comparing the local board ID, LSID[3:0], with the address signals input to A[12:9].

This is defined to be true when:

LSID_3 = A12

LSID_2 = A11

LSID_1 = A10

LSID_0 = A9

Memory allocation is 512 bytes per SEABREEZE device. 128 bytes are needed for each ATT1RX04, and to simplify things, the SEABREEZE internal registers are allocated in the same way. A[6:0] selects the registers within each ATT1RX04 (note SEABREEZE internal registers only use 16 bytes of the assigned 128 bytes that are addressed by A[3:0]). Since A[6:0] are used to address the registers within an ATT1RX04, A[8:7] can be used to distinguish which ATT1RX04 or internal register of the SEABREEZE is being addressed. (Note A[8:7] in Table 4.)

The addressing of SEABREEZE internal registers is described in the Host CPU Interface section.

Table 5 shows a memory map of one SEABREEZE device.

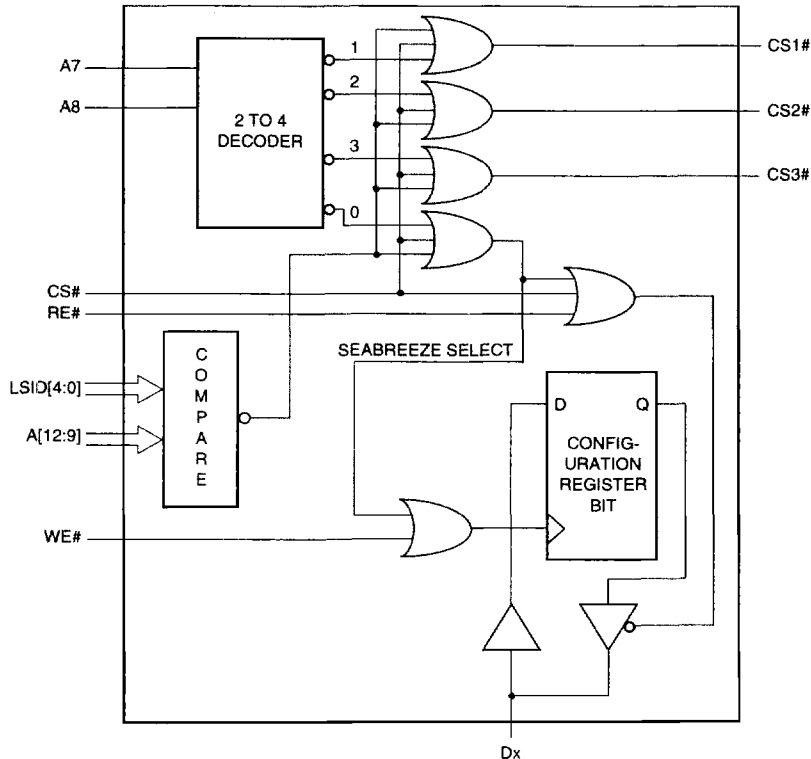
Table 5. Memory Map Allocation for the SEABREEZE

Address											Description		
A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2		A1	A0
A[12:9] = LSID[3:0]				0	0	X	X	X	0	0	0	0	SEABREEZE internal register select (16 bytes used) (128 bytes allocated)
						X	X	X	1	1	1	1	
A[12:9] = LSID[3:0]				0	1	0	0	0	0	0	0	0	ATT1RX04 CS1# (128 bytes)
						1	1	1	1	1	1	1	
A[12:9] = LSID[3:0]				1	0	0	0	0	0	0	0	0	ATT1RX04 CS2# (128 bytes)
						1	1	1	1	1	1	1	
A[12:9] = LSID[3:0]				1	1	0	0	0	0	0	0	0	ATT1RX04 CS3# (128 bytes)
						1	1	1	1	1	1	1	

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Principles of Operation (continued)

Resets (continued)



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Figure 6. Block Diagram of the Address Decoder

Memory Allocation Alternatives

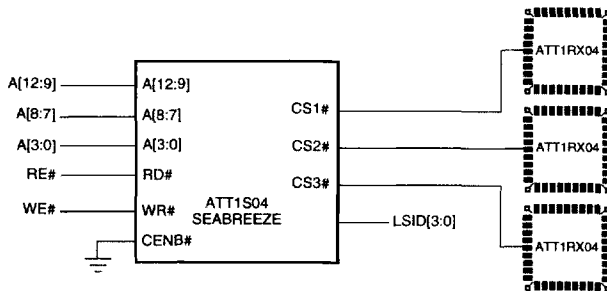
The SEABREEZE is designed to eliminate all external address decoding circuitry for low-end systems. Figure 7 shows the easiest configuration. Each SEABREEZE requires 256 bytes of memory, which includes the memory space of the three associated ATT1RX04 devices. No external address decoding is required if the total system memory allocated is less than or equal to 2^{14} bytes. When more address space is needed, a different approach should be used.

One approach is to add external address decoding. Figure 8 shows an example circuit in which the SEABREEZE and associated ATT1RX04 devices require only 256 bytes of memory but the total memory available is expanded to 2^{20} bytes. In this example, the SEABREEZE or an associated ATT1RX04 is addressed when $A[19:15] = 0$ and $A[12:9] = \text{LSID}[3:0]$.

A second approach is to manipulate the address lines that are connected to the A[12:7] pins of the SEABREEZE. Potentially, A[19:16] to A[12:9] could be connected as shown in Figure 9. In this scenario, each SEABREEZE and associated ATT1RX04 device will use 2^{15} bytes, but total memory available becomes 2^{20} bytes again. This may or may not result in extra memory depending on how many SEABREEZE devices exist in the system.

Principles of Operation (continued)

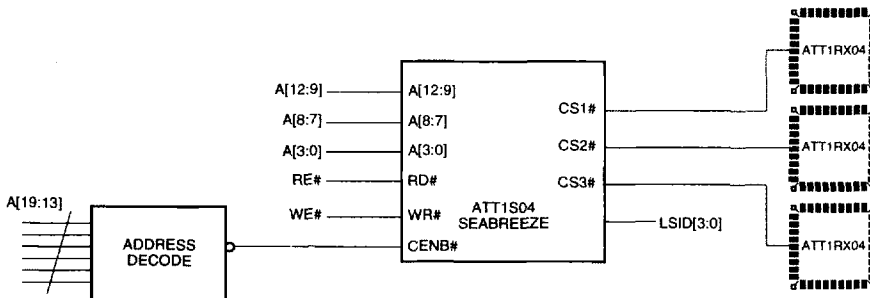
Memory Allocation Alternatives (continued)



5-4085bC

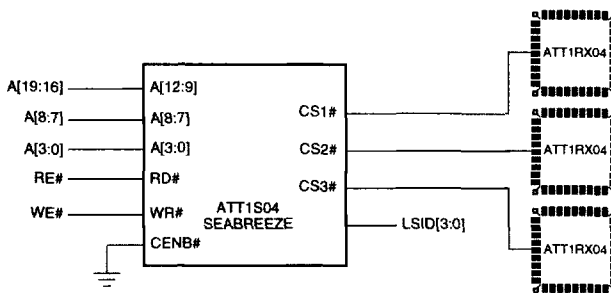
Figure 7. Easiest Memory Allocation

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Figure 8. Optional External Address Decode Circuit



5-4085aC

Figure 9. Alternate Address Map with Easy Memory Allocation

Principles of Operation (continued)

Host CPU Interface

The host interface provides access to the SEABREEZE registers over a 3-bit bidirectional data bus. The host accesses a register by applying the appropriate address and asserting either RE# or WE#.

The SEABREEZE does not expect RE#, WE#, or the address and data buses to be synchronous to CLK20. The interface is completely asynchronous.

Registers and Memory Map

The SEABREEZE contains 15 internal registers addressed by A[3:0]. Twelve are port configuration registers, one is a reset register, and three registers are reserved.

Table 6 provides the register memory association and overview for the repeater register bank.

Table 6. Register Map

Register A[3:0]	Offset*	Description	Access	D2†	D1†	D0†
	Hex					
0	0	Port 0 Configuration Register	RD/WR	P1EN	P1CB1	P1CB0
1	1	Port 1 Configuration Register	RD/WR	P2EN	P2CB1	P2CB0
2	2	Port 2 Configuration Register	RD/WR	P3EN	P3CB1	P3CB0
3	3	Port 3 Configuration Register	RD/WR	P4EN	P4CB1	P4CB0
4	4	Port 4 Configuration Register	RD/WR	P5EN	P5CB1	P5CB0
5	5	Port 5 Configuration Register	RD/WR	P6EN	P6CB1	P6CB0
6	6	Port 6 Configuration Register	RD/WR	P7EN	P7CB1	P7CB0
7	7	Port 7 Configuration Register	RD/WR	P8EN	P8CB1	P8CB0
8	8	Port 8 Configuration Register	RD/WR	P9EN	P9CB1	P9CB0
9	9	Port 9 Configuration Register	RD/WR	P10EN	P10CB1	P10CB0
10	A	Port 10 Configuration Register	RD/WR	P11EN	P11CB1	P11CB0
11	B	Port 11 Configuration Register	RD/WR	P12EN	P12CB1	P12CB0
12	C	Reset Complete Status	RD	Reserved	RC1	RC0
13	D	Software Reset	RD/WR	SWR2§	SWR1§	SWR0§
14	E	Reserved†	—	—	—	—
15	F	Reserved†	—	—	—	—

* Address pins A3 to A0.

† Reserved registers are for internal use and should not be written. Reserved bits should be programmed to zero.

‡ All bits default to zero except SWR2 and SWR0. SWR2 and SWR0 default to a 1 on powerup and when RST_IN# is asserted.

§ Self-clearing.

Principles of Operation (continued)

Host CPU Interface (continued)

Interrupts

Table 7. Register Bit Descriptions

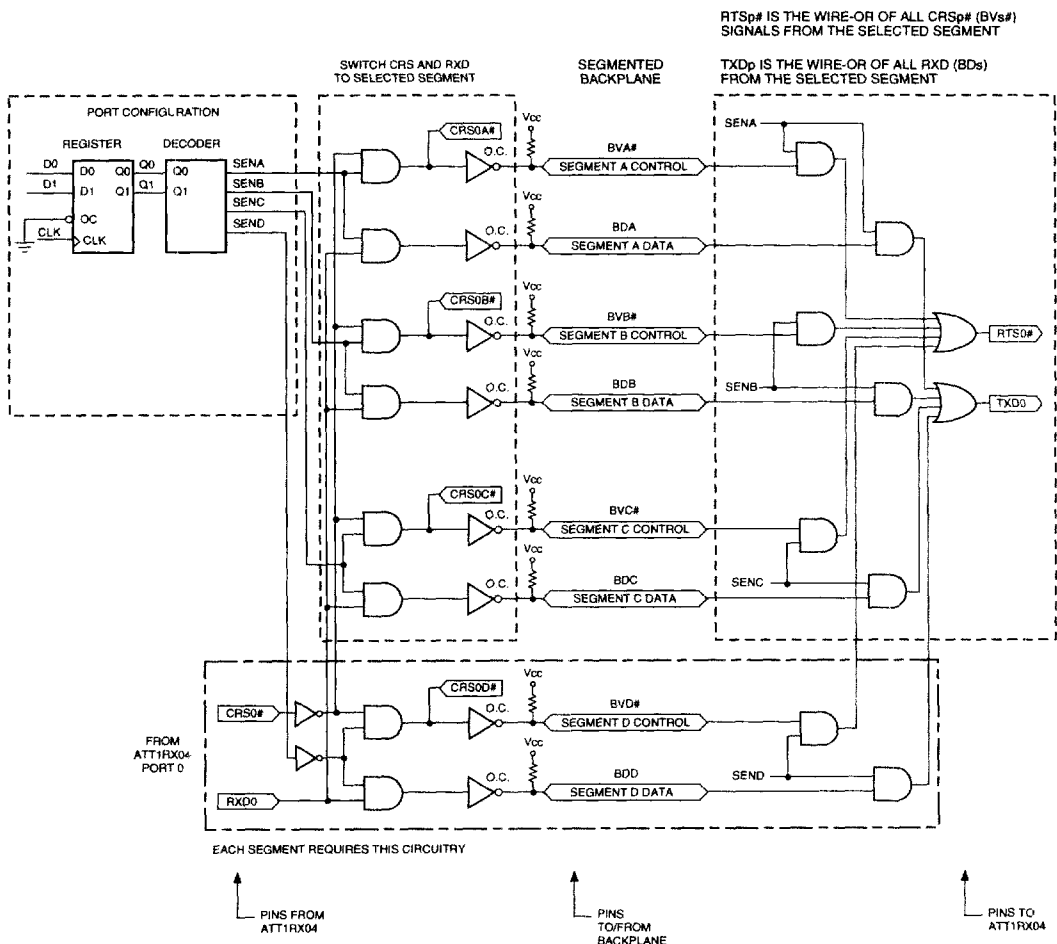
Symbol	Description															
Reserved	Program to zero for normal operation.															
SWR[2:0]	Software Reset Bit. SWR[2:0] must be programmed to '010' to cause a 2 μ s pulse on RST_OUT. The bits are self-clearing at the end of the reset. The bits can be read back to determine when the reset is completed. These bits default to '101'. These bits do not reset the SEABREEZE itself.															
RC0	RST_OUT Current State. RC0, bit 0 of register 12 indicates the state of the RST_OUT signal. When 1, RST_OUT is high; when 0, RST_OUT is low.															
RC1	ATT1RX04 Reset Complete. RC1, bit 1 of register 12, is a 1 when RST_OUT is high and stays at 1 for 200 ms after RST_OUT is deasserted. The RC1 status bit can be monitored by software to indicate when the ATT1RX04s are completely reset.															
PpEN	Port p (1-12) Enable. This bit is used to enable ports. When zero (default) the port is disabled. This means the inputs on CRSp# and RXDp# are ignored and TXDp, RTSp#, and COLp# are 3-stated. When programmed to one, the port is configured as specified by PpCB0 and PpCB1.															
PpCB[1:0]	<p>Port p Configuration Register Bits. These bits are used to configure the port as follows:</p> <table border="0"> <tr> <td>PpCB1</td> <td>PpCB0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Port p is assigned to segment A.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Port p is assigned to segment B.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Port p is assigned to segment C.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Port p is assigned to segment D.</td> </tr> </table> <p>These bits default to zero on powerup or when RST_IN# is low. The design ensures a smooth transition between segments. The transition occurs during the interframe gap (IFG). It is first disabled from its currently assigned segment during the IFG of that segment. It then waits for the IFG of the new segment to add the port.</p> <p>Note: The IFG is when both CRSp# and RTSp# are deasserted.</p>	PpCB1	PpCB0		0	0	Port p is assigned to segment A.	0	1	Port p is assigned to segment B.	1	0	Port p is assigned to segment C.	1	1	Port p is assigned to segment D.
PpCB1	PpCB0															
0	0	Port p is assigned to segment A.														
0	1	Port p is assigned to segment B.														
1	0	Port p is assigned to segment C.														
1	1	Port p is assigned to segment D.														

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Principles of Operation (continued)

Data and Control Switch

The data and control switch connects port signals to the appropriate segment signals. Figure 10 shows the signal flow of the data and switch control circuitry for one port. For each port, there is a port configuration register and an associated decoder that indicate which segment the port should be connected to. There is circuitry to switch CRSp# and RXDp to the selected segment. The output buffers are open collector and connected to the backplane. Figure 11 shows the buffer structure. All backplane signals represent a system-level wire-AND of all the individual port signals. The RTS# and TXD signals end up being a wire-AND of all the RXDs from all the ports on the selected segment. Figure 10 is conceptual: it does not show the clocking and it does not detail transitioning from one segment to another.



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Figure 10. Data and Switch Control for One Port

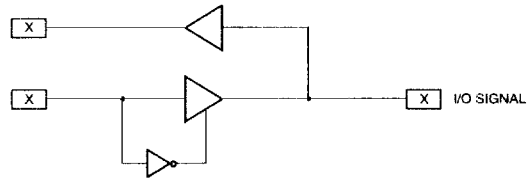
Principles of Operation (continued)

Collision Handling

A conceptual block diagram of the collision circuitry is shown in Figure 12. The collision handling circuitry drives the COLp# signal to each port of the ATT1RX04. COLp# is asserted when the backplane collision signal, BCOLs#, of the segment to which the port is assigned is asserted. COLp# is only asserted when RTSp# is asserted and COLp# is asserted for a minimum of 200 ns.

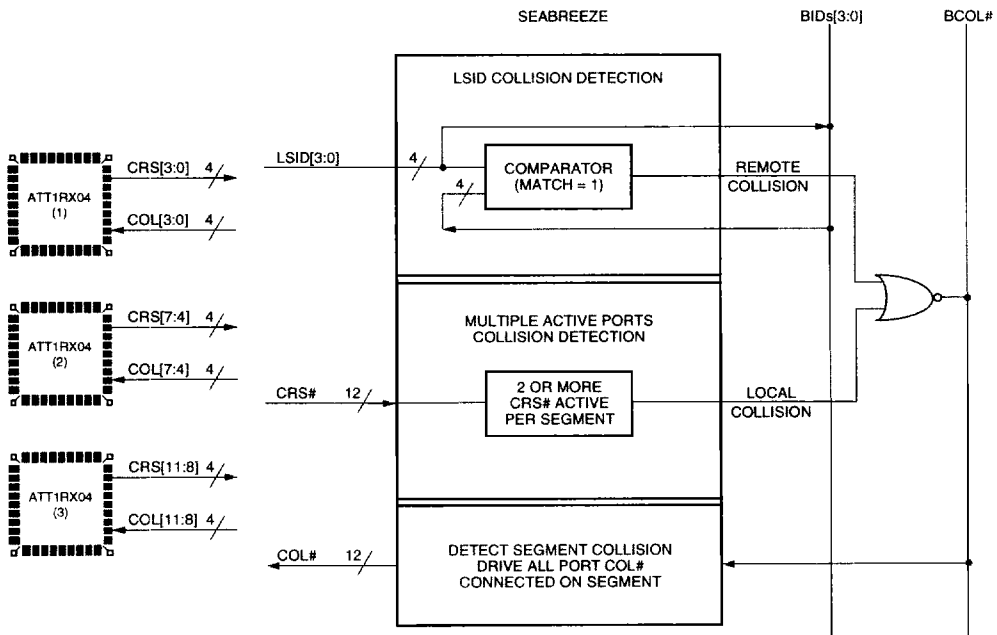
The collision handling circuitry also drives the BCOLs# signal. BCOLs# is an open-drain output so all devices connected to that segment of the backplane connect to the same signal. BCOLs# is also sensed by the SEABREEZE to detect when it is driven. The buffer structure is shown in Figure 11. The SEABREEZE drives BCOLs# when a local collision is detected (i.e., there are multiple active ports) or when a remote collision is detected, i.e., collision is detected between the SEABREEZE device and some other device on the backplane.

Each port on each board must generate a unique port identification bit pattern, which is comprised of the LSID[3:0] and an internally generated port ID. The internally generated port ID is determined by the pins that the signals are received on. This is transmitted to the identification (ID) bus when the CRSp# becomes active. Active repeaters must simultaneously compare the ID bus data to the LSID and the port ID. If two users are on the bus, at least one will not match and BCOLs# will be asserted to reflect a collision. Note that part of this ID bus remains internal to the SEABREEZE and is used to determine a local collision. Another part is driven to the segment BID[4:0] so that different SEABREEZE devices can signal a collision between themselves.



5-4080C

Figure 11. I/O Buffer Structure of Backplane Signal



5-4079C

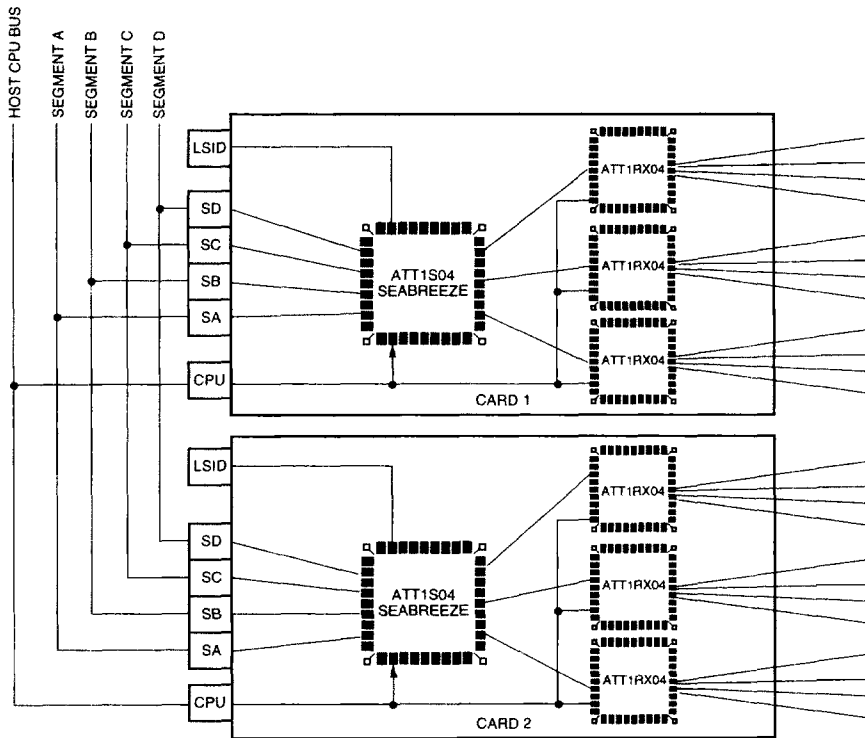
Figure 12. Collision Circuitry

Principles of Operation (continued)

Application Examples

Figure 13 shows multiple ATT1RX04s on a single card and shows two cards and four segments connected through a backplane connector.

The ATT1RX04s provide the TP or AUI interface and the repeater functions. The host assigns each port to one of the four segments. The SEABREEZE then does the collision handling and segment switching. Figure 14 shows the connection between the ATT1RX04 and the SEABREEZE. These two cards could just as easily be on one card; however, two different LSIDs would be needed. (In that case, the backplane connector would assign LSID[3:0] and the card would hardwire LSID[0] to a 1 for the one SEABREEZE and to a 0 for the other SEABREEZE.)



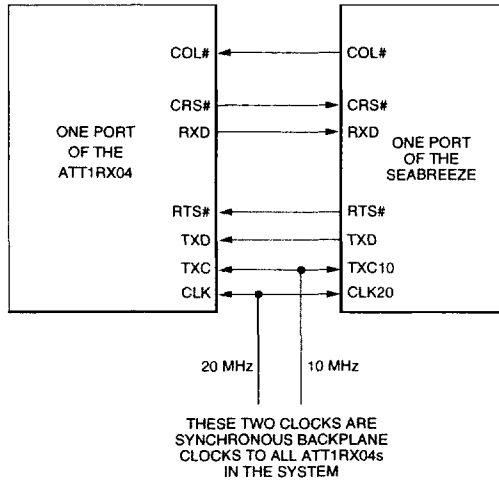
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Figure 13. Cascading Cards

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Principles of Operation (continued)

Application Examples (continued)



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5-3961C

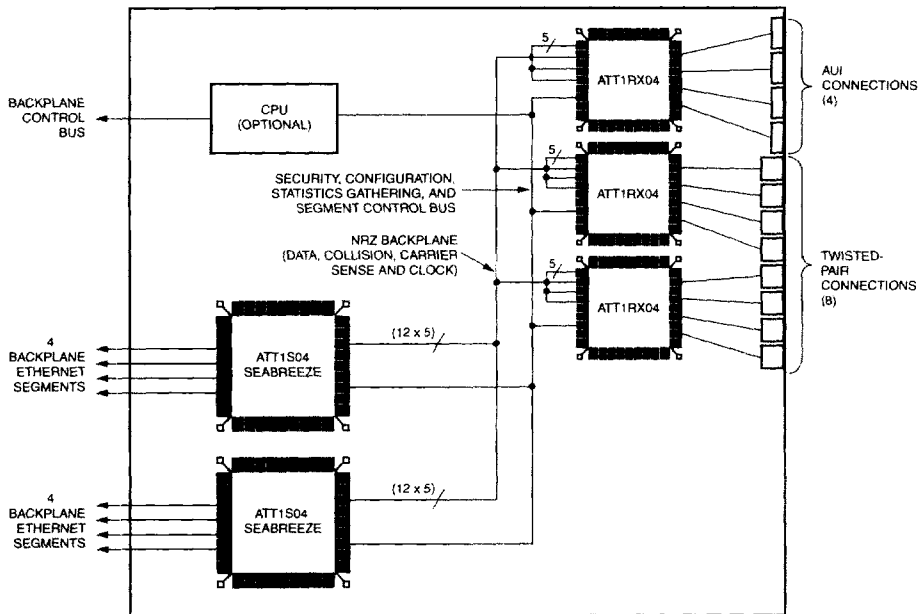
Figure 14. Typical ATT1RX04 Connection Diagram

Principles of Operation (continued)

Application Examples (continued)

Applications that require more than four segments can be achieved by cascading ATT1S04 SEABREEZE devices. The example in Figure 15 shows a 12-port, eight-segment design. Each SEABREEZE provides the capability for four segments. Figure 16 shows the connection between the ATT1RX04 and the ATT1S04. Only one port is shown for simplicity. Each port from an ATT1RX04 is connected to each SEABREEZE. To assign that port to segment B6, for example, the port must be configured to segment B of SEABREEZE #2 and must be disabled on SEABREEZE #1. The disabled port of SEABREEZE #1 will ignore inputs and will 3-state its outputs so that logically the ATT1RX04 port is only connected to SEABREEZE #2.

LSID[0] is used to distinguish between the SEABREEZE devices so they each generate their own internal chip selects. Note that both address decoders are not fully utilized.



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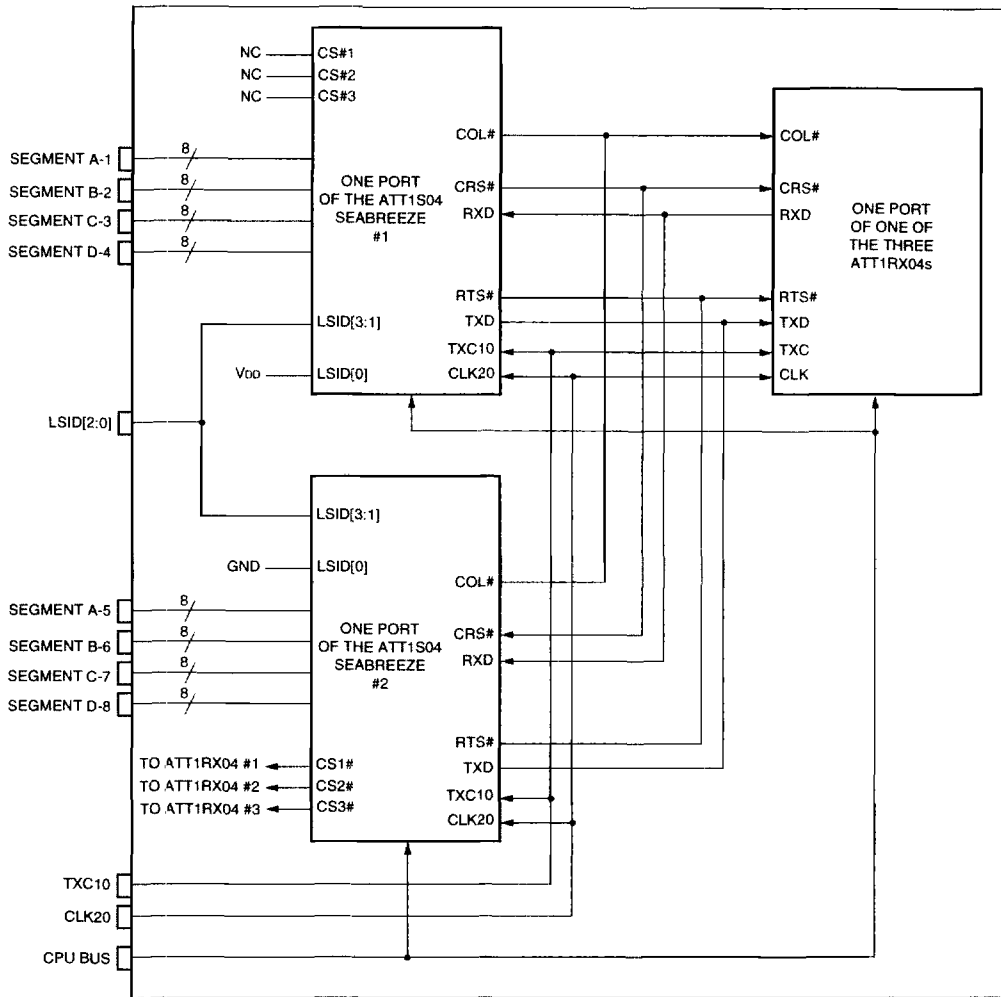
5-37766F

Figure 15. 12-Port, Eight-Segment Card

Principles of Operation (continued)

Application Examples (continued)

SECTION 2.6



5-4061C

Note: Eight cards of 12 ports are possible in this configuration.

Figure 16. Application Example Showing How to Connect Ports of the ATT1RX04 to the ATT1S04 for a 12-Port, Eight-Segment Connection

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause immediate or latent permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature Range	T _A	0	70	°C
Storage Temperature Range	T _{stg}	-40	125	°C
Voltage on Any Pin with Respect to Ground	—	-0.5	V _{DD} + 0.5	V
V _{DD}	—	—	7.0	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Device	Voltage
SEABREEZE	>1000 V

Electrical Characteristics

Ambient temperature 0 °C to 70 °C, V_{DD} = 5.0 V ± 10%, GND = 0.0 V.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage (TTL):					
Low	V _{IL}	—	0	0.8	V
High	V _{IH}	—	2.2	V _{DD}	V
Input Voltage (CMOS):					
Low	V _{IL}	—	0	0.3 V _{DD}	V
High	V _{IH}	—	0.7 V _{DD}	V _{DD}	V
Output Voltage (CMOS)*:					
Low	V _{OL}	I _{OL} = 0 mA	—	0.5	V
High	V _{OH}	I _{OH} = 0 mA	V _{DD} - 0.5	—	V
Input Leakage Current:					
TTL Inputs	I _{ILH} , I _{ILL}	V _{IH} = V _{DD} or GND	—	10	μA
Inputs with Pull-ups	I _{ILHP} , I _{ILLP}	V _{IH} = GND	- 40	-270	μA
Negative Schmitt Trigger Voltage	—	—	0.6	1.8	ns
Power Supply Current	I _{DD5}	0 °C, V _{DD} = 5.5 V	—	170	mA
Power Dissipation†	PD	25 °C, V _{DD} = 5.0 V	—	600	mW
	PD	0 °C, V _{DD} = 5.5 V	—	900	mW

* The following are sink/source values used to achieve the specified Min and Max values:

Group A — (CLK20, TXC10, COLp#, RTSp#, TXDp#, CSc#, RST_OUT) = 8 mA; propagation delays relative to CLK with TXC high is 35 ns maximum.

Group B — (BCOLs#, EVs#, BDs, BID[4:0], D[2:0]) = 9 mA.

† The rise and fall times are 10% and 90% of the signal level.

SECTION 2.6

Timing Characteristics

Clock Signals

TXC10 is used for clocking the transmit and receive data and control signals. The rising edge of TXC10 is coincident (some skew permitted) with the falling edge of CLK20. Figure 17 shows the relationship between the 20 MHz CLK20 and 10 MHz TXC10 clocks. Table 8 lists the frequency tolerance and the duty cycle for the CLK20. The point marked REF (see Figure 18) is shown on the second falling edge of the CLK20. The reason for this is that TXC10 must change on this edge. The maximum skew of TXC10 from the falling edge of CLK20 is 12 ns. The minimum skew allowed is 0 ns. This signal is used to enable CLK20 which toggles data into and out of the ATT1RX04 on the rising edge.

Table 8. Clock Timing (See Figure 17.)

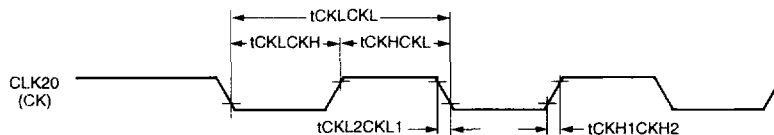
Symbol	Parameter	Min	Typ	Max	Unit
tCKLCKL	Clock Period*	49.995	—	50.005	ns
tCKHCKL	Clock High†	20	—	—	ns
tCKLCKH	Clock Low†	20	—	—	ns
tCKH1CKH2	Clock Rise Time	—	—	5	ns
tCKL2CKL1	Clock Fall Time	—	—	5	ns

* The clock period is referred to as CLK throughout the timing diagrams.

† These timing values are valid subject to the following constraints:

$$tCKHCKH[\min] \leq (tCKHCKL[\min] + tCKLCKH[\max]) \leq tCKHCKH[\max]$$

$$tCKHCKH[\min] \leq (tCKLCKH[\min] + tCKHCKL[\max]) \leq tCKHCKH[\max]$$

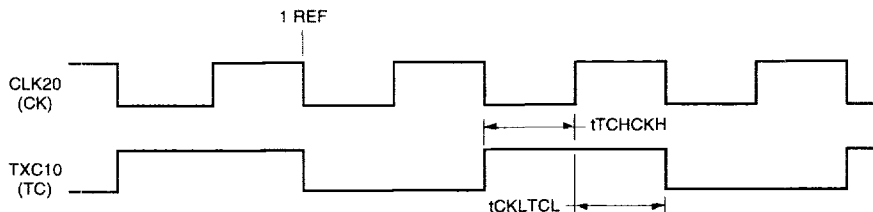


5-2226bC

Figure 17. Clock Timing

Table 9. CLK20 and TXC10 Timing (See Figure 18.)

Symbol	Parameter	Min	Typ	Max	Unit
tTCHTCH	TXC10 Clock Period	99.990	100	100.010	ns
tTCHTCL	TXC10 Clock High	40	50	—	ns
tTCLTCH	TXC10 Clock Low	40	50	—	ns
tTCHCKH	TXC10 High to CLK20 High (setup)	15	—	—	ns
tCKLTCL	CLK20 High to TXC10 Low (hold)	15	—	—	ns
tCKH1CKH2	Clock Rise Time	—	—	5	ns
tCKL2CKL1	Clock Fall Time	—	—	5	ns



5-3392bC

Figure 18. CLK20 and TXC10 Timing

Timing Characteristics (continued)

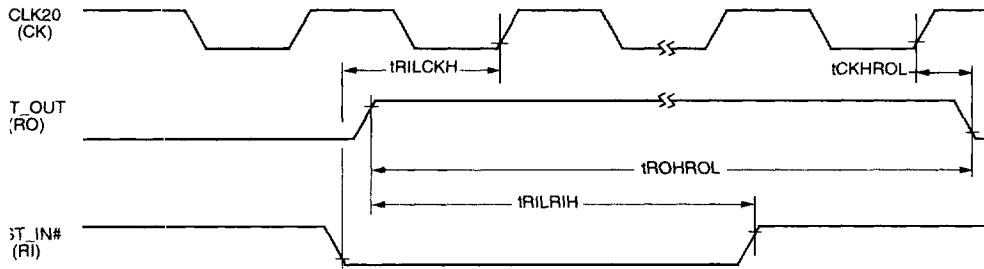
Reset Signals

Table 10. RST_IN# and RST_OUT Timing (See Figure 19.)

Symbol	Parameter	Min	Typ	Max	Unit
tROHROL	RST_OUT Pulse Width	2	—	RST_IN# + 2	μs
tRILRIH*	RST_IN# Pulse Width	500	—	—	ns
tCKHROL†	CLK20 to RST_OUT Deassertion (prop delay)	6	—	20	ns
tRILCKH	RST_IN# to CLK High (setup)	5	—	—	ns

* When RST_IN# is greater than 2 μs, RST_OUT is deasserted relative to RST_IN# deassertion with this same propagation delay.

† When RST_OUT is triggered by a software reset, it is asserted relative to CLK20 with this same propagation delay. Specs for the powerup reset are TBD.



5-4054a.r1

Figure 19. RST_IN# and RST_OUT Timing

SECTION 2.6

Timing Characteristics (continued)

Microprocessor Interface Signals

Table 11. Microprocessor Write Timing (100 pF Loading) (See Figure 20.)

Symbol	Parameter	Min	Typ	Max	Unit
tWHCSH	WE# High to CENB# High (CENB# hold)	10	—	—	ns
tAVWL	Address Valid to WE# Low (ADDR setup)	20	—	—	ns
tWHAX	WE# High to ADDR Invalid (ADDR hold)	20	—	—	ns
tDVWH	Data Valid to WE# High (setup)	10	—	—	ns
tWHDX	WE# High to Data Invalid (hold)	10	—	—	ns
tWLWH	WE# Low and CENB# Low	100	—	—	ns
tWHWL, tWHRL	WE# High to WE# Low or RE# Low	100	—	—	ns

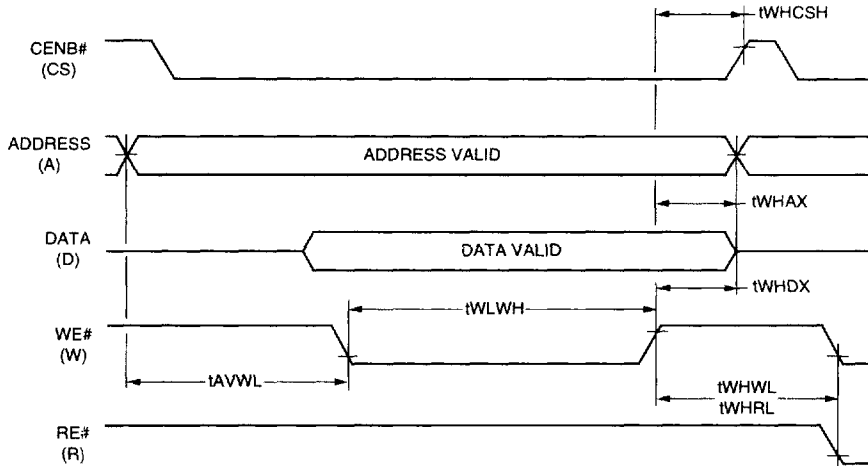


Figure 20. Microprocessor Write Cycle

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5-2233aC

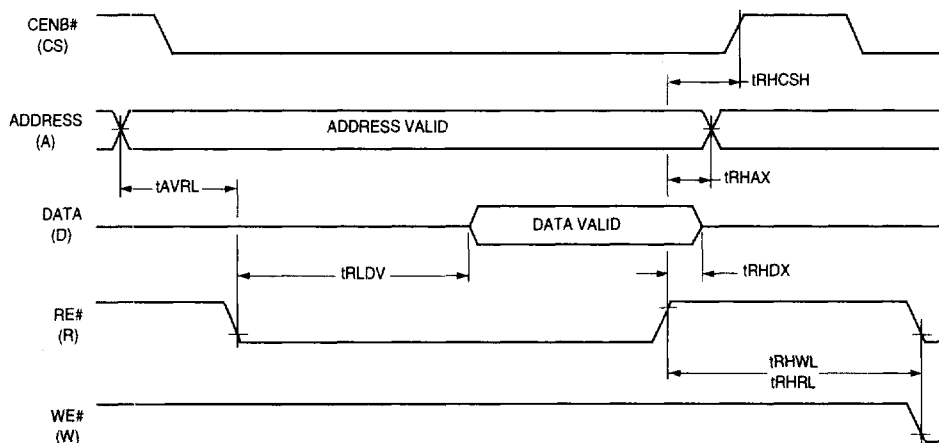
Timing Characteristics (continued)

Microprocessor Interface Signals (continued)

Table 12. Microprocessor Read Timing (See Figure 21.)

Symbol	Parameter	Min	Typ	Max	Unit
tRHCSH	RE# High to CENB# High (CENB# hold)	10	—	—	ns
tAVRL	Address Valid to RE# Low (ADDR setup)	20	—	—	ns
tRHAX	RE# High to ADDR Invalid (ADDR hold)	20	—	—	ns
tRLDV	RE# Low and CENB# Low to Data Valid	50	—	100	ns
tRHDX	RE# High to Data Invalid (data hold)	—	—	30	ns
tRHWL, tRHRL	RE# High to WE# Low or RE# Low	100	—	—	ns

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5-3612aC

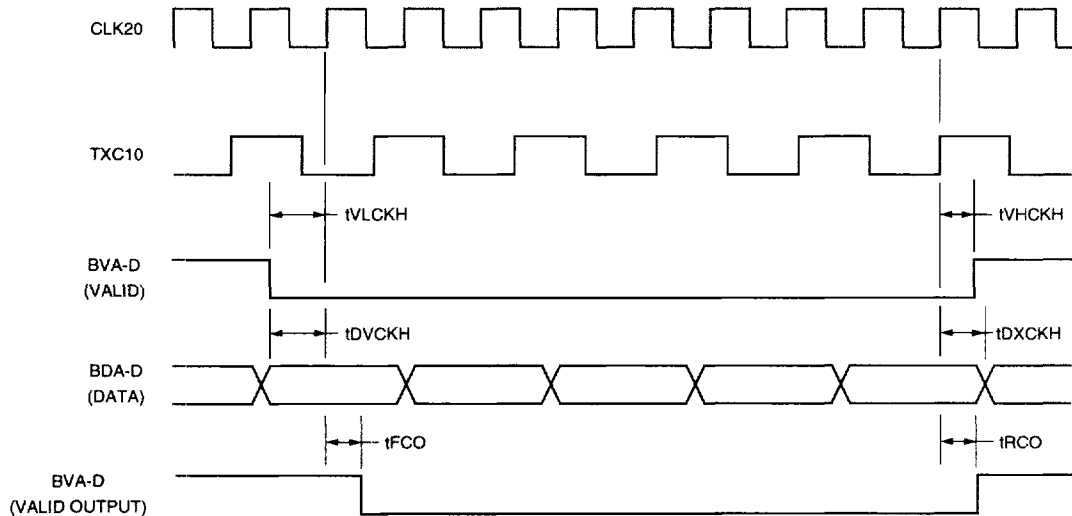
Figure 21. Microprocessor Read Cycle

Timing Characteristics (continued)

Backplane Interface Timing

Table 13. Backplane Interface Timing (See Figure 22.)

Symbol	Input Mode Parameter	Value	Unit
tVLCKH	Backplane Valid to CLK20 High (setup)	3	ns
tVHCKH	Backplane Valid High to CLK20 High (hold)	6	ns
tDVCKH	Backplane Data High to CLK20 High (setup)	3.5	ns
tDXCKH	Backplane Data Invalid to CLK20 High (hold)	6	ns
Input Mode Parameter		min	max
tFCO	CLK20 to Output Falling	12 nS to 7 ns	20 nS
tRCO	CLK20 to Output Rising	10 ns to 8 nS	27 nS



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5-4871.r4

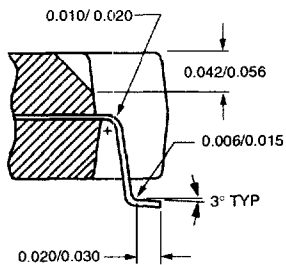
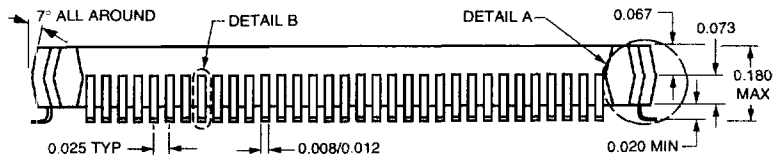
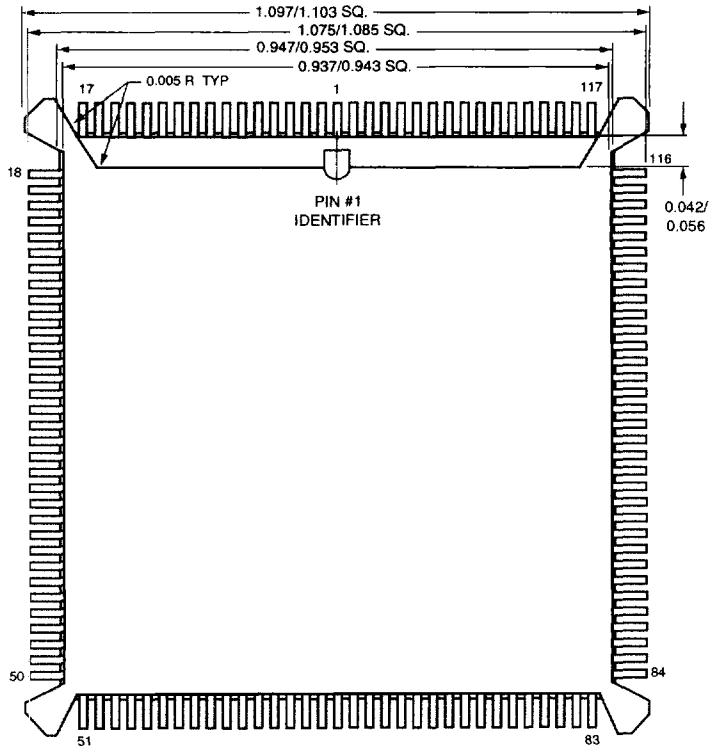
Figure 22. Backplane Interface Timing

The above timing relationships detail the setup and hold time requirements based upon the minimum and maximum system configurations. The maximum tolerable CLK20 clock skew is 2.5 ns. A minimum system configuration is three (3) ATT1S04 devices, 3 pF board capacitance, a 250 Ω pull-up register, and a maximum system configuration is sixteen (16) ATT1S04 devices, 10 pF board capacitance, and a 250 Ω pull-up register.

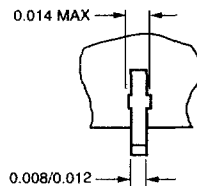
Outline Diagram

132-Pin BQFP Package

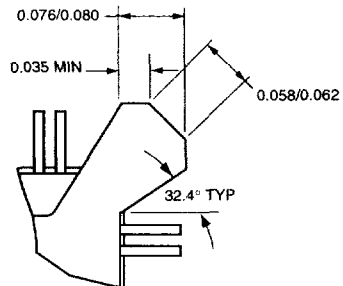
Dimensions are in millimeters.



DETAIL A



DETAIL B



BUMPER DETAIL

SECTION 2.6

Ordering Information

Device Code	Package	Temperature
ATT1S04	132-Pin BQFP	0 °C to 70 °C