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SSI 82C100/101 Programmable Logic Array

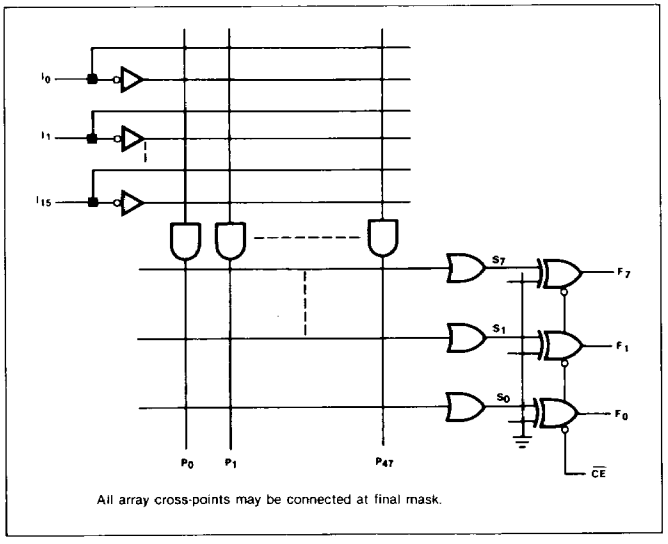
Preliminary Data Sheet

GENERAL DESCRIPTION

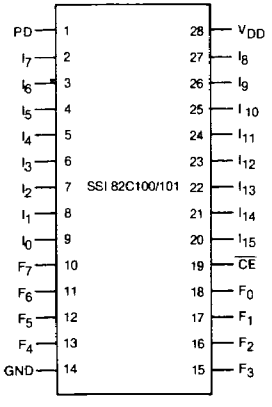
The SSI 82C100/101 are CMOS mask Programmable Logic Arrays (PLA). The AND-OR-Invert architecture gives the user the ability to implement custom sum-of-product logic equations. Sixteen inputs and eight outputs yield a total of 48 available product terms. A product term is the logical AND of up to 16 of the inputs in true or compliment form. As many as all of these product terms can be ORed together to create a desired output function. The output can then be programmed as active high or low. A mask option gives the designer a choice of outputs, either three-state with the SSI 82C100 or active pull down (open-drain) with the SSI 82C101. A chip enable ($\overline{CE}$) pin controls the outputs. The SSI 82C100/101 is fully TTL compatible.

FEATURES

- **Mask programmable**
- **16 input variables**
- **8 output variables**
- **48 product terms**
- **Chip enable ($\overline{CE}$) pin**
- **Three-state outputs**
- **70 nsec Address access time**
- **Functional replacement for Signetics 82S100/101**



LOGIC DIAGRAM



Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

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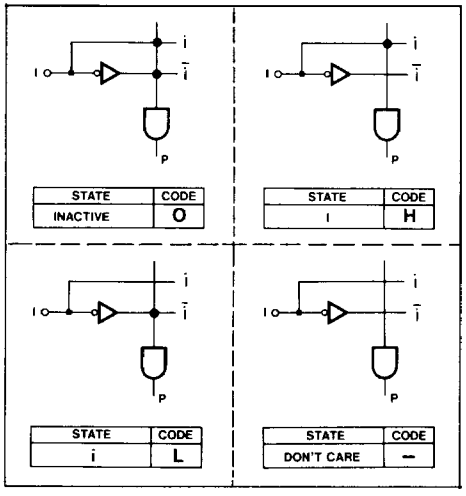
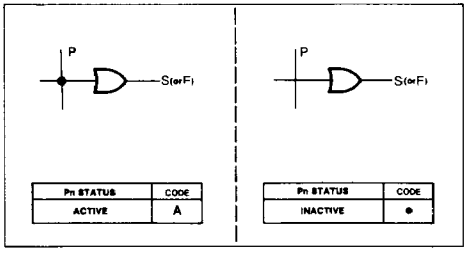
Programming
Either boolean equations, our logic diagram with the connections shown or a completed program table are sufficient for indicating a customer's programming needs. A blank diagram and table are included in this data sheet for the designer's use.

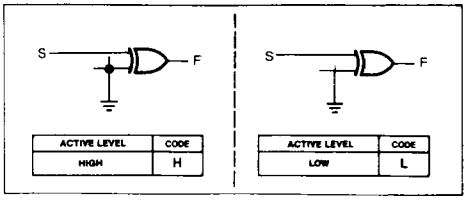
Inputs and the "AND" Array
Each input to the SSI 82C100/101 is available to the AND array in either true or complement form. Either form of these 16 inputs may be connected to any of the AND gates. However if both forms are inputs to any one gate, that gate is inactive regardless of its other inputs. The four ways to program an AND gate are shown below.



"OR" Array
Any of the product terms (output of the AND array) can be connected to any of the OR gates.



Outputs
An output can be programmed active high or low by either grounding or leaving open the unused input of the EXOR gate.



Chip Enable
For the SSI 82C100 a high on the $\overline{CE}$ pin will cause the outputs to go to a high-impedance state. With the SSI 82C101, the $\overline{CE}$ pin going high forces all the outputs high, provided an external pull-up resistor is connected. In either device, a low on the $\overline{CE}$ pin gives the chip control of the outputs.

Power Down Mode
The PD pin on the SSI 82C100/101 is a control for the power down mode. A high on the pin reduces chip power and speed by a factor of 100 but retains the device's logical functions. During normal operation PD can be grounded or left floating.

Absolute Maximum Ratings*

Parameter	Min	Max	Unit
Supply Voltage (V_{CC})	—	+7	Vdc
Input Voltage	−0.3	VCC+0.3	Vdc
Output Voltage	−0.3	VCC+0.3	Vdc
Input Currents	−1	+1	mA
Output Currents	—	+20	mA
Storage Temperature	−65	+150	°C

*Exceeding the absolute maximum ratings may cause permanent damage to the device.

DC Electrical Characteristics (0 °C ≤ Ta ≤ +75 °C, 4.75V ≤ Vcc ≤ 5.25V All voltages are with respect to ground.)

Parameter	Test Conditions	Min.	Max.	Units
Input Voltage High	Vcc = Max	2.0	—	V
Input Voltage Low	Vcc = Min	—	0.85	V
Output Voltage High[1]	IOH = −2mA	2.4	—	V
Ouput Voltage Low[2]	IOL = 9.6mA Vcc = Min	—	0.45	V
Input Current High[3]	Vin = Vcc	—	25	μA
Input Current Low[3]	Vin = 0.45V	−100	—	μA
PD Input Current High	Vin = Vcc	—	100	μA
PD Input Current Low	Vin = 0.45V	−25	—	—
Output Current Hi-Z	$\overline{CE}$ = High, Vcc = Max Vout = Vcc	−40	40	μA
	Vout = 0.45V	−40	40	μA
Output Current Short Circuit[4, 5]	$\overline{CE}$ = Low, Vout = OV Pullup Active	−14	−100	mA
Supply Current[6]	PD Low	—	50	mA
Supply Current	PD High	—	500	μA
Input Capacitance	Vin = 2.0V	—	8	pF
Output Capacitance	Vout = 2.0V $\overline{CE}$ = High, Vcc = 5.0V	—	17	pF

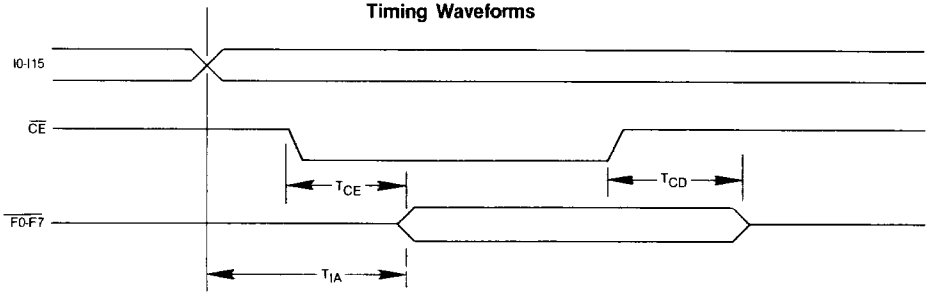
Notes:
1. Measured with $\overline{CE}$ low (chip enabled) and a logic high output.
2. Measured with $\overline{CE}$ low (chip enabled) and a logic low output. Output sink current is applied through a resistor to Vcc.
3. Except PD
4. Only one output should be tested at a time.
5. Do not exceed 1 second with short circuit current.
6. Measure supply current with $\overline{CE}$ low, I0-I15 high, outputs open and PD as specified.

Timing Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Propagation Delay	TIA	See Fig 1	—	50	ns
Chip Enable Delay[7]	TCE	See Fig 2	—	30	ns
Chip Disable Delay[8]	TCD	See Fig 3	—	30	ns

Notes: 7. TCE is the delay from $\overline{CE}$ low to data valid.
8. TCD is the delay from $\overline{CE}$ high to high-Z or high output state. The chip disable state is reached when the output moves 0.5V from its initial value.

Timing Waveforms



Note: Input rise and fall times (10%-90%) are less than 5 ns.

Test Circuits for Timing Measurements

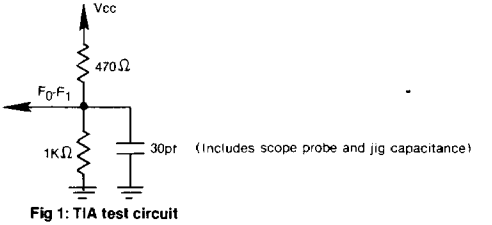


Fig 1: TIA test circuit

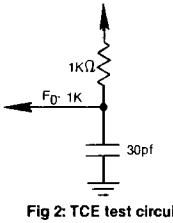


Fig 2: TCE test circuit

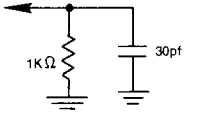


Fig 3: TCD test circuit

Example

This example illustrates all three means of providing programming data to SSI. Any one of the three is sufficient. The diagram below and the table on the next page indicate the programming necessary to implement these equations:

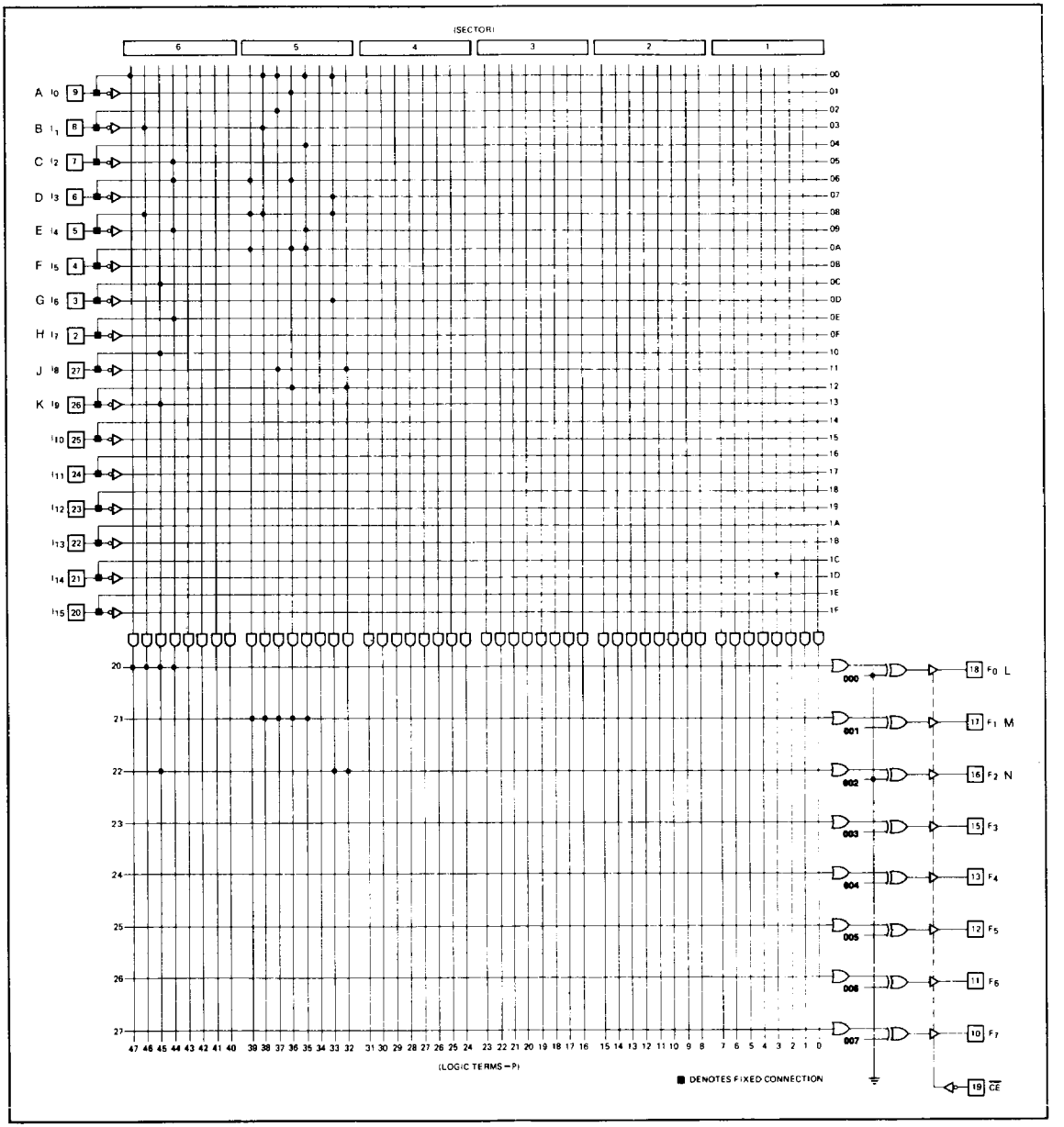
Boolean Equations

$L = A + \bar{B}E + GJ\bar{K} + \bar{C}D\bar{E}H$

$\bar{M} = DEF + A\bar{B}E + AB\bar{J} + \bar{A}DFK + AC\bar{E}F$

$N = GJ\bar{K} + A\bar{D}E\bar{G} + \bar{J}K$

PLA Logic Diagram



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PLA Logic Program Table