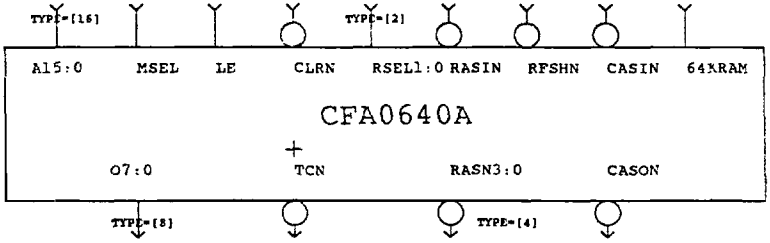
CFA0640A DRAM Controller

DESCRIPTION: CFA0640A is fully compatible with the AM2964 bit-slice dynamic RAM controller. One extra input, 64KRAM, is added to select the 64K or 16K dynamic memory. To use 16K RAMs, CFA0640A requires that 64KRAM be tied to low, while AM2964 requires that the A15 input be pulled up to +12V through a 1K resistor. When RFSHN is not active, MSEL selects output address O7:0 from A15:8 or A7:0. The RSEL1:0 inputs select one of the four RASN3:0 outputs to go low when RASIN goes low, and the CASON output follows CASIN. When RFSHN is active, the O7:0 outputs become the inverted refresh counter outputs, and all RASN3:0 outputs go active with RASIN to refresh all memory banks. CASON is disabled and is always high. The refresh counter can be cleared at any time by resetting CLRN, which advances the refresh counter at the low-to-high transition of either RASIN or RFSHN when the other is low. TCN goes low when the refresh counter has been sequenced through either the 256 or the 128 addresses, depending on the 64KRAM input. For detailed description, see the AM2964 data sheet.

LOGIC SYMBOL:



INPUTS (LOADING IN TRANSISTOR PAIRS):
A15:0(3.4), MSEL(2), LE(18), CLRN(16), RSEL1:0(3.4), RASIN(2), RFSHN(9), CASIN(1), 64KRAM(2)

OUTPUTS (DRIVE IN (#P,#N)):
O7:0(1,0.5), TCN(2,2), RASN3:0(1,0.5), CASON(1,0.5)

GATE COUNT: GATES USED = 276
AREA USED = 325

CFA0640A

PIN DESCRIPTION:

INPUTS:	A15:0	ADDRESS INPUTS WITH A15 THE MSB
	MSEL	MUX-SELECT INPUT TO SELECT LOWER ORDER ADDRESS (WHEN HIGH) OR HIGHER ORDER ADDRESS (WHEN LOW)
	LE	ADDRESS LATCH ENABLE
	CLRN	REFRESH COUNTER CLEAR ACTIVE LOW INPUT
	RSEL1:0	RASN(I) DECODER SELECT INPUT
	RASIN	ROW ADDRESS STROBE INPUT
	RFSHN	REFSH ACTIVE LOW CONTROL INPUT
	CASIN	COLUMN ADDRESS STROBE INPUT
	64KRAM	SELECT 64K RAM (WHEN HIGH) OR 16K RAM (WHEN LOW)
OUTPUTS:	O7:0	RAM ADDRESS OUTPUT
	TCN	TERMINAL COUNT OUTPUT
	RASN3:0	ROW ADDRESS STROBE OUTPUTS
	CASON	COLUMN ADDRESS STROBE OUTPUT

SWITCHING CHARACTERISTICS:

	PARAMETER	DESCRIPTION	DELAY*	NOTE
1.	TPD	A(I) TO O(I)	5 NS	
2.	TPHL	RASIN TO RASN(I)	2.2 NS	RFSHN=H
3.	TPHL	RASIN TO RASN(I)	2.2 NS	RFSHN=L
4.	TPD	MSEL TO O(I)	4.3 NS	MIN
5.	TPD	MSEL TO O(I)	5.7 NS	MAX
6.	TPHL	CASIN TO CASON	2 NS	RFSHN=H
7.	TPHL	RSEL(I) TO RASN(I)	5.3 NS	LE=H,RASIN=L
8.	TPLH	RFSHN TO TCN	11 NS	RASIN=L
9.	TPLH	RASIN TO TCN	10.7 NS	RFSHN=L
10.	TCYCLE	RASIN	11.9 NS	
11.	TPD	RFSHN TO O(I)	4.8 NS	
12.	TPHL	RFSHN TO RASN(I)	2.5 NS	RASIN=L
13.	TPW	CLRN=L	1.7 NS	
14.	TPLH	RFSHN TO CASON	1.3 NS	
15.	TPD	LE TO O(I)	5 NS	
16.	TPHL	LE TO RASN(I)	5.3 NS	
17.	TPLH	CLRN TO TCN	7.1 NS	
18.	TPLH	CLRN TO O(I)	5.9 NS	RFSHN=L
19.	TS	A(I) TO LE SETUP TIME	0.6 NS	
20.	TH	A(I) TO LE HOLD TIME	0.8 NS	
21.	TS	RSEL(I) TO LE SETUP TIME	0.6 NS	
22.	TH	RSEL(I) TO LE HOLD TIME	0.8 NS	
23.	TS	CLRN RECOVERY TIME	0 NS	
24.	TSKEW	O(I) TO RASN(I)	3 NS	RFSHN=H
25.	TSKEW	O(I) TO CASON	3.9 NS	
26.	TSKEW	O(I) TO RASN(I)	2.9 NS	RFSHN=L
27.	TSKEW	O(I) TO RASN(I)	0 NS	MSEL=H->L
28.	TPD	64RAM TO TCN	3.6 NS	
29.	TPD	64RAM TO O(I)	3.3 NS	LE=H

* ALL TIMINGS ARE BASED ON 10K NOMINAL CONDITIONS WITH 2 OUTPUT LOADINGS.