

# UT54ACS273/UT54ACTS273

## Radiation-Hardened Octal D-Flip-Flops with Clear

### FEATURES

- Contains eight flip-flops with single-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers, shift registers, and pattern generators
- 1.2μ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 20-pin DIP
  - 20-lead flatpack

### DESCRIPTION

The UT54ACS273 and the UT54ACTS273 are positive-edge-triggered D-type flip-flops with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

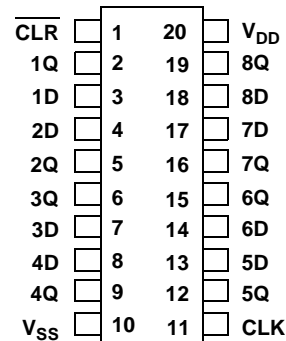
The devices are characterized over full military temperature range of -55°C to +125°C.

### FUNCTION TABLE

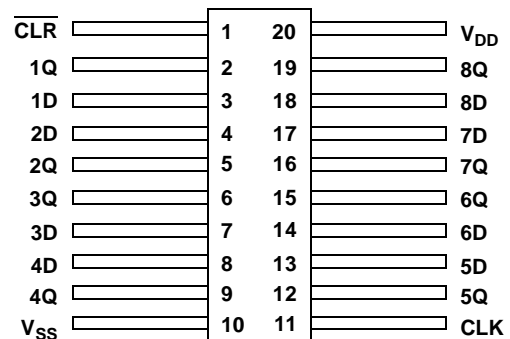
INPUTS			OUTPUTS
$\overline{\text{CLR}}$	CLK	D <sub>x</sub>	Q <sub>x</sub>
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No change

### PINOUTS

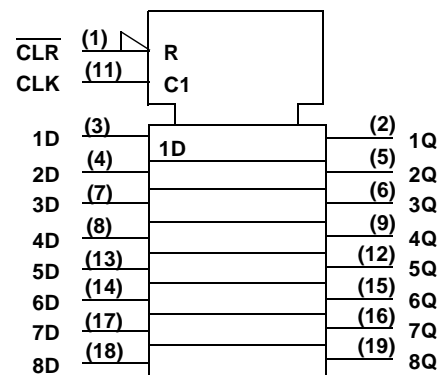
#### 20-Pin DIP Top View



#### 20-Lead Flatpack Top View



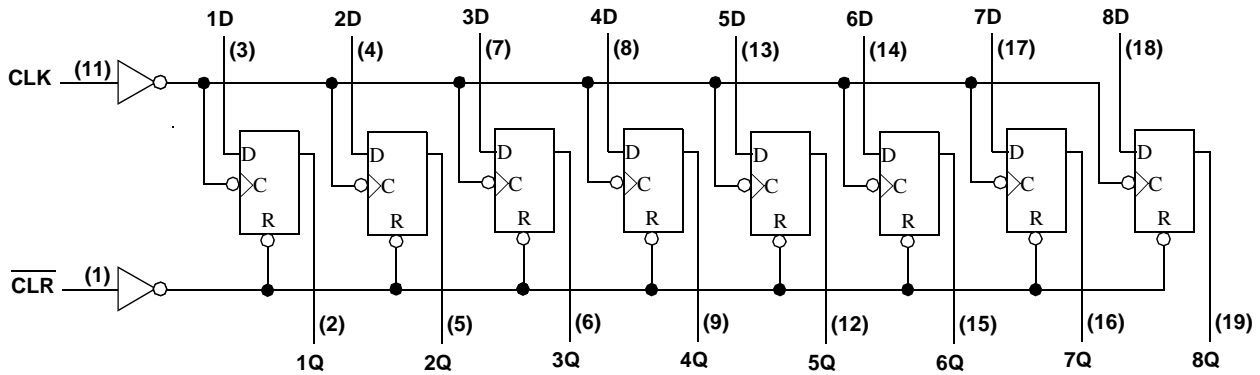
### LOGIC SYMBOL



#### Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

**LOGIC DIAGRAM**



**RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>**

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
SEL Threshold	120	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-.3 to V <sub>DD</sub> +.3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>LIMIT</b>	<b>UNITS</b>
$V_{DD}$	Supply voltage	4.5 to 5.5	V
$V_{IN}$	Input voltage any pin	0 to $V_{DD}$	V
$T_C$	Temperature range	-55 to + 125	°C

**DC ELECTRICAL CHARACTERISTICS <sup>7</sup>**(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V <sup>6</sup>, -55°C < T<sub>C</sub> < +125 °C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V <sub>IL</sub>	Low-level input voltage <sup>1</sup> ACTS ACS			0.8 .3V <sub>DD</sub>	V
V <sub>IH</sub>	High-level input voltage <sup>1</sup> ACTS ACS		.5V <sub>DD</sub> .7V <sub>DD</sub>		V
I <sub>IN</sub>	Input leakage current ACTS/ACS	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	1	μA
V <sub>OL</sub>	Low-level output voltage <sup>3</sup> ACTS ACS	I <sub>OL</sub> = 8.0mA I <sub>OL</sub> = 100μA		0.40 0.25	V
V <sub>OH</sub>	High-level output voltage <sup>3</sup> ACTS ACS	I <sub>OH</sub> = -8.0mA I <sub>OH</sub> = -100μA	.7V <sub>DD</sub> V <sub>DD</sub> - 0.25		V
I <sub>OS</sub>	Short-circuit output current <sup>2,4</sup> ACTS/ACS	V <sub>O</sub> = V <sub>DD</sub> and V <sub>SS</sub>	-200	200	mA
I <sub>OL</sub>	Output current <sup>10</sup> (Sink)	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> V <sub>OL</sub> = 0.4V	8		mA
I <sub>OH</sub>	Output current <sup>10</sup> (Source)	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> V <sub>OH</sub> = V <sub>DD</sub> - 0.4V	-8		mA
P <sub>total</sub>	Power dissipation <sup>2,8,9</sup>	C <sub>L</sub> = 50pF		1.9	mW/ MHz
I <sub>DDQ</sub>	Quiescent Supply Current	V <sub>DD</sub> = 5.5V		10	μA
ΔI <sub>DDQ</sub>	Quiescent Supply Current Delta ACTS	For input under test V <sub>IN</sub> = V <sub>DD</sub> - 2.1V For all other inputs V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> V <sub>DD</sub> = 5.5V		1.6	mA
C <sub>IN</sub>	Input capacitance <sup>5</sup>	f = 1MHz @ 0V		15	pF
C <sub>OUT</sub>	Output capacitance <sup>5</sup>	f = 1MHz @ 0V		15	pF

## UT54ACS273/UT54ACTS273

### Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

**AC ELECTRICAL CHARACTERISTICS <sup>2</sup>**(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V <sup>1</sup>, -55°C < T<sub>C</sub> < +125 °C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t <sub>PLH</sub>	CLK to Q	4	17	ns
t <sub>PHL</sub>	CLK to Q	4	19	ns
t <sub>PHL</sub>	$\overline{\text{CLR}}$ to Q	5	19	ns
f <sub>MAX</sub>	Maximum clock frequency		63	MHz
t <sub>SU1</sub>	$\overline{\text{CLR}}$ inactive setup time before CLK ↑	5		ns
t <sub>SU2</sub>	Data setup time before CLK ↑	5		ns
t <sub>H</sub>	Data hold time after CLK ↑	3		ns
t <sub>w</sub>	Minimum pulse width $\overline{\text{CLR}}$ low CLK high CLK low	8		ns

**Notes:**

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).