

SONY.

CXB1143Q/Q-Y

Quad 4 : 1 Multiplexer with D-FF

T-68-11-51

Description

The CXB1143Q is an ultra high speed monolithic ECL IC, which contains four 4 : 1 multiplexers followed by D type flip flops. The data select (S₀, S₁) inputs determine which data is enabled. The selected data is transferred to the flip flops output by the positive transition of clock (C) input. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

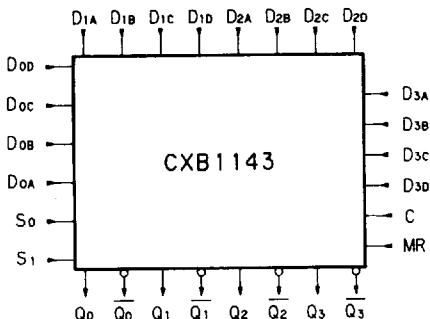
Features

- Typical clock rate up to 2.6 GHz
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

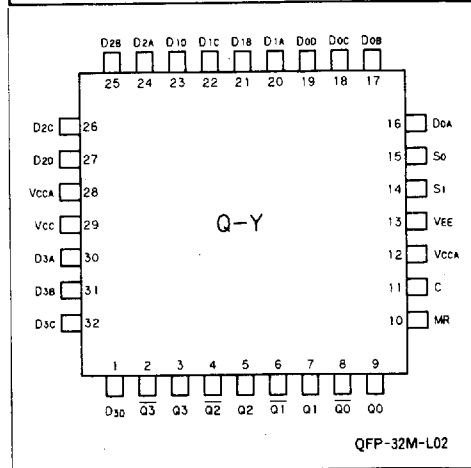
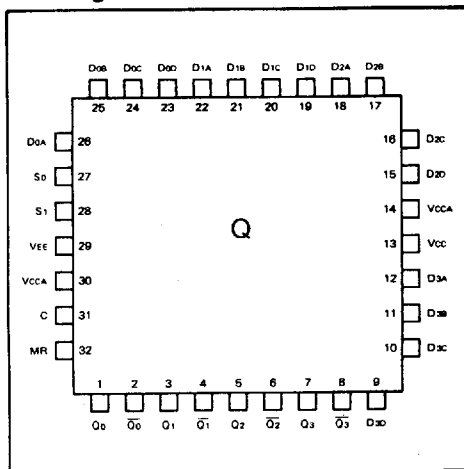
Pin Names

- D_{nA}–D_{nD} Data inputs
- Q_n, Q_n Data outputs
- S_n Data select inputs
- C Clock input
- MR Direct Master Reset input
- V_{cc} Circuit ground
- V_{CCA} Circuit ground for outputs
- V_{EE} Negative power supply

Logic Symbol



Pin Assignment



Truth Table

Select inputs		Outputs
S ₀	S ₁	Q _n
L	L	D _{nA}
H	L	D _{nB}
L	H	D _{nC}
H	H	D _{nD}

Note : H ; HIGH voltage Level
L ; LOW voltage Level

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CXB1143Q/QY

DC Characteristics

T-68-11-51

 $V_{EE} = -4.5V \pm 0.3V$, $V_{CC} = V_{CCA} = GND$, $V_{TT} = -2.0V$, $T_c = 0^\circ C$ to $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I _{EE}		-177	-130	-90	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

 $V_{EE} = -4.5V \pm 0.3V$, $V_{CC} = V_{CCA} = GND$, $V_{TT} = -2.0V$, $T_c = 0^\circ C$ to $+85^\circ C$, $R_T = 50\Omega$ to V_{TT}

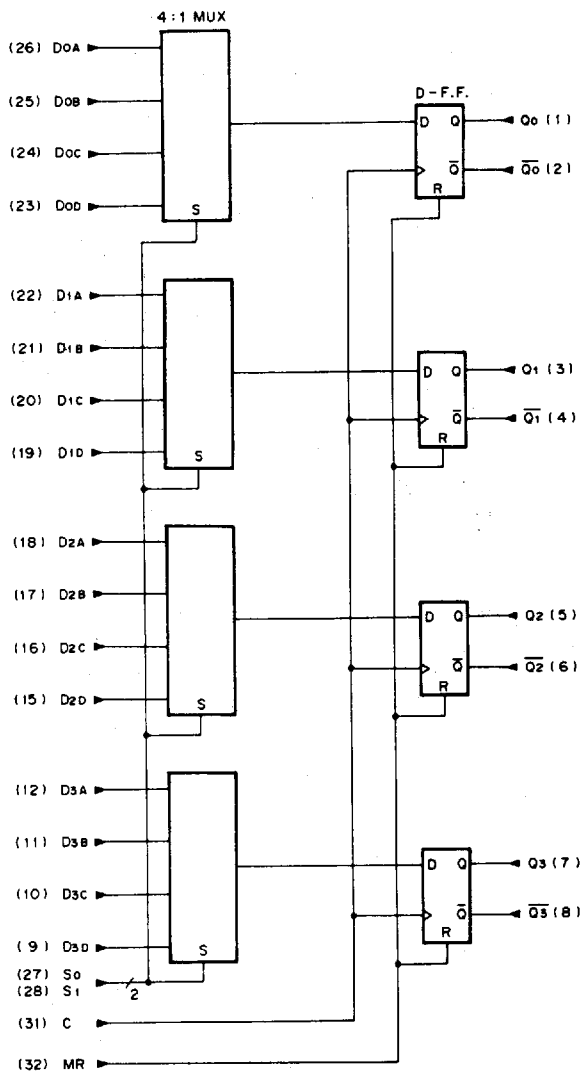
Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit		
Propagation delay time	T _{PLH}	C	Q _n		630	840	1090	ps		
	T _{PHL}				660	880	1150			
	T _{PLH}	MR			770	1030	1340			
	T _{PHL}				780	1050	1370			
Gate-to-Gate skew	T _{SG-G}	C					30		80	
Set up time	T _S	D, C				200				
		SEL, C				450				
Hold time	T _H	C, D				50				
		C, SEL				-200				
Release time	T _R	MR, C				260				
Min. Pulse width	T _{PW}	MR		390						
Max. Clock frequency	f _{MAX}			2.0	2.6		GHz			
Rise time	T _{TLH}	C			250	330				
Fall time	T _{THL}		20% to 80%		200	260	ps			

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

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T-68-11-51

Block Diagram



Package Data

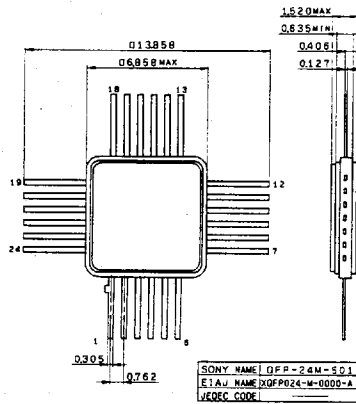
T-90-20

Package Outline

Unit: mm

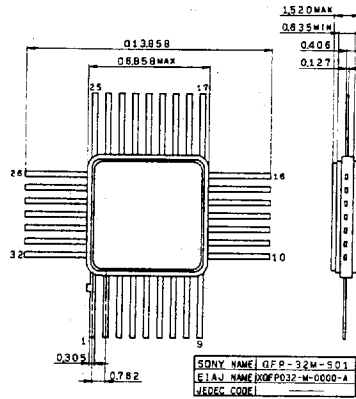
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



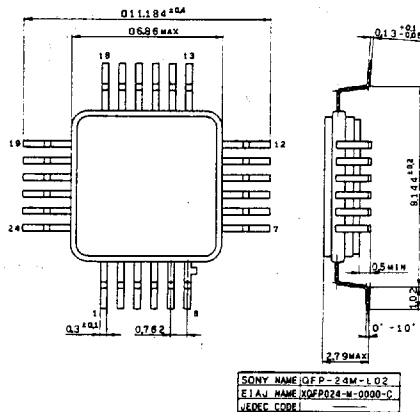
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



24pin QFP (QFP-24M-L02)

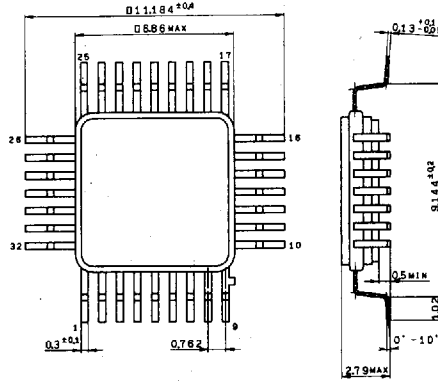
24pin QFP (Metal) 0.3g



T-90-20

32pin QFP (QFP-32M-L02)

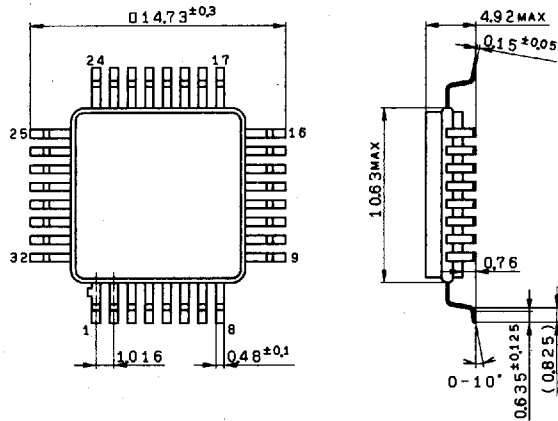
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	

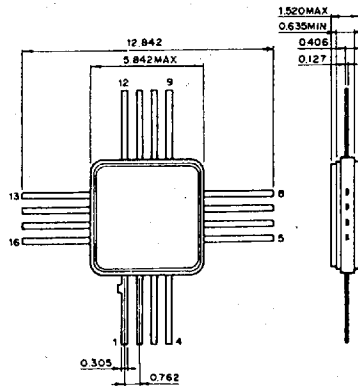
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	

16pin QFP



Package Data

Package Data	Page
1. 16 pin QFP	6-3
2. 24 pin QFP	6-3
3. 32 pin QFP	6-3
4. 24 pin QFP with formed lead	6-4
5. 32 pin QFP with formed lead	6-4

Package Data

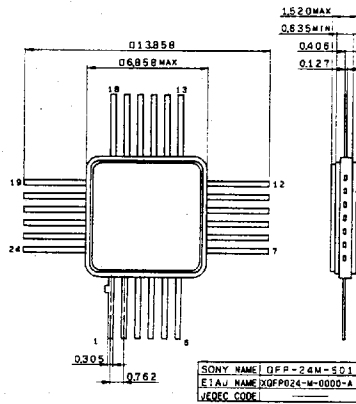
T-90-20

Package Outline

Unit: mm

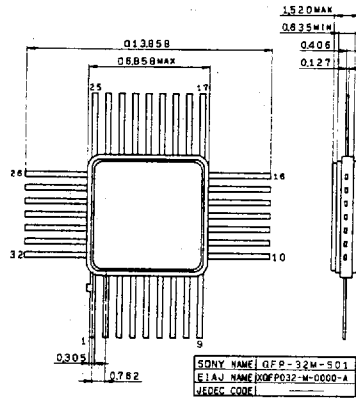
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



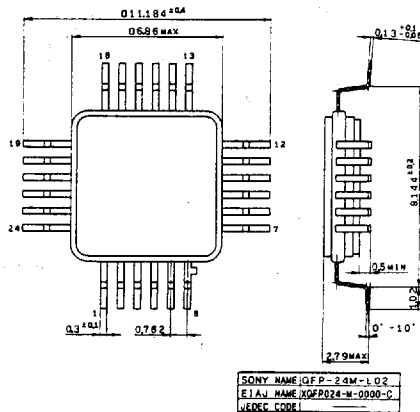
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32pin QFP (Metal) 0.2g



24pin QFP (QFP-24M-L02)

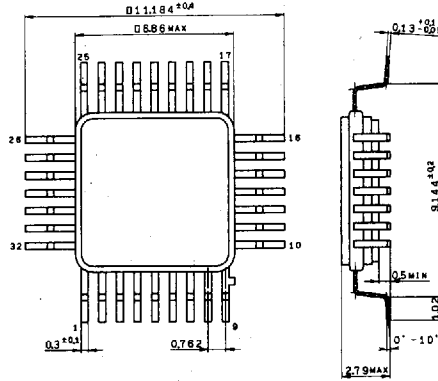
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T-90-20

32pin QFP (QFP-32M-L02)

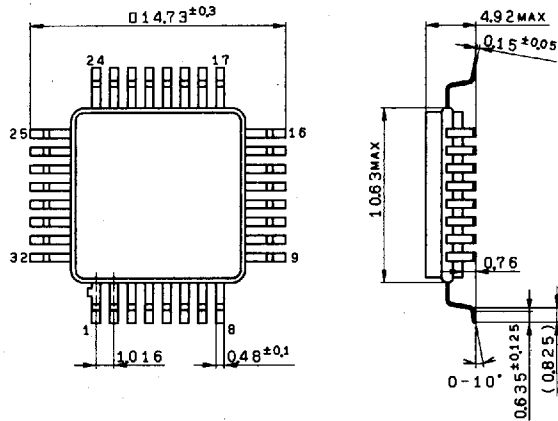
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	

16pin QFP

