MSM511002B

1,048,576-Word × 1-Bit DYNAMIC RAM: STATIC COLUMN MODE TYPE

DESCRIPTION

The MSM511002B is a new generation dynamic RAM organized as 1,048,576-word × 1-bit. The technology used to fabricate the MSM511002B is OKI's CMOS silicon gate process technology. The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

FEATURES

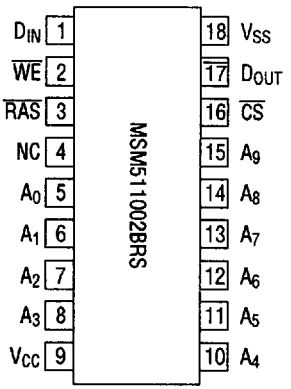
- Silicon gate, quardruple polysilscon COMS, 1-transistor memory cell
- 1,048,576-word × 1-bit organization
- Signal 5V power supply, ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 512 cycles/8ms
- Common I/O capability using Early Write operation
- Static column mode, read modify write capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$-only refresh capability
- Package:

18-Pin 300mil	Plastic DIP	(DIP18-P-300-W1)
26-Pin 300mil	Plastic SOJ	(SOJ26-P-300)
20-Pin 400mil	Plastic ZIP	(ZIP20-P-400)

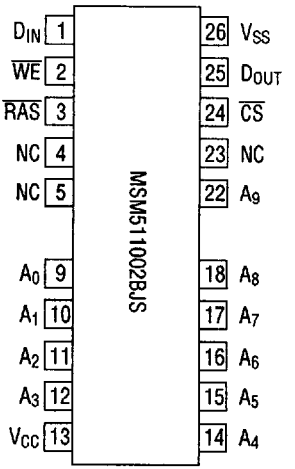
PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (Max.)	Standby (Max.)
MSM511002B-60	60ns	30ns	15ns	120ns	495mW	5.5mW
MSM511002B-70	70ns	35ns	20ns	130ns	440mW	
MSM511002B-80	80ns	40ns	20ns	150ns	385mW	
MSM511002B-10	100ns	50ns	25ns	190ns	330mW	

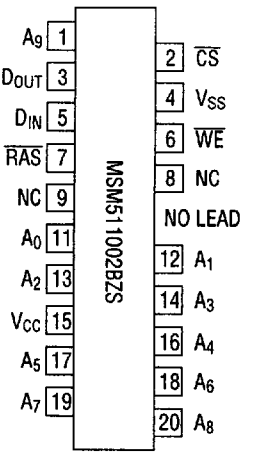
PIN CONFIGURATION (TOP VIEW)



18-PIN DIP



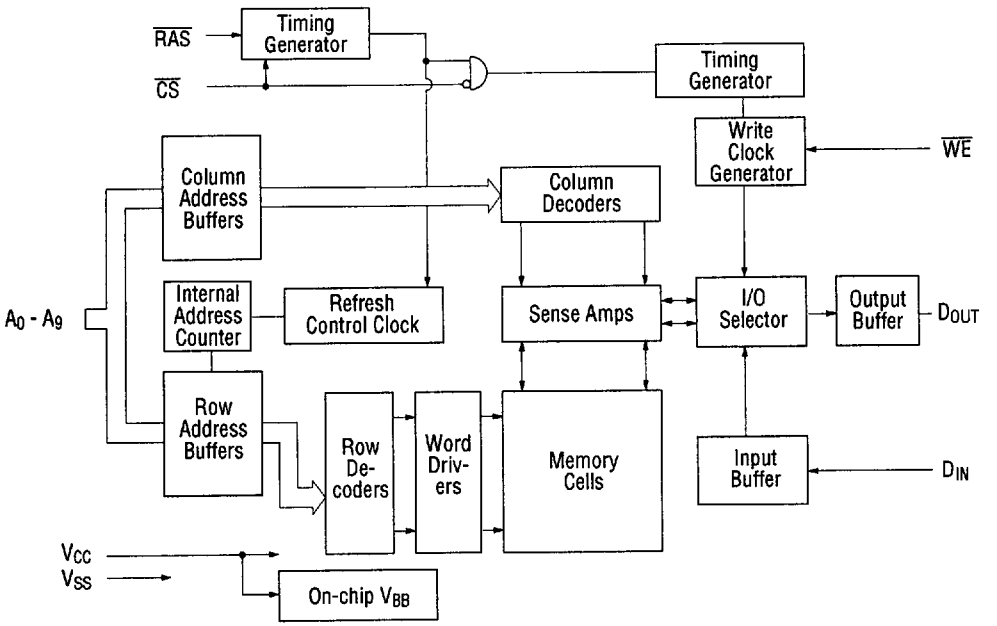
26-PIN SOJ



20-PIN ZIP

Pin Name	Function
A_0 - A_9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, D_{IN})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	C_{IN2}	—	7	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	7	pF

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = 5.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ 6.5V; All other pins not under test = 0V	−10	10	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0V ≤ V_O ≤ 5.5V	−10	10	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling t_{RC} = Min.	—	90	—	80	—	70	—	60	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CS}$ = V_{IH}	—	2	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CS}$ = V_{CC} −0.2V	—	1	—	1	—	1	—	1	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH} t_{RC} = Min.	—	90	—	80	—	70	—	60	mA	1, 2
Average Power Supply Current ($\overline{CS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$ refresh	—	90	—	80	—	70	—	60	mA	1
Average Power Supply Current (Static Column Mode)	I_{CC9}	$\overline{RAS}$ = V_{IL} $\overline{CS}$ cycling, t_{SC} = Min.	—	80	—	70	—	60	—	55	mA	1

Notes: 1. Specified values are obtained with the output open.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}

AC Characteristics (1/3)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	150	—	190	—	ns	
Read Modify Write Cycle Time	t_{RMW}	140	—	155	—	175	—	220	—	ns	
Static Column Mode Cycle Time	t_{SC}	40	—	45	—	50	—	55	—	ns	
Static Column Mode Read Modify Write Cycle Time	t_{SRMW}	65	—	70	—	80	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{CS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	—	40	—	50	ns	4, 6, 7
Access Time from Last Write	t_{ALW}	—	60	—	65	—	75	—	95	ns	4, 7
Output Low Impedance Time from $\overline{CS}$	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Data Output Hold Time Reference to Column Address	t_{AOH}	5	—	5	—	5	—	5	—	ns	
Data Output Enable Time Reference to $\overline{WE}$	t_{OW}	—	25	—	30	—	30	—	30	ns	
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	
Transition Time	t_T	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ Precharge	t_{RP}	50	—	50	—	60	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode Cycle Only)	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CS}$ Precharge Time (Static Column Mode)	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ Pulse Width	t_{CS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode Cycle Only)	t_{CSC}	15	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	50	ns	6
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	

AC Characteristics (2/3)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	10	—	ms	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	50	—	ns	
Column Address Hold Time Reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	50	—	55	—	60	—	75	—	ns	
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	75	—	85	—	95	—	115	—	ns	
Column Address Hold Time Reference to $\overline{RAS}$ Precharge	t_{AH}	10	—	10	—	10	—	10	—	ns	
Column Address Hold Time Reference to $\overline{WE}$	t_{AHLW}	60	—	65	—	75	—	95	—	ns	
Last Write to Column Address Delay	t_{LWAD}	20	30	20	30	20	35	25	45	ns	7
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Reference to $\overline{CS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	50	—	55	—	60	—	75	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	8
Write Command Pulse Width	t_{WP}	10	—	15	—	15	—	20	—	ns	
Write Invalid Time	t_{WI}	10	—	10	—	10	—	10	—	ns	
Write Command Hold Time (D_{OUT} Disable)	t_{WCH}	10	—	15	—	15	—	20	—	ns	8
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	60	—	75	—	ns	
Data Output Hold Time Reference to $\overline{WE}$	t_{WOH}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay	t_{CWD}	15	—	20	—	20	—	25	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	60	—	70	—	80	—	100	—	ns	8
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	50	—	ns	8
$\overline{RAS}$ to Second $\overline{WE}$ Delay	t_{RSWD}	75	—	85	—	95	—	115	—	ns	

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AC Characteristics (3/3)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	9
$\overline{RAS}$ to $\overline{CS}$ Set-up Time ($\overline{CS}$ Before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$)	t_{CHR}	30	—	30	—	30	—	30	—	ns	
$\overline{CS}$ Active Delay from $\overline{RAS}$ Precharge	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	40	—	40	—	40	—	50	—	ns	
$\overline{CS}$ Precharge Time	t_{CPN}	10	—	10	—	10	—	15	—	ns	

Notes:

1. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$-only) before proper device operation is achieved.

2. The AC characteristics assume $t_T = 5ns$.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels of input signals for timing measurement. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD} (Max.) limit insures that t_{RCC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled exclusively by t_{AA}.

7. Operation within the t_{LWAD} (Max.) limit insures that t_{ALW} (Max.) can be met. t_{LWAD} (Max.) is specified as a reference point only; if tLWAD is greater than the specified t_{LWAD} (Max.) limit, access time is controlled exclusively by t_{AA}.

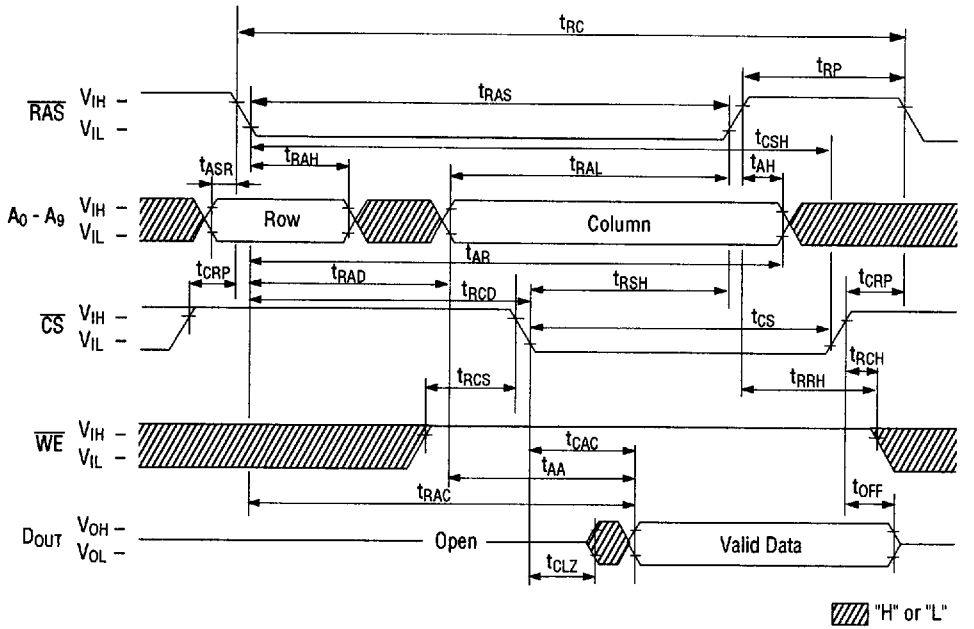
8. t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (Min.) and $t_{WH} \geq t_{WH}$ (Min.), the cycle is an Early Write cycle and the data out pin remains open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read modify write cycle and the data out contains data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

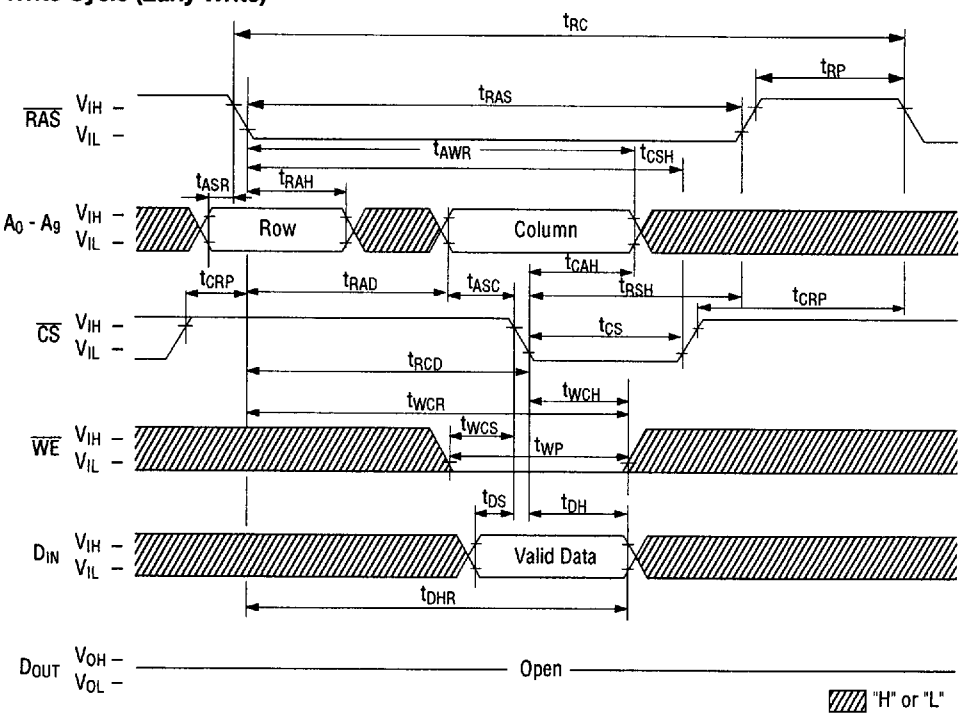
10. These parameters are referenced to $\overline{CS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a read modify write cycle.

TIMING WAVEFORM

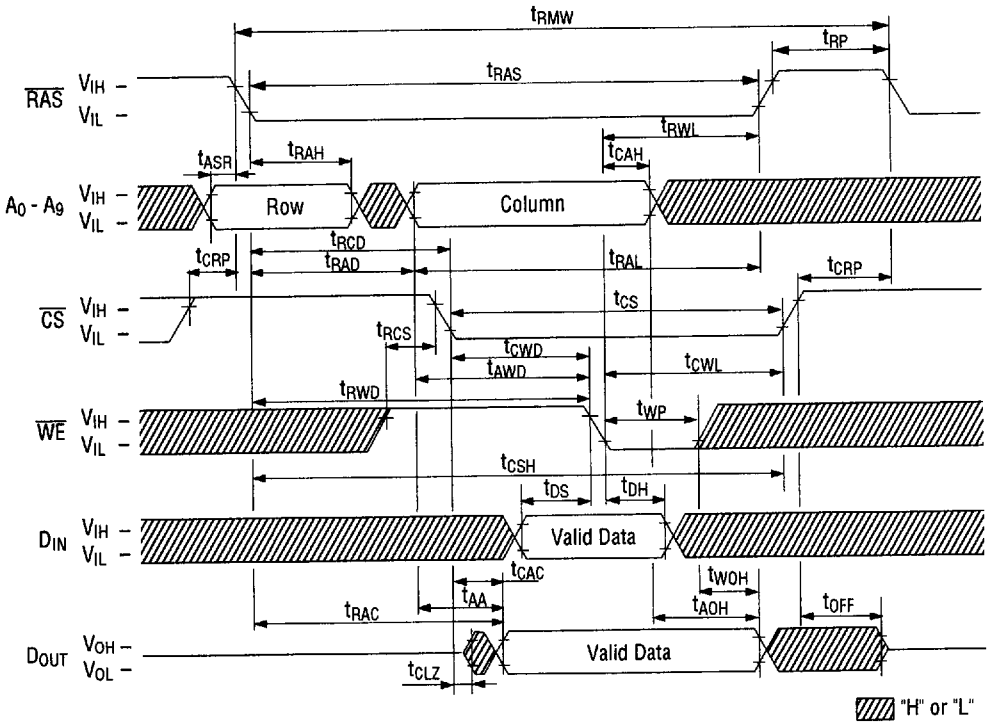
Read Cycle



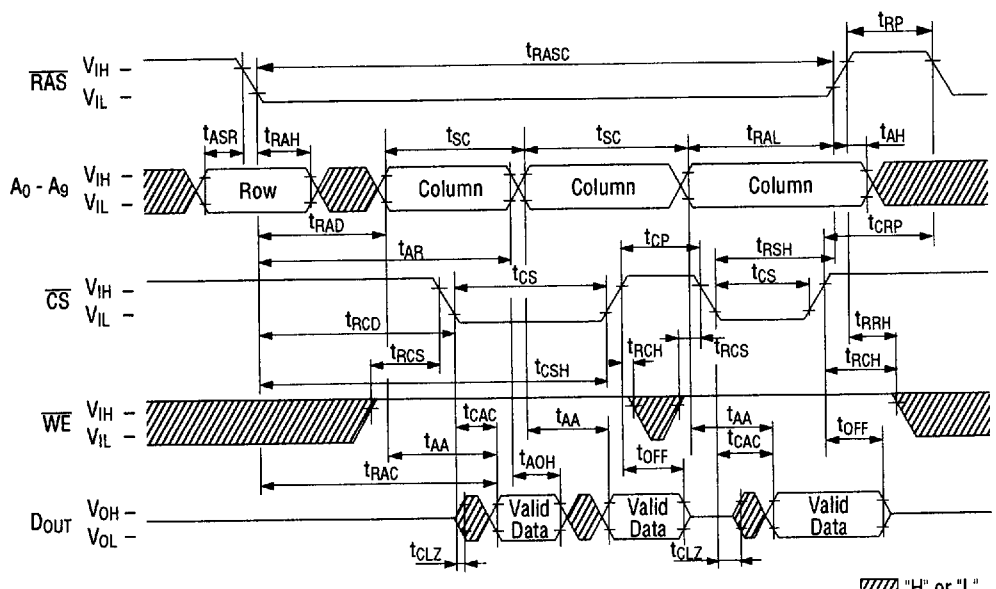
Write Cycle (Early Write)



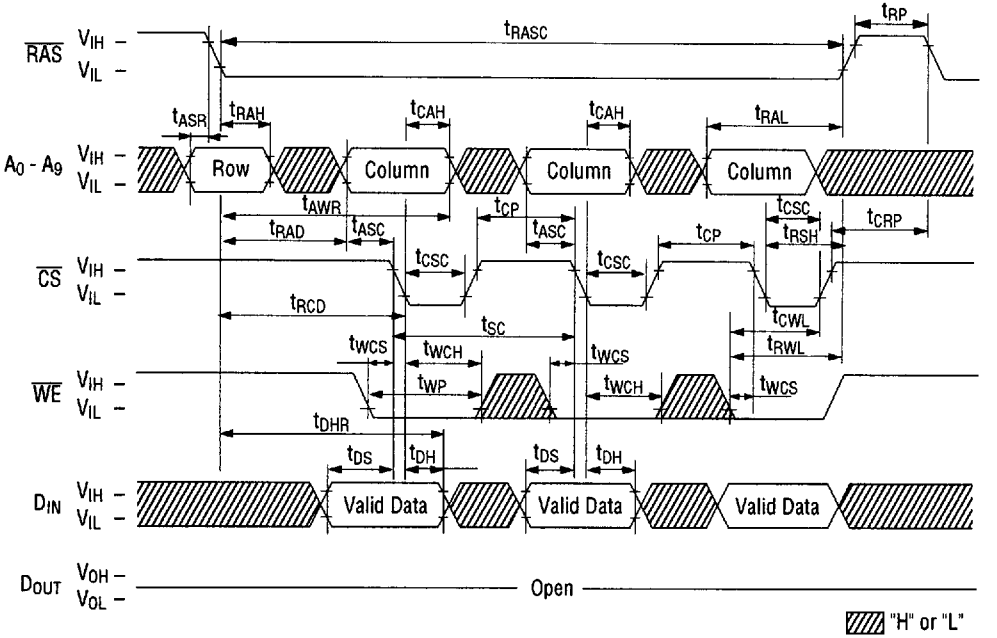
Read Modify Write Cycle



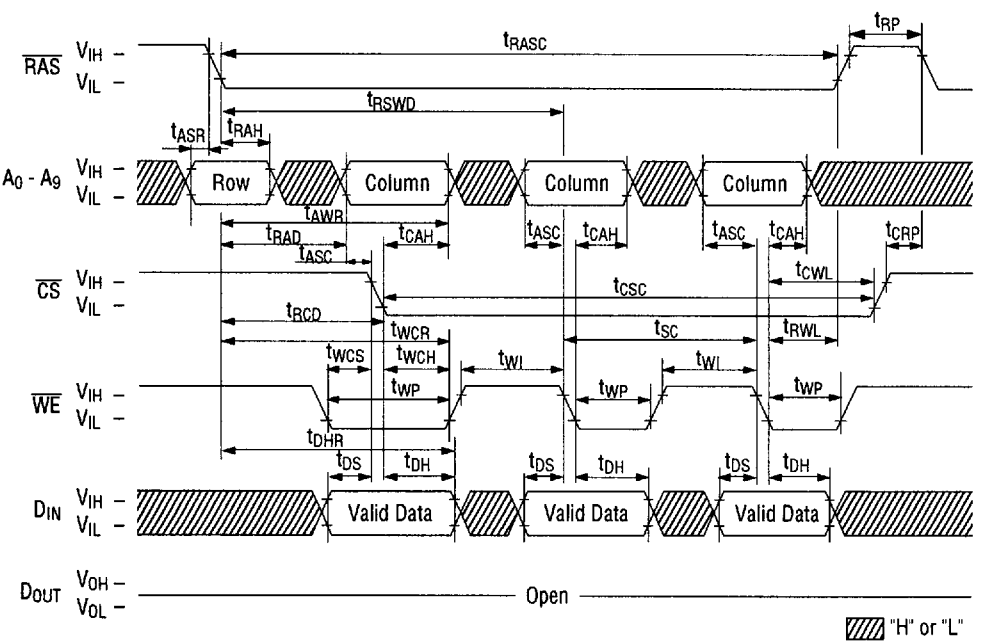
Static Column Mode Read Cycle



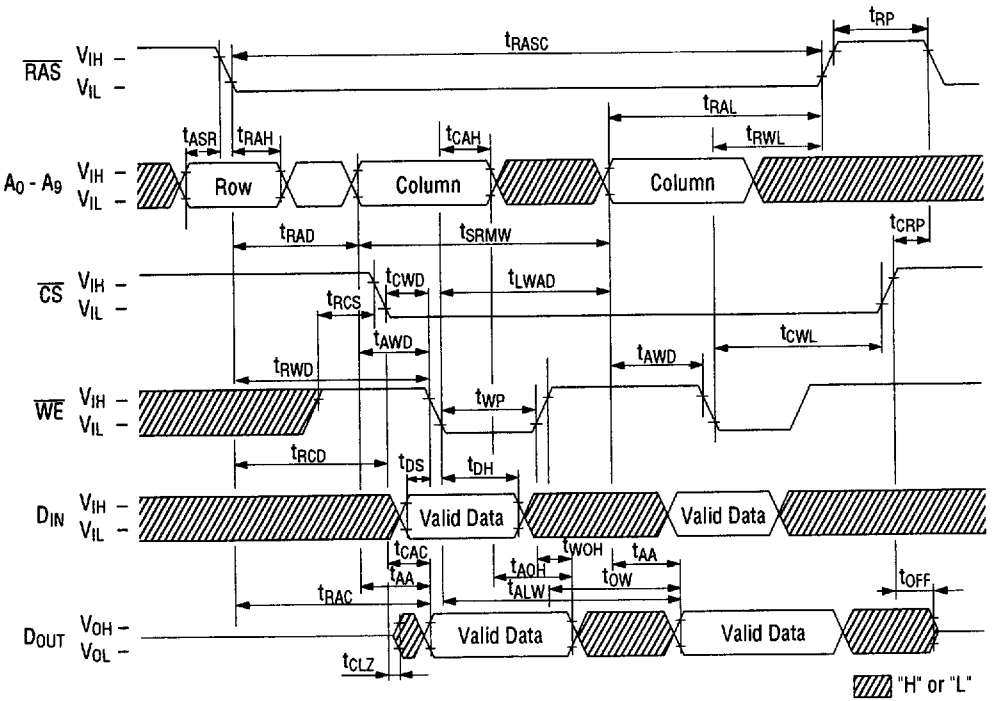
Static Column Mode Write Cycle (Early Write)



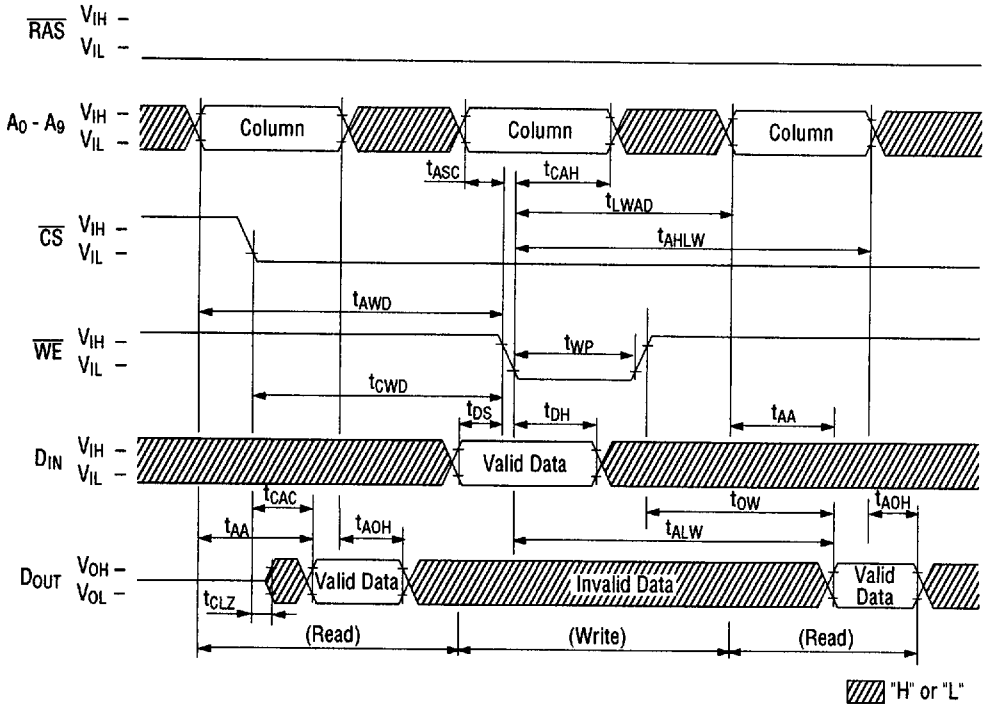
Static Column Mode Write Cycle (Early Write)



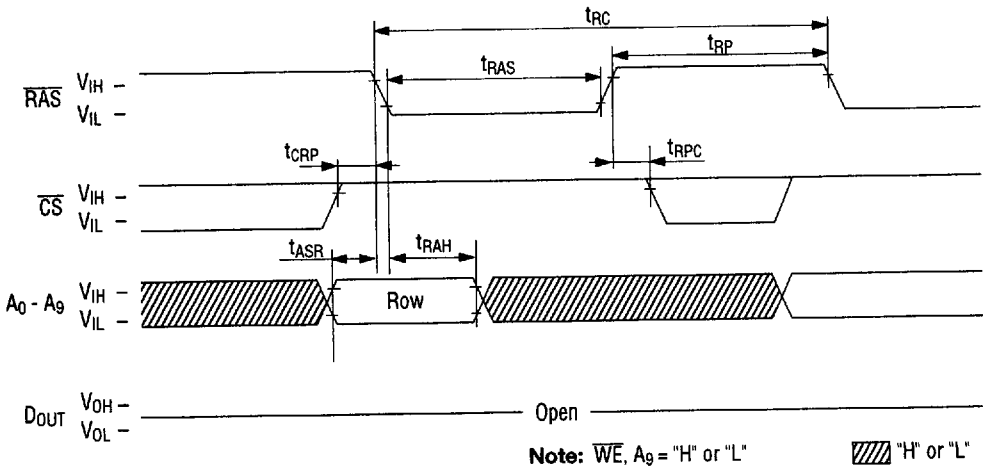
Static Column Mode Read Modify Write Cycle



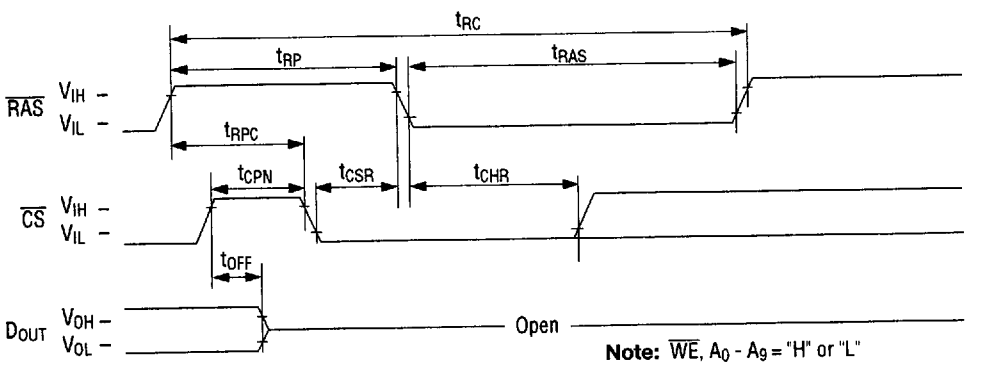
Static Column Mode Read/Write Mixed Cycle



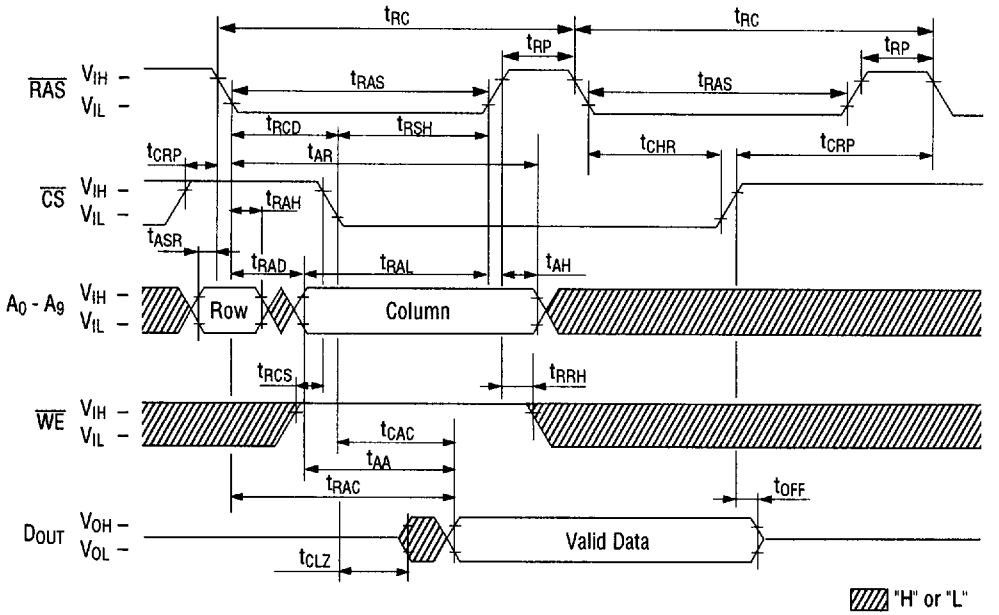
$\overline{RAS}$-only Refresh Cycle



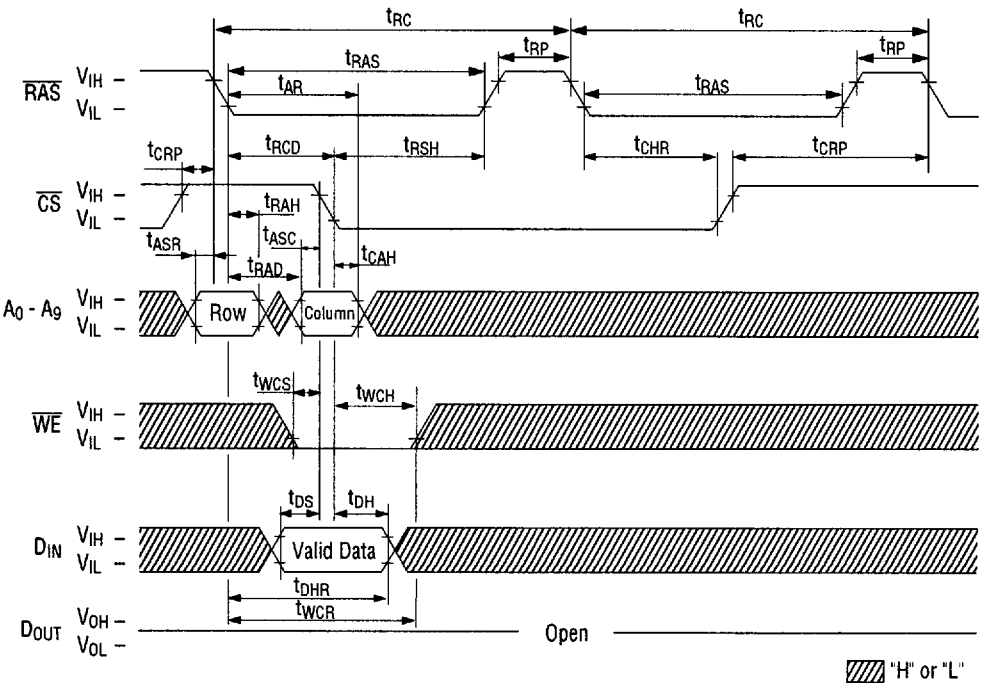
$\overline{CS}$ Before $\overline{RAS}$ Auto-refresh Cycle



Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



$\overline{CS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle