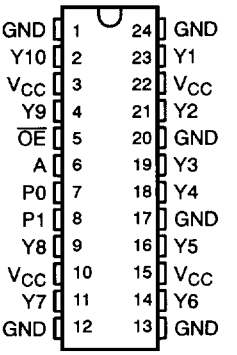
- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **LVTTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Ten Outputs**
- **Outputs Have Internal Series Damping Resistor To Reduce Transmission Line Effects**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC2351 is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable ($\overline{OE}$) input is provided to disable the outputs to a high-impedance state. Each output has an internal series damping resistor to improve signal integrity at the load. The CDC2351 operates at 3.3-V V_{CC}.

The CDC2351 propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part to part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The CDC2351 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS
A	$\overline{OE}$	Yn
L	H	Z
H	H	Z
L	L	L
H	L	H

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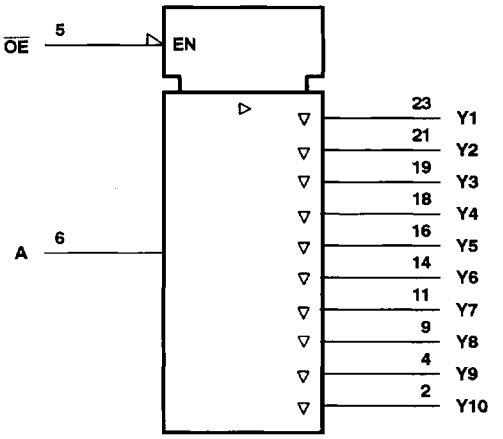
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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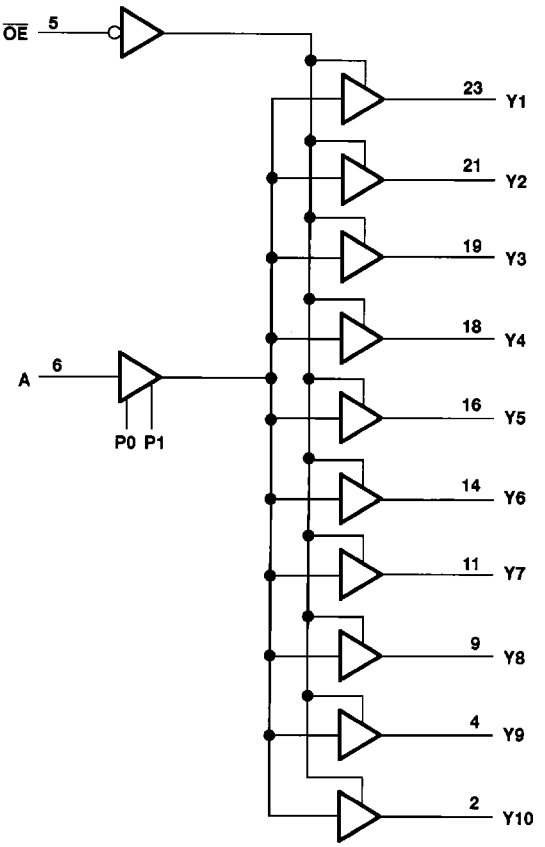
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 3.6 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_I < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and negative-voltage rating may be exceeded if the input clamp-current rating is observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
f_{clock}	Input clock frequency		100	MHz
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	MIN	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = – 32 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 32 mA					0.5	V
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1		±1	µA
I_O†	V_{CC} = 3.6 V,	V_O = 2.5 V						mA
I_{OZ}	V_{CC} = 3.6 V,	V_{CC} = 3 V or 0						µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high					mA
			Outputs low					
			Outputs disabled					
C_i	V_I = V_{CC} or GND							pF
C_o	V_O = V_{CC} or GND							pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V, T_A = 25°C MIN	TYP	MAX	V_{CC} = 3 V to 3.6 V, T_A = 0°C to 70°C MIN	MAX	UNIT
t_{PLH}	A	Y						ns
t_{PHL}								
t_{PZH}	$\overline{OE}$	Y						ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Y						ns
t_{PLZ}								
$t_{sk(o)}$	A	Y		0.3	0.5		0.5	ns
$t_{sk(p)}$	A	Y		0.6	0.8		0.8	ns
$t_{sk(pr)}$	A	Y			1		1	ns
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

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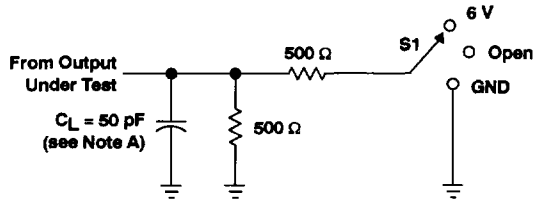
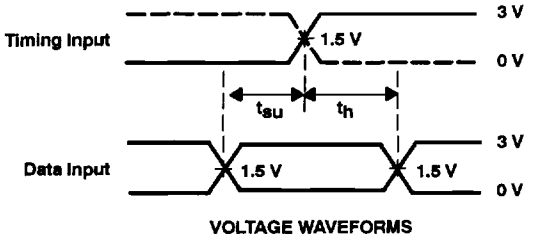
PARAMETER MEASUREMENT INFORMATION

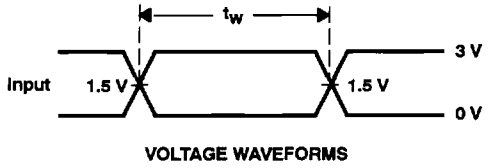


LOAD CIRCUIT

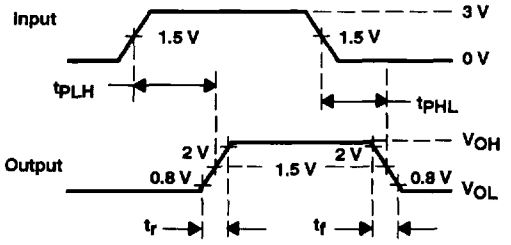
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



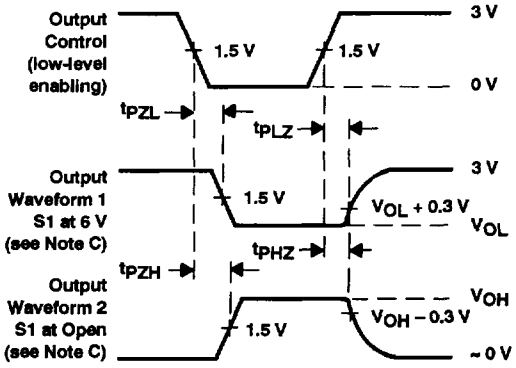
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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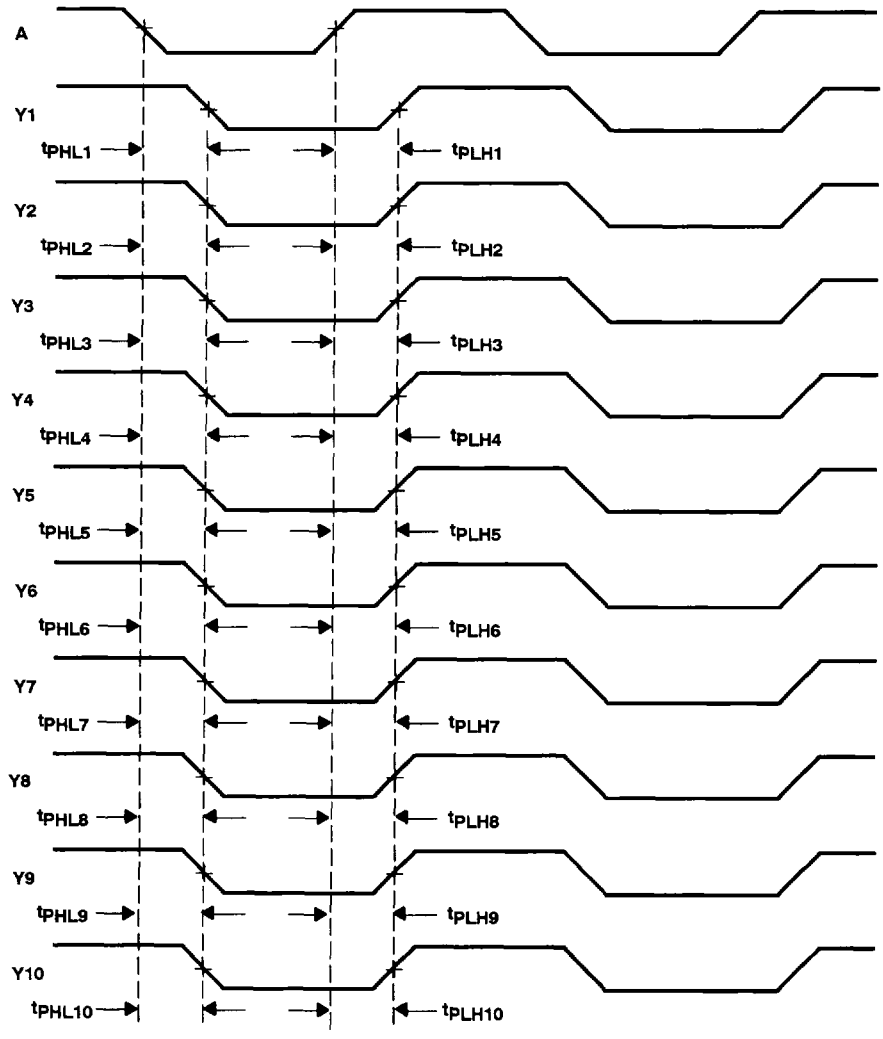
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$