XQ UltraScale Architecture Data Sheet: Overview

DS895 (v2.1) July 9, 2021 **Product Specification**

General Description

The Defense-grade XQ UltraScale™ architecture-based devices extend the equivalent commercial offerings, adding unique ruggedized packages, extended operating temperature range support, and added environmental qualification testing. This XQ portfolio spans the following families, with each offering a unique mix of features.

XQ Kintex® UltraScale FPGAs: High-performance FPGAs with a focus on price/performance, using both monolithic and next-generation stacked silicon interconnect (SSI) technology. High DSP and block RAM-to-logic ratios and next-generation transceivers, combined with low-cost packaging, enable an optimum blend of capability and cost.

XQ Kintex UltraScale+™ FPGAs: Increased performance and on-chip UltraRAM memory to reduce BOM cost. The ideal mix of high-performance peripherals and cost-effective system implementation. Kintex UltraScale+ FPGAs have numerous power options that deliver the optimal balance between the required system performance and the smallest power envelope.

XQ Virtex® UltraScale+ FPGAs: The highest transceiver bandwidth, highest DSP count, and highest on-chip and in-package memory available in the UltraScale architecture. Virtex UltraScale+ FPGAs also provide numerous power options that deliver the optimal balance between the required system performance and the smallest power envelope.

XQ Zynq® UltraScale+ MPSoCs: Combine the Arm® v8-based Cortex®-A53 high-performance energy-efficient 64-bit application processor with the Arm Cortex-R5F real-time processor and the UltraScale architecture to create the industry's first Defense-grade MPSoCs. Provide unprecedented power savings, heterogeneous processing, and programmable acceleration.

XQ Zynq UltraScale+ RFSoCs: Combine RF data converter subsystem and forward error correction with industry-leading programmable logic and heterogeneous processing capability. Integrated RF-ADCs, RF-DACs, and soft-decision FECs (SD-FEC) provide the key subsystems for multiband, multi-mode cellular radios and cable infrastructure.

XQ Device Comparisons

Table 1: **Device Resources**(1)

	XQ Kintex UltraScale FPGA	XQ Kintex UltraScale+ FPGA	XQ Virtex UltraScale+ FPGA	XQ Zynq UltraScale+ MPSoC	XQ Zynq UltraScale+ RFSoC
MPSoC Processing System				✓	✓
RF-ADC/DAC and SD-FEC					✓
System Logic Cells (K)	530–1,451	475–1,143	862–2,835	154–1,143	930
Block Memory (Mb)	21.1–75.9	16.9–34.6	25.3–70.9	5.1–34.6	38.0
UltraRAM (Mb)		18–36	90–270	0–36	22.5
HBM DRAM (GB)			0(2)		
DSP (Slices)	1,920–5,520	1,824–1,968	2,280–9,216	360–3,528	4,272
DSP Performance (GMAC/s)(3)	7,297	3,050	14,284	5,468	6,621
Transceivers	16–64	16–56	40–96	0–48	8–16
Max. Transceiver Speed (Gb/s)	16.3	28.2	28.2	28.2	28.2
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	2,402	5,416	1,950	902
I/O Pins	312–728	280–512	416–832	82–644	152–408

Notes:
1. Metrics given in this table pertain to the XQ ruggedized package devices. For non-ruggedized device variants consult Xilinx sales.
2. HBM not currently offered in an XQ ruggedized Package; consult Xilinx sales for further details and options.
3. Calculated based on XQ maximum DSP clock rate for a Symmetric FIR Filter, e.g. for KU040 with 1920 DSP48s, -2 speed-grade DSP48 F_{MAX}=661MHz, GMACs=2x0.661x1,920=2,538.

Table 2: **XQ Zynq UltraScale+ MPSoC and RFSoC Processor System Features**

	MPSoC		RFSoC
	EG Devices	**EV Devices**	**DR Devices**
APU	Quad-core Arm Cortex-A53	Quad-core Arm Cortex-A53	Quad-core Arm Cortex-A53
RPU	Dual-core Arm Cortex-R5F	Dual-core Arm Cortex-R5F	Dual-core Arm Cortex-R5F
GPU	Mali™-400MP2	Mali-400MP2	–
VCU	–	H.264/H.265	–

Key Defense-grade Ruggedized Package Features

- Ruggedized packaging
- MIL-STD-883 group D Qualification testing
- Military (M) temperature support of –55°C to +125°C (optionally available)
- Full range extended temperature testing
- Mask set control
- Full compliance with MIL-PRF-38535 Pb content standards
- Longer-term availability
- Anti-counterfeiting features
- Available information assurance (IA) methodology
- Available anti-tamper (AT) technology

Ruggedized Packaging

XQ ruggedized packages have a unique 4-corner lid that has wider vent openings around the periphery. This lid simplifies the board-level assembly process for applications requiring conformal coating. In the conformal coating process, boards go through a caustic etching process to achieve the required conformal coating adherence. The caustic etching material or other corrosive chemicals can become trapped inside of non-ruggedized packaging, leading to reliability concerns with flip-chip packaging. With the XQ ruggedized package, the 4-corner lid significantly simplifies cleaning and manufacturing process, allowing the device to be fully flushed prior to sealing the device/board with conformal coating.

MIL-STD-883 group D specification stress testing is completed prior to production release of the defense grade (XQ) devices. Qualification reports are available for the XQ UltraScale architecture ruggedized devices.

MIL-STD-883 group D Qualification testing for Defense-grade products includes the following:

- Physical dimensions (TM 2016)
- Thermal shock (TM 1011 condition B 15 cycles)
- Temperature cycling (TM 1010 condition C 100 cycles)
- Moisture Resistance (TM 1004)
- Vibration - Variable Frequency (TM 2007 Condition A minimum)
- Constant Acceleration - Centrifuge (TM 2001 Condition D minimum - Y1 orientation only)
- Salt Atmosphere (TM 1009 Condition A minimum)

Full Range Extended Temperature Testing

Ruggedized XQ devices are offered in Military (M) and Industrial (I) temperature grades:

- Military: –55°C to +125°C
- Industrial: –40°C to +100°C

Full-range extended temperature testing is offered on XQ ruggedized devices and includes full functional and parametric testing at room temperature as well as hot and cold temperature extremes. Xilinx tests 100% of all die at wafer sort and 100% of all devices at Final Production testing. Xilinx continuously improves the test coverage of its products through advancements in design for test (DFT) methods spanning digital logic, IP cores, memory elements, I/O cells, and many other areas. Xilinx achieves very high test coverage with industry-leading manufacturing and foundry processes, as confirmed by a low PPM failure rate and low customer return rates; for more information see www.xilinx.com/quality.

Mask Set Control

Mask-set control is valuable for secure and critical applications where a mask-set change can trigger a detailed silicon-level analysis, re-verification, and/or re-certification process. Ruggedized XQ products have a locked mask-set throughout the production life cycle. In the event that a technical change must be made, a formal customer notification process is required for these XQ devices.

Full Compliance with MIL-PRF-38535 Pb Content Standards

XQ UltraScale architecture ruggedized devices are fully compliant to MIL-PRF-38535 with respect to Pb content in all solder interfaces and contain a minimum of 3% Pb by weight. Aerospace and Defense applications can require compliance to government flow-down requirements where materials cannot contain more than 97% tin (Sn), due to a risk that tin whiskers might develop in the case of greater than 97% tin, such as in RoHS solder interfaces. Components with solder terminals comprised of 3% Pb are not prone to tin whisker growth. In addition, the most commonly used lead-free solders are known to be more brittle than tin-lead solders, therefore, in high vibration and shock applications, the ductile tin-lead solder joints might be required.

Anti-Counterfeiting Features

XQ UltraScale architecture-based devices offer multiple levels of anti-counterfeiting protection. Protection starts with the device package itself, since the unique 4-corner lid construction differentiates it from the commercial product. This aspect makes it significantly more difficult for counterfeiters, who can no longer simply re-mark a commercial device and sell it as a Defense-grade product. Supplementing this packaging is a unique laser marking, which uses micro-watermarking characters and patterns, whereby certain elements can be verified by the end-user. Other elements can only be verified by Xilinx.

Overview of Device Families

UltraScale devices are based on an architecture that spans multiple nodes from the planar 20nm SoC process to 16nm FinFET process technology, while also scaling from monolithic devices through high-density multi-die 3D ICs. The UltraScale architecture provides diverse benefits and advantages to an array of markets and applications.

This architecture combines enhancements in the configurable logic block (CLB), a dramatic increase in device routing, and a revolutionary ASIC-like clocking architecture with high-performance DSP, memory interface PHYs, and serial transceivers. All UltraScale architecture-based programmable logic, inclusive of that found in these FPGAs, MPSoCs, and RFSoCs, are capable of pushing the system performance-per-watt envelope, enabling breakthrough speeds, with high device utilization. High system performance and power reduction innovations make the UltraScale architecture the logical choice for many next-generation applications.

The UltraScale architecture further adds new memory structures with UltraRAM and HBM, as well as MPSoC and RFSoC technologies. These technologies enable increased integration and performance per watt.

Built upon Xilinx's UltraScale architecture, the UltraScale+ families achieve a significant boost in performance-per-watt by using TSMC's 16nm FinFET+ process node. Xilinx provides scalability and package migration within the FPGA families and SoC families that are built on the UltraScale architecture.

XQ Kintex UltraScale FPGAs

Ruggedized XQ UltraScale Kintex FPGAs enable designers with a broad selection of devices to advance state-of-the-art integrated aerospace & defense solutions, with flexible and dynamically reconfigurable high-performance programmable logic and DSP, 16Gb/s transceivers, and ruggedized-packages with support for –55°C to +125°C operation.

XQ Kintex UltraScale FPGAs are second generation Kintex devices and expand the mid-range device offering with increased throughput and reduced latency for real-time DSP-intensive applications.

XQ Kintex UltraScale devices offer ASIC-class system-level performance, clock management, and power management for high efficiency in performance-per-watt. These FPGAs combine 16G transceivers, integrated PCI Express, 100G Ethernet MAC/PCS, Interlaken blocks, analytical placement and co-optimization, and careful process optimization to achieve the highest performance-per-watt attainable at the 20nm SoC process node. In addition, the XQ Kintex UltraScale family leverages new IP Integrator technology, which allows designers to quickly stitch IP together by designing at the interface level. The IP Integrator provides correct-by-construction signal level connectivity to enable an even higher level of productivity and integration. Based on the ASIC-class advantage of the Xilinx UltraScale architecture, XQ Kintex UltraScale devices are co-optimized with the Vivado® Design Suite and leverage the UltraFAST™ design methodology to accelerate time to market.

XQ Kintex UltraScale+ FPGAs

Ruggedized XQ UltraScale+ Kintex FPGAs, enable designers with a broad selection of devices to advance state-of-the-art integrated aerospace & defense solutions, with flexible and dynamically reconfigurable high-performance programmable logic and DSP, 16Gb/s and 28Gb/s transceivers, and ruggedized-packages with support for –55°C to +125°C operation.

XQ Kintex UltraScale+ devices deliver the industry's most effective solution for system performance-per-watt with ASIC-class serial connectivity. These devices expand the mid-range by delivering the highest throughput with lowest latency for real-time DSP-intensive applications. Based on the ASIC-class advantage of the UltraScale architecture, XQ Kintex UltraScale+ devices are co-optimized with the Vivado Design Suite and leverage the UltraFAST design methodology to accelerate time to market.

XQ Virtex UltraScale+ FPGAs

Ruggedized XQ UltraScale+ Virtex FPGAs, enable designers with a broad selection of devices to advance state-of-the-art integrated aerospace & defense solutions, with flexible and dynamically reconfigurable high-performance programmable logic and DSP, 28Gb/s transceivers, and ruggedized-packages with support for –55°C to +125°C operation (VU3P only).

XQ Virtex UltraScale+ devices provide 3X system-level performance per-watt compared to 7 series FPGAs, enabling increased system integration and bandwidth for a wide range of applications. With optional integrated high-bandwidth memory (HBM) or 58G PAM4 transceivers, the XQ Virtex UltraScale+ family delivers a step-function increase in performance, bandwidth, and reduced latency for systems demanding massive data flow and packet processing. Based on the ASIC-class advantage of the UltraScale architecture, XQ Virtex UltraScale+ devices are co-optimized with the Vivado Design Suite and leverage the UltraFAST design methodology to accelerate time to market.

XQ Zynq UltraScale+ MPSoCs

XQ Zynq UltraScale+ MPSoCs enable designers with a broad selection of devices to advance state-of-the-art integrated aerospace & defense solutions, with the industry's first heterogeneous multiprocessor SoC devices with flexible and dynamically reconfigurable high-performance programmable logic and DSP, 16Gb/s and 28Gb/s transceivers, quad-core Arm Cortex-A53, dual-core Arm Cortex-R5F embedded processors, and optional features including Arm Mali-400 GPU, 4k60 H.265/H.264 video codec, 256-bit PUF, and XQ ruggedized packages with support for –55°C to +125°C operation.

The UltraScale MPSoC architecture provides: processor scalability from 32 to 64 bits with support for virtualization, the combination of application and real-time processors, graphics/video processing, waveform and packet processing, next-generation interconnect and memory, advanced power management, and technology enhancements that deliver multi-level security, safety, and reliability. Xilinx offers a large number of soft IP cores for the XQ Zynq UltraScale+ MPSoC family. Stand-alone and Linux device drivers are available for the peripherals in the PS and the PL. Xilinx's Vivado Design Suite, SDK™, and PetaLinux development environments enable rapid product development for software, hardware, and systems engineers. The Arm-based PS also brings a broad range of third-party tools and IP providers in combination with Xilinx's existing PL ecosystem.

The XQ Zynq UltraScale+ MPSoC family delivers unprecedented processing, I/O, and memory bandwidth in the form of an optimized mix of heterogeneous processing engines embedded in a next-generation,

high-performance, on-chip interconnect with appropriate on-chip memory subsystems. The heterogeneous processing and programmable engines, which can be optimized for different application tasks, enable the XQ Zynq UltraScale+ MPSoCs to deliver the extensive performance and efficiency required to address next-generation smarter systems while retaining backwards compatibility with the original Zynq-7000 SoC family. The UltraScale MPSoC architecture also incorporates multiple levels of security, increased safety, and advanced power management, which are critical requirements of next-generation smarter systems. Xilinx's embedded UltraFast design methodology fully exploits the ASIC-class capabilities afforded by the UltraScale MPSoC architecture while supporting rapid system development.

The inclusion of an application processor enables high-level operating system support, e.g., Linux. Other standard operating systems used with the Cortex-A53 processor are also available for the XQ Zynq UltraScale+ MPSoC family. The PS and the PL are on separate power domains, enabling users to power down the PL for power management if required. The processors in the PS always boot first, allowing a software centric approach for PL configuration. PL configuration is managed by software running on the CPU, so it boots similar to an ASSP.

XQ Zynq UltraScale+ RFSoCs

XQ Zynq UltraScale+ RFSoCs enable designers with a broad selection of devices to advance state-of-the-art integrated aerospace & defense solutions, with the industry's first heterogeneous multiprocessor SoC devices with flexible and dynamically reconfigurable high-performance programmable logic and DSP, 28Gb/s transceivers, quad-core Arm Cortex-A53, dual-core Arm Cortex-R5F embedded processors, and optional features of high-speed 5GSPS ADCs and 9.85GSPS DACs, optional 256-bit PUF, and ruggedized-packages with support for –55°C to +125°C operation.

Combining the processing system with UltraScale architecture programmable logic and RF-ADCs, RF-DACs, and soft-decision FECs, the Zynq UltraScale+ RFSoC family is capable of implementing a complete software-defined radio including direct RF sampling data converters. Zynq UltraScale+ RFSoCs are additionally suitable for a broad spectrum of radar applications.

Zynq UltraScale+ RFSoCs integrate up to 16 channels of RF-ADCs and RF-DACs. The RF data converters also include power efficient digital down converters (DDCs) and digital up converters (DUCs) that include programmable interpolation and decimation, NCO, and complex mixer. The DDCs and DUCs can also support dual-band operation.

The soft-decision FEC (SD-FEC) is a highly flexible forward error correction engine capable of operating in Turbo decoding mode for wireless applications such as LTE and LDPC encode/decode modes.

XQ Kintex UltraScale FPGA Feature Summary

Table 3: **XQ Kintex UltraScale Ruggedized FPGA Feature Summary**

	XQKU040	XQKU060	XQKU095	XQKU115
System Logic Cells	530,250	725,550	1,176,000	1,451,100
CLB Flip-Flops	484,800	663,360	1,075,200	1,326,720
CLB LUTs	242,400	331,680	537,600	663,360
Maximum Distributed RAM (Mb)	7.0	9.1	4.7	18.3
Block RAM/FIFO w/ECC (36Kb)	600	1,080	1,680	2,160
Total Block RAM (Mb)	21.1	38.0	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	10	12	16	24
I/O DLLs	40	48	64	64
Maximum HP I/Os(1)	416	520	650	624
Maximum HR I/Os(2)	104	104	52	104
DSP Slices	1,920	2,760	768	5,520
System Monitor	1	1	1	2
PCIe Gen3 x8	3	3	4	6
150G Interlaken	0	0	2	0
100G Ethernet	0	0	2	0
GTH 16.3Gb/s Transceivers(3)	20	32	32	64
GTY 16.3Gb/s Transceivers(4)	0	0	32	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in RB packages support data rates up to 12.5Gb/s. See Table 13.
4. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See Table 13.

XQ Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 4: **XQ Kintex UltraScale Ruggedized Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	XQKU040	XQKU060	XQKU095	XQKU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY(4)	HR, HP GTH
RBA676(5)	27x27	104, 208 16			
RFA1156	35x35	104, 416 20	104, 416 28	52, 468 20, 8	
RLD1517	40x40				104, 234 64
RLF1924	45x45				104, 624 64

Notes:
1. Go to Ordering Information for package designation details.
2. RB/RF/RL packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., B2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
4. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.
5. GTH transceivers in RB packages support data rates up to 12.5Gb/s.

XQ Kintex UltraScale+ FPGA Feature Summary

Table 5: **XQ Kintex UltraScale+ Ruggedized FPGA Feature Summary**

	XQKU5P	XQKU15P
System Logic Cells	474,600	1,143,450
CLB Flip-Flops	433,920	1,045,440
CLB LUTs	216,960	522,720
Max. Distributed RAM (Mb)	6.1	9.8
Block RAM Blocks	480	984
Block RAM (Mb)	16.9	34.6
UltraRAM Blocks	64	128
UltraRAM (Mb)	18.0	36.0
CMTs (1 MMCM and 2 PLLs)	4	11
Max. HP I/O(1)	208	468
Max. HD I/O(2)	96	96
DSP Slices	1,824	1,968
System Monitor	1	1
GTH Transceiver 16.3Gb/s	0	32
GTY Transceivers 28.2Gb/s(3)	16	24
Transceiver Fractional PLLs	8	38
PCIe Gen3 x16	1	5
150G Interlaken	0	4
100G Ethernet w/RS-FEC	1	4

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFRB784 to 12.5Gb/s; FFRA1156 to 16.3Gb/s. See Table 6.

XQ Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 6: **XQ Kintex UltraScale+ Ruggedized Device-Package Combinations and Maximum I/Os**

Package (1)(2)(4)	Package Dimensions (mm)	XQKU5P	XQKU15P
		HD, HP GTH, GTY	HD, HP GTH, GTY
SFRB784(3)	23x23	96, 208 0, 16	
FFRB676	27x27	72, 208 0, 16	
FFRA1156(3)	35x35		48, 468 20, 8
FFRE1517	40x40		96, 416 32, 24

Notes:

1. Go to Ordering Information for package designation details.
2. FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. GTY transceiver line rates are package limited: SFRB784 to 12.5Gb/s; FFRA1156 to 16.3Gb/s.
4. Packages with the same last letter and number sequence, e.g., A676, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.

XQ Virtex UltraScale+ FPGA Feature Summary

Table 7: **XQ Virtex UltraScale+ Ruggedized FPGA Feature Summary**

	XQVU3P	XQVU7P	XQVU11P
System Logic Cells	862,050	1,724,100	2,835,000
CLB Flip-Flops	788,160	1,576,320	2,592,000
CLB LUTs	394,080	788,160	1,296,000
Max. Distributed RAM (Mb)	12.0	24.1	36.2
Block RAM Blocks	720	1,440	2,016
Block RAM (Mb)	25.3	50.6	70.9
UltraRAM Blocks	320	640	960
UltraRAM (Mb)	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–
CMTs (1 MMCM and 2 PLLs)	10	20	12
Max. HP I/O(1)	520	832	416
DSP Slices	2,280	4,560	9,216
System Monitor	1	2	3
GTY Transceivers 28.2Gb/s	40	76	96
GTM Transceivers 58.0Gb/s	–	–	–
100G / 50G KP4 FEC	–	–	–
Transceiver Fractional PLLs	20	40	48
PCIe Gen3 x16	2	4	3
150G Interlaken	3	6	6
100G Ethernet w/RS-FEC	3	6	9

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.

XQ Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 8: **XQ Virtex UltraScale+ Ruggedized Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)	Package Dimensions (mm)	XQVU3P	XQVU7P	XQVU11P
		HP, GTY	HP, GTY	HP, GTY
FFRC1517	40x40	520, 40		
FLRA2104	47.5x47.5		832, 52	
FLRB2104	47.5x47.5		702, 76	
FLRC2104	47.5x47.5			416, 96

Notes:
1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.
4. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.

XQ Zynq UltraScale+ MPSoC: Feature Summary

Table 9: **XQ Zynq UltraScale+ Ruggedized MPSoC Device Feature Summary**

	XQZU3EG	XQZU5EV	XQZU7EV	XQZU9EG	XQZU11EG	XQZU15EG	XQZU19EG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore™ with CoreSight™; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache						
Real-Time Processing Unit	Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM						
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC						
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters						
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII						
Graphic Processing Unit	Arm Mali-400MP2; 64KB L2 Cache						
System Logic Cells	154,350	256,200	504,000	599,550	653,100	746,550	1,143,450
CLB Flip-Flops	141,120	234,240	460,800	548,160	597,120	682,560	1,045,440
CLB LUTs	70,560	117,120	230,400	274,080	298,560	341,280	522,720
Distributed RAM (Mb)	1.8	3.5	6.2	8.8	9.1	11.3	9.8
Block RAM Blocks	216	144	312	912	600	744	984
Block RAM (Mb)	7.6	5.1	11.0	32.1	21.1	26.2	34.6
UltraRAM Blocks	0	64	96	0	80	112	128
UltraRAM (Mb)	0	18.0	27.0	0	22.5	31.5	36.0
DSP Slices	360	1,248	1,728	2,520	2,928	3,528	1,968
CMTs	3	4	8	4	8	4	11
Max. HP I/O(1)	156	156	312	208	416	208	572
Max. HD I/O(2)	96	96	48	120	96	120	96
System Monitor	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s(3)	0	16	20	24	32	24	32
GTY Transceivers 28.2Gb/s	0	0	0	0	16	0	16
Transceiver Fractional PLLs	0	8	12	12	24	12	36
PCIe Gen3 x16	0	2	2	0	4	0	5
150G Interlaken	0	0	0	0	1	0	4
Video Codec Unit (VCU)	–	1	1	–	–	–	–
100G Ethernet w/ RS-FEC	0	0	0	0	2	0	4

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFRC784 package support data rates up to 12.5Gb/s. See Table 10.

XQ Zynq UltraScale+ MPSoC: Device-Package Combinations and Maximum I/Os

Table 10: **XQ Zynq UltraScale+ MPSoC Ruggedized Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	XQZU3EG	XQZU5EV	XQZU7EV	XQZU9EG	XQZU11EG	XQZU15EG	XQZU19EG
		PSIO, HDIO, HPIO GTR, GTH, GTY						
SFRA484(6)	19x19	170, 24, 58 4, 0, 0						
SFRC784(7)	23x23	214, 96, 156 4, 0, 0	214, 96, 156 4, 4, 0					
FFRB900	31x31		214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0				
FFRC900	31x31				214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0	
FFRB1156	35x35				214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0	
FFRC1156	35x35			214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0		
FFRB1517	40x40							214, 72, 572 4, 16, 0
FFRC1760	42.5x42.5					214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16

Notes:

1. Go to Ordering Information for package designation details.
2. FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. Packages that bond out 170 PS I/O support DDR 32-bit only.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFRC784 package support data rates up to 12.5Gb/s.

XQ Zynq UltraScale+ RFSoC: Device Feature Summary

Table 11: **Zynq UltraScale+ Ruggedized RFSoC Feature Summary**

		XQZU21DR	XQZU28DR	XQZU29DR	XQZU48DR	XQZU49DR
12-bit RF-ADC w/ DDC	# of ADCs	–	8	16	–	–
	Max Rate (GSPS)	–	4.096	2.058	–	–
14-bit RF-ADC w/ DDC	# of ADCs	–	–	–	8	16
	Max Rate (GSPS)	–	–	–	5.0	2.5
14-bit RF-DAC w/ DUC	# of DACs	–	8	16	8	16
	Max Rate (GSPS)	–	6.554	6.554	9.85(1)	9.85(1)
SD-FEC		8	8	0	8	0
Application Processing Unit		Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON and Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache				
Real-Time Processing Unit		Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM				
Embedded and External Memory		256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC				
General Connectivity		214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; Watchdog Timers; Triple Timer Counters				
High-Speed Connectivity		4 PS-GTR; PCIe® Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII				
System Logic Cells		930,300	930,300	930,300	930,300	930,300
CLB Flip-Flops		850,560	850,560	850,560	850,560	850,560
CLB LUTs		425,280	425,280	425,280	425,280	425,280
Distributed RAM (Mb)		13.0	13.0	13.0	13.0	13.0
Block RAM Blocks		1,080	1,080	1,080	1,080	1,080
Block RAM (Mb)		38.0	38.0	38.0	38.0	38.0
UltraRAM Blocks		80	80	80	80	80
UltraRAM (Mb)		22.5	22.5	22.5	22.5	22.5
DSP Slices		4,272	4,272	4,272	4,272	4,272
CMTs		8	8	8	8	8
Maximum HP I/O		208	299	312	299	312
Maximum HD I/O		72	48	96	48	96
System Monitor		1	1	1	1	1
GTY Transceivers 28.2Gb/s		16	16	16	16	16
Transceivers Fractional PLLs		8	8	8	8	8
PCIe Gen3 x16		2	2	2	–	–
PCIe Gen3 x16 /Gen4 x8 /CCIX		–	–	–	2	2
150G Interlaken		1	1	1	1	1
100G Ethernet w/ RS-FEC		2	2	2	2	2

Notes:

1. For 10GSPS RF-DAC operation, contact your local Xilinx Sales Representative.

XQ Zynq UltraScale+ RFSoC: Device-Package Combinations and Maximum I/Os

Table 12: **Zynq UltraScale+ RFSoC Ruggedized Device-Package Combinations and Maximum I/Os**

Package[1]	Dimensions	XQZU21DR	XQZU28DR	XQZU29DR	XQZU48DR	XQZU49DR
		PSIO, HDIO, HPIO, PS-GTR, GTY, RF-ADC, RF-DAC				
FFRD1156	35x35	214, 72, 208 4, 16, 0, 0				
FFRE1156	35x35		214, 48, 104 4, 8, 8, 8		214, 48, 104 4, 8, 8, 8	
FFRG1517	40x40		214, 48, 299 4, 16, 8, 8			
FSRG1517	40x40				214, 48, 299 4, 16, 8, 8	
FFRF1760	42.5x42.5			214, 96, 312 4, 16, 16, 16		
FSRF1760	42.5x42.5					214, 96, 312 4, 16, 16, 16

Notes:

1. Packages with the same last letter and number sequence, e.g., B900, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.

Programmable Logic Details

UltraScale architecture-based devices (FPGAs, MPSoCs, and RFSoCs) contain programmable logic.

Device Layout

UltraScale architecture-based devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.

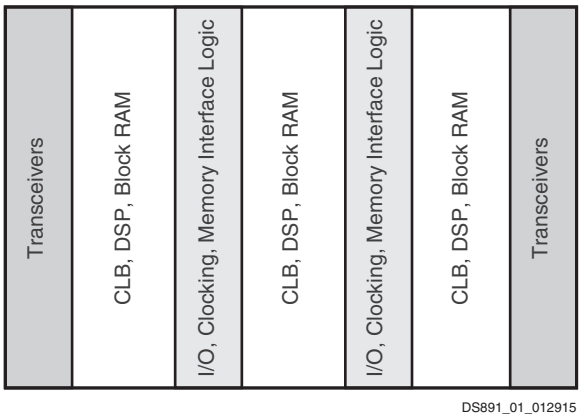


Figure 1: **Device with Columnar Resources**

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of a device divided into regions.

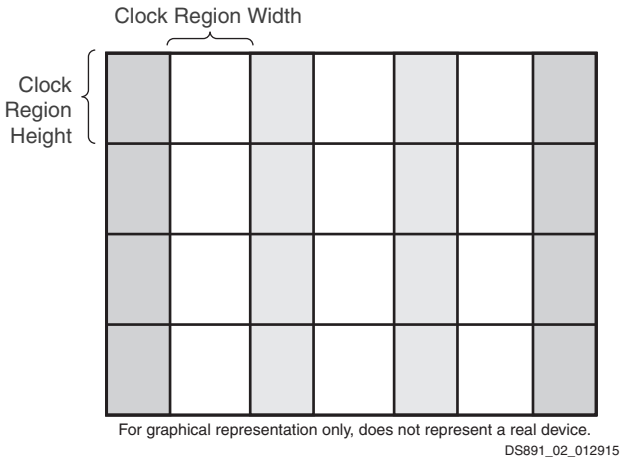


Figure 2: **Column-Based Device Divided into Clock Regions**

Input/Output

All UltraScale architecture-based devices have I/O pins for communicating to external components. In addition, in the PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC or RFSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in UltraScale architecture-based devices varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-range (HR), high-performance (HP), or high-density (HD). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP or HR pins per bank or 24 HD pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own V_{CCO} supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Four types of transceivers are used in the UltraScale architecture: GTH, GTY, and GTM in FPGAs, GTH and GTY in the PL in MPSoCs and RFSoCs, and PS-GTR in the PS of MPSoCs and RFSoCs. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. Table 13 compares the available transceivers.

Table 13: **Transceiver Information**

	XQ Kintex UltraScale		XQ Kintex UltraScale+		XQ Virtex UltraScale+		XQ Zynq UltraScale+ MPSoC and RFSoCs		
Type	GTH(1)	GTY(3)	GTH	GTY	GTY	GTM	PS-GTR	GTH	GTY
Qty(2)	16–64	0–8	20–60	0–60	40–128	0–48	4	0–44	0–28
Max. Data Rate	16.3Gb/s	16.3Gb/s	16.3Gb/s	32.75Gb/s	32.75Gb/s	58.0Gb/s	6.0Gb/s	16.3Gb/s	32.75Gb/s
Min. Data Rate	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	9.8Gb/s	1.25Gb/s	0.5Gb/s	0.5Gb/s

Notes:

1. GTH transceivers in RB packages support data rates up to 12.5Gb/s.
2. XQ ruggedized UltraScale+ devices have fewer GTs available in some cases, see Table 6, Table 8, Table 10, and Table 12 for clarification of available XQ ruggedized package features in each family.
3. UltraScale+ device GTY max data rate is limited to 28.2Gb/s.

GTH/GTY Transceivers

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter (GTH/GTY)

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver (GTH/GTY)

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally "auto-adapt" to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

GTM Transceivers

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 16 and 160 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter (GTM)

The transmitter is fundamentally a parallel-to-serial converter. These transmitter outputs drive pulse amplitude modulated signals with either 4 levels (PAM4) or 2 levels (NRZ) to the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data can optionally leverage a Reed-Solomon, RS(544,514) Forward Error Correction encoder and/or 64b66b data encoder. The bit-serial output signal drives two package pins with PAM4 differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver (GTM)

The receiver is fundamentally a serial-to-parallel converter, changing the incoming PAM4 differential signal into a parallel stream of words. The receiver takes the incoming differential data stream, feeds it through automatic gain compensation (AGC) and a continuous time linear equalizer (CTLE), after which it is sampled with a high-speed analog to digital converter. Further equalization is completed digitally via a decision feedback equalizer (DFE) and feed forward equalizer (FFE) implemented in DSP logic before the recovered bits are parallelized and provided to the PCS. This equalization provides the flexibility to receive data over channels ranging from very short chip-to-chip to high loss backplane applications across all supported rates. Clock recovery circuitry generates a clock derived from the high-speed PLL to clock in serial data and provides an appropriately divided and phase-aligned clock, RXOUTCLK, to internal logic. Parallel data can optionally be transferred into an RS-FEC and/or 64b/66b decoder before being presented to the FPGA interface.

Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port. UltraScale devices are compliant to the PCI Express Base Specification Revision 3.0. UltraScale+ devices are compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates.

The Root Port can be used to build the basis for a compatible root complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the device.

This block is highly configurable to system design requirements and can operate up to the maximum lane widths and data rates listed in Table 14.

Table 14: **PCIe Maximum Configurations**

	XQ Kintex UltraScale	XQ Kintex UltraScale+	XQ Virtex UltraScale+	XQ Zynq UltraScale+
Gen1 (2.5Gb/s)	x8	x16	x16	x16
Gen2 (5Gb/s)	x8	x16	x16	x16
Gen3 (8Gb/s)	x8	x16	x16	x16

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, FPGA, MPSoC, or RFSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

XQ Zynq UltraScale+ MPSoC and RFSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs and RFSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale architecture-based devices can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.

UltraRAM

UltraRAM is a high-density, dual-port, synchronous memory block available in UltraScale+ devices. Both of the ports share the same clock and can address all of the 4K x 72 bits. Each port can independently read from or write to the memory array. UltraRAM supports two types of write enable schemes. The first mode is consistent with the block RAM byte write enable mode. The second mode allows gating the data and parity byte writes separately. UltraRAM blocks can be connected together to create larger memory arrays. Dedicated routing in the UltraRAM column enables the entire column height to be connected together. If additional density is required, all the UltraRAM columns in an SLR can be connected together with a few fabric resources to create single instances of RAM approximately 100Mb in size. This makes UltraRAM an ideal solution for replacing external memories such as SRAM. Cascadable anywhere from 288Kb to 100Mb, UltraRAM provides the flexibility to fulfill many different memory requirements.

Block RAM

Every UltraScale architecture-based device contains a number of 36Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as 32K × 1; 16K × 2; 8K × 4; 4K × 9 (or 8); 2K × 18 (or 16); 1K × 36 (or 32); or 512 × 72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27 × 18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ FPGAs and the PL of XQ Zynq UltraScale+ MPSoC and RFSoCs is similar to the Kintex UltraScale and Virtex UltraScale devices but with additional features including a PMBus interface.

XQ Zynq UltraScale+ MPSoCs and RFSoCs contain an additional System Monitor block in the PS. See Table 15.

Table 15: **Key System Monitor Features**

	XQ Kintex UltraScale	XQ Kintex UltraScale+ XQ Virtex UltraScale+ XQ Zynq UltraScale+ PL	XQ Zynq UltraScale+ PS
ADC	10-bit 200kSPS	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP	JTAG, I2C, DRP, PMBus	APB

In FPGAs and the PL of the MPSoCs and RFSoCs, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the PS MPSoC and RFSoC uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

Core Processing System Details

XQ Zynq UltraScale+ MPSoCs and RFSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different XQ Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered Arm AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core Arm Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on Arm-v8A architecture, offering the best performance-to-power ratio. The Armv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port (ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the Arm CoreSight Debug System.

The key features of the APU include:

- 64-bit quad-core Arm Cortex-A53 MPCores. Features associated with each core include:
  - Arm v8-A Architecture
  - Operating target frequency: up to 1.5GHz
  - Single and double precision floating point:
    4 SP / 2 DP FLOPs
  - NEON Advanced SIMD support with single and double precision floating point instructions
  - A64 instruction set in 64-bit operating mode, A32/T32 instruction set in 32-bit operating mode
  - Level 1 cache (separate instruction and data, 32KB each for each Cortex-A53 CPU)
    - 2-way set-associative Instruction Cache with parity support
    - 4-way set-associative Data Cache with ECC support
  - Integrated memory management unit (MMU) per processor core

  - TrustZone for secure mode operation
  - Virtualization support
- Ability to operate in single-core, symmetric multicore, and asymmetric multicore modes
- Integrated 16-way set-associative 1MB Unified Level 2 cache with ECC support
- Interrupts and Timers
  - Generic interrupt controller (GIC-400)
  - Arm generic timers (4 timers per CPU)
  - One watchdog timer (WDT)
  - One global timer
  - Two triple timers/counters (TTC)
- CoreSight debug and trace support
  - Embedded Trace Macrocell (ETM) for instruction trace
  - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- ACP interface to PL for I/O coherency and Level 2 cache allocation
- ACE interface to PL for full coherency
- Power island gating on each processor core
- Optional eFUSE disable per core

Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core Arm Cortex-R5F PS. Cortex-R5F cores are 32-bit real-time processor cores based on Arm-v7R architecture. Each of the Cortex-R5F cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5F cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the Arm CoreSight Debug System.

- Dual-core Arm Cortex-R5F MPCores. Features associated with each core include:
  - Arm v7-R Architecture (32-bit)
  - Operating target frequency: Up to 600MHz
  - A32/T32 instruction set support
  - 4-way set-associative Level 1 caches (separate instruction and data, 32KB each) with ECC support
  - Integrated Memory Protection Unit (MPU) per processor
  - 128KB Tightly Coupled Memory (TCM) with ECC support

  - TCMs can be combined to become 256KB in lockstep mode
- Ability to operate in single-processor or dual-processor modes (split and lock-step)
- Dedicated SWDT and two Triple Timer Counters (TTC)
- CoreSight debug and trace support
  - Embedded Trace Macrocell (ETM) for instruction and trace
  - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- Optional eFUSE disable

PS Memory and Interconnect System

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for XQ Zynq UltraScale+ MPSoCs and RFSoCs and supports boot from managed NAND devices.

The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

Dynamic Memory Controller (DDRC)

- DDR3, DDR3L, DDR4, LPDDR3, LPDDR4
- Target data rate: Up to 2400Mb/s DDR4 operation in -1 speed grade
- 32-bit and 64-bit bus width support for DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit bus width support for LPDDR4 memory
- ECC support (using extra bits)
- Up to a total DRAM capacity of 32GB

- Low power modes
  - Active/precharge power down
  - Self-refresh, including clean exit from self-refresh after a controller power cycle
- Enhanced DDR training by allowing software to measure read/write eye and make delay adjustments dynamically
- Independent performance monitors for read path and write path
- Integration of PHY Debug Access Port (DAP) into JTAG for testing

The DDR memory controller is multi-ported and enables the PS and the PL to have shared access to a common memory. The DDR controller features six AXI slave ports for this purpose:

- Two 128-bit AXI ports from the Arm Cortex-A53 CPU(s), RPU (Arm Cortex-R5F and LPD peripherals), GPU, high speed peripherals (USB3, PCIe & SATA), and High Performance Ports (HP0 & HP1) from the PL through the Cache Coherent Interconnect (CCI)
- One 64-bit port is dedicated for the Arm Cortex-R5F CPU(s)
- One 128-bit AXI port from the DisplayPort and HP2 port from the PL
- One 128-bit AXI port from HP3 and HP4 ports from the PL
- One 128-bit AXI port from General DMA and HP5 from the PL

Xilinx Memory Protection Unit (XMPU)

- Region based memory protection unit
- Up to 16 regions
- Each region supports address alignment of 1MB or 4KB
- Regions can overlap; the higher region number has priority
- Each region can be independently enabled or disabled
- Each region has a start and end address

Xilinx Peripheral Protection Unit (XPPU)

- Provides peripheral protection support
- Up to 20 masters simultaneously
- Multiple aperture sizes
- Access control for a specified set of address apertures on a per master basis
- 64KB peripheral apertures and controls access on per peripheral basis

Domain-specific DMA Controllers

- Two general-purpose DMA controllers; one for each low and high power domains
- Eight independent channels per DMA
- Multiple transfer types:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory and
  - Scatter-gather
- 8 peripheral interfaces per DMA
- TrustZone per DMA for optional secure operation

PS-PL Interconnect

All the blocks are connected to each other and to the PL through a multi-layered Arm Advanced Microprocessor Bus Architecture (AMBA) AXI interconnect. The interconnect is non-blocking and supports multiple simultaneous master-slave transactions.

The interconnect is designed with latency sensitive masters, such as the Arm CPU, having the shortest paths to memory, and bandwidth critical masters, such as the potential PL masters, having high throughput connections to the slaves with which they need to communicate.

Traffic through the interconnect can be regulated through the Quality of Service (QoS) block in the interconnect. The QoS feature is used to regulate traffic generated by the CPU, DMA controller, and a combined entity representing the masters in the IOP.

The PS-PL interface includes:

- AMBA AXI4 interfaces for primary data communication
  - Six 128-bit/64-bit/32-bit High Performance (HP) Slave AXI interfaces from PL to PS.
    - Four 128-bit/64-bit/32-bit HP AXI interfaces from PL to PS DDR.
    - Two 128-bit/64-bit/32-bit high-performance coherent (HPC) ports from PL to cache coherent interconnect (CCI).
  - Two 128-bit/64-bit/32-bit HP Master AXI interfaces from PS to PL.
  - One 128-bit/64-bit/32-bit interface from PL to RPU in PS (PL_LPD) for low latency access to OCM.
  - One 128-bit/64-bit/32-bit AXI interface from RPU in PS to PL (LPD_PL) for low latency access to PL.
  - One 128-bit AXI interface (ACP port) for I/O coherent access from PL to Cortex-A53 cache memory. This interface provides coherency in hardware for Cortex-A53 cache memory.
  - One 128-bit AXI interface (ACE Port) for Fully coherent access from PL to Cortex-A53. This interface provides coherency in hardware for Cortex-A53 cache memory and the PL.
- Clocks and resets
  - Four PS clock outputs to the PL with start/stop control.
  - Four PS reset outputs to the PL.

High-Performance AXI Ports

The high-performance AXI4 ports provide access from the PL to DDR and high-speed interconnect in the PS. The six dedicated AXI memory ports from the PL to the PS are configurable as either 128-bit, 64-bit, or 32-bit interfaces. These interfaces connect the PL to the memory interconnect via a FIFO interface. Two of the AXI interfaces support I/O coherent access to the APU caches.

Each high-performance AXI port has these characteristics:

- Reduced latency between PL and processing system memory
- 1KB deep FIFO
- Configurable either as 128-bit, 64-bit, or 32-bit AXI interfaces
- Multiple AXI command issuing to DDR

Accelerator Coherency Port (ACP)

The XQ Zynq UltraScale+ MPSoC and RFSoC accelerator coherency port (ACP) is a 64-bit AXI slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACP directly connects the PL to the snoop control unit (SCU) of the Arm Cortex-A53 processors, enabling cache-coherent access to CPU data in the L2 cache. The ACP provides a low latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACP only snoops access in the CPU L2 cache, providing coherency in hardware. It does not support coherency on the PL side. So this interface is ideal for a DMA or an accelerator in the PL that only requires coherency on the CPU cache memories. For example, if a MicroBlaze™ processor in the PL is attached to the ACP interface, the cache of MicroBlaze processor will not be coherent with Cortex-A53 caches.

AXI Coherency Extension (ACE)

The XQ Zynq UltraScale+ MPSoC and RFSoC AXI coherency extension (ACE) is a 64-bit AXI4 slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACE directly connects the PL to the snoop control unit (SCU) of the Arm Cortex-A53 processors, enabling cache-coherent access to Cache Coherent Interconnect (CCI). The ACE provides a low-latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACE snoops accesses to the CCI and the PL side, thus, providing full coherency in hardware. This interface can be used to hook up a cached interface in the PL to the PS as caches on both the Cortex-A53 memories and the PL master are snooped thus providing full coherency. For example, if a MicroBlaze processor in the PL is hooked up using an ACE interface, then Cortex-A53 and MicroBlaze processor caches will be coherent with each other.

Static Memory Interfaces

The static memory interfaces support external static memories.

- ONFI 3.1 NAND flash support with up to 24-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash
- 8-bit eMMC interface supporting managed NAND flash

NAND ONFI 3.1 Flash Controller

- ONFI 3.1 compliant
- Supports chip select reduction per ONFI 3.1 spec
- SLC NAND for boot/configuration and data storage
- ECC options based on SLC NAND
  - 1, 4, or 8 bits per 512+spare bytes
  - 24 bits per 1024+spare bytes
- Maximum throughput as follows
  - Asynchronous mode (SDR) 24.3MB/s
  - Synchronous mode (NV-DDR) 112MB/s (for 100MHz flash clock)
- 8-bit SDR NAND interface
- 2 chip selects
- Programmable access timing
- 1.8V and 3.3V I/O
- Built-in DMA for improved performance

Quad-SPI Controller

- 4 bytes (32-bit) and 3 bytes (24-bit) address width
- Maximum SPI Clock at Master Mode at 150MHz
- Single, Dual-Parallel, and Dual-Stacked mode
- 32-bit AXI Linear Address Mapping Interface for read operation
- Up to 2 chip select signals
- Write Protection Signal
- Hold signals
- 4-bit bidirectional I/O signals
- x1/x2/x4 Read speed required
- x1 write speed required only
- 64 byte Entry FIFO depth to improve QSPI read efficiency
- Built-in DMA for improved performance

SD/SDIO 3.0 Controller

In addition to secure digital (SD) devices, this controller also supports eMMC 4.51.

- Host mode support only
- Built-in DMA
- 1/4-Bit SD Specification, version 3.0

- 1/4/8-Bit eMMC Specification, version 4.51
- Supports primary boot from SD Card and eMMC (Managed NAND)
- High speed, default speed, and low-speed support
- 1 and 4-bit data interface support
  - Low speed clock 0-400KHz
  - Default speed 0-25MHz
  - High speed clock 0-50MHz
- High speed Interface
  - SD UHS-1: 208MHz
  - eMMC HS200: 200MHz
- Memory, I/O, and SD cards
- Power control modes
- Data FIFO interface up to 512B

System-Level Management Features

Several functions span both the PS and PL and include:

- Reset Management
- Clock Management
- Power Domains
- PS Boot and Device Configuration
- Hardware and Software Debug Support

Reset Management

The reset management function provides the ability to reset the entire device or individual units within it. The PS supports these reset functions and signals:

- External and internal power-on reset signal
- Warm reset
- Watchdog timer reset
- User resets to PL
- Software, watchdog timer, or JTAG provided resets
- Security violation reset (locked down reset)

Clock Management

The PS in XQ Zynq UltraScale+ MPSoCs and RFSoCs is equipped with five phase-locked loops (PLLs), providing flexibility in configuring the clock domains within the PS. There are four primary clock domains of interest within the PS. These include the APU, the RPU, the DDR controller, and the I/O peripherals (IOP). The frequencies of all of these domains can be configured independently under software control.

Power Domains

The XQ Zynq UltraScale+ MPSoCs and RFSoCs contain four separate power domains. When they are connected to separate power supplies, they can be completely powered down independently of each other without consuming any dynamic or static power. The processing system includes:

- Full Power Domain (FPD)
- Low Power Domain (LPD)
- Battery Powered Domain (BPD)

In addition to these three Processing System power domains, the PL can also be completely powered down if connected to separate power supplies.

The Full Power Domain (FPD) consists of the following major blocks:

- Application Processing Unit (APU)
- DMA (FP-DMA)
- Graphics Processing Unit (GPU)
- Dynamic Memory Controller (DDRC)
- High-Speed I/O Peripherals

The Low Power Domain (LPD) consists of the following major blocks:

- Real-Time Processing Unit (RPU)
- DMA (LP-DMA)
- Platform Management Unit (PMU)
- Configuration Security Unit (CSU)
- Low-Speed I/O Peripherals
- Static Memory Interfaces

The Battery Power Domain (BPD) is the lowest power domain of the XQ Zynq UltraScale+ MPSoC and RFSoC processing system. In this mode, all the PS is powered off except the Real-Time Clock (RTC) and battery-backed RAM (BBRAM).

Power Examples

Power for the XQ Zynq UltraScale+ MPSoCs and RFSoCs varies depending on the utilization of the PL resources, and the frequency of the PS and PL. To estimate power, use the Xilinx Power Estimator (XPE) at:

http://www.xilinx.com/products/design_tools/logic_design/xpe.htm

Platform Management Unit (PMU)

- Performs system initialization during boot
- Acts as a delegate to the application and real-time processors during sleep state
- Initiates power-up and restart after the wake-up request
- Maintains the system power state at all time
- Manages the sequence of low-level events required for power-up, power-down, reset, clock gating, and power gating of islands and domains
- Provides error management (error handling and reporting)
- Provides safety check functions (e.g., memory scrubbing)

The PMU includes the following blocks:

- Platform management processor
- Fixed ROM for boot-up of the device
- 128KB RAM with ECC for optional user/firmware code
- Local and global registers to manage power-down, power-up, reset, clock gating, and power gating requests
- Interrupt controller with 16 interrupts from other modules and the inter-processor communication interface (IPI)
- GPI and GPO interfaces to and from PS I/O and PL
- JTAG interface for PMU debug
- Optional User-Defined Firmware

Configuration Security Unit (CSU)

- Triple redundant Secure Processor Block (SPB) with built-in ECC
- Crypto Interface Block consisting of
  - 256-bit AES-GCM
  - SHA-3/384
  - 4096-bit RSA
- Key Management Unit
- Built-in DMA
- PCAP interface
- Supports ROM validation during pre-configuration stage
- Loads First Stage Boot Loader (FSBL) into OCM in either secure or non-secure boot modes
- Supports voltage, temperature, and frequency monitoring after configuration

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ devices is similar to the Kintex UltraScale and Virtex UltraScale devices but with the addition of a PMBus interface.

XQ Zynq UltraScale+ MPSoCs and RFSoCs contain one System Monitor in the PL and an additional block in the PS. The System Monitor in the PL has the same features as the block in UltraScale+ FPGAs. See Table 16.

Table 16: **Key System Monitor Features**

	XQ Zynq UltraScale+ PL	XQ Zynq UltraScale+ PS
ADC	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP, PMBus	APB

In FPGAs and the MPSoC and RFSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC and RFSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor inputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the PMU in the PS.

High-Speed and General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

PS External Interfaces

The XQ Zynq UltraScale+ MPSoC's external interfaces use dedicated pins that cannot be assigned as PL pins. These include:

- Clock, reset, boot mode, and voltage reference
- Up to 78 dedicated multiplexed I/O (MIO) pins, software-configurable to connect to any of the internal I/O peripherals and static memory controllers
- 32-bit or 64-bit DDR4/DDR3/DDR3L/LPDDR3 memories with optional ECC
- 32-bit LPDDR4 memory with optional ECC
- 4 channels (TX and RX pair) for transceivers

MIO Overview

The IOP peripherals communicate to external devices through a shared pool of up to 78 dedicated multiplexed I/O (MIO) pins. Each peripheral can be assigned one of several pre-defined groups of pins, enabling a flexible assignment of multiple devices simultaneously. Although 78 pins are not enough for simultaneous use of all the I/O peripherals, most IOP interface signals are available to the PL, allowing use of standard PL I/O pins when powered up and properly configured. Extended multiplexed I/O (EMIO) allows unmapped PS peripherals to access PL I/O.

Port mappings can appear in multiple locations. For example, there are up to 12 possible port mappings for CAN pins. The PS Configuration Wizard (PCW) tool aids in peripheral and static memory pin mapping. See Table 17.

Table 17: **MIO Peripheral Interface Mapping**

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 78 bits	Yes CAN: External PHY GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: • Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, *or* • Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

Transceiver (PS-GTR)

The four PS-GTR transceivers, which reside in the full power domain (FPD), support data rates of up to 6.0Gb/s. All the protocols cannot be pinned out at the same time. At any given time, four differential pairs can be pinned out using the transceivers. This is user programmable via the high-speed I/O multiplexer (HS-MIO).

- A Quad transceiver PS-GTR (TX/RX pair) able to support following standards simultaneously
  - x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
  - 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
  - 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
  - 1 or 2 USB3.0 channels at 5.0Gb/s
  - 1-4 Ethernet SGMII channels at 1.25Gb/s

- Provides flexible host-programmable multiplexing function for connecting the transceiver resources to the PS masters (DisplayPort, PCIe, Serial-ATA, USB3.0, and GigE).

HS-MIO

The function of the HS-MIO is to multiplex access from the high-speed PS peripheral to the differential pair on the PS-GTR transceiver as defined in the configuration registers. Up to 4 channels of the transceiver are available for use by the high-speed interfaces in the PS. See Table 18.

Table 18: **HS-MIO Peripheral Interface Mapping**

Peripheral Interface	Lane0	Lane1	Lane2	Lane3
PCIe (x1, x2 or x4)	PCIe0	PCIe1	PCIe2	PCIe3
SATA (1 or 2 channels)	SATA0	SATA1	SATA0	SATA1
DisplayPort (TX only)	DP1	DP0	DP1	DP0
USB0	USB0	USB0	USB0	–
USB1	–	–	–	USB1
SGMII0	SGMII0	–	–	–
SGMII1	–	SGMII1	–	–
SGMII2	–	–	SGMII2	–
SGMII3	–	–	–	SGMII3

GPIO

- Up to 128 GPIO bits
  - Up to 78-bits from MIO and 96-bits from EMIO
- Each GPIO bit can be dynamically programmed as input or output
- Independent reset values for each bit of all registers
- Interrupt request generation for each GPIO signals
- Single Channel (Bit) write capability for all control registers include data output register, direction control register, and interrupt clear register
- Read back in output mode

PCIe

- Compliant with the PCI Express Base Specification 2.1
- Fully compliant with PCI Express transaction ordering rules
- Lane width: x1, x2, or x4 at Gen1 or Gen2 rates
- 1 Virtual Channel
- Full duplex PCIe port
- Endpoint and single PCIe link Root Port
- Root Port supports Enhanced Configuration Access Mechanism (ECAM), Cfg Transaction generation
- Root Port support for INTx, and MSI

- Endpoint support for MSI or MSI-X
  - 1 physical function, no SR-IOV
  - No relaxed or ID ordering
  - Fully configurable BARs
  - INTx not recommended, but can be generated
  - Endpoint to support configurable target/slave apertures with address translation and Interrupt capability

SATA

- Compliant with SATA 3.1 Specification
- SATA host port supports up to 2 external devices
- Compliant with Advanced Host Controller Interface ('AHCI') ver. 1.3
- 1.5Gb/s, 3.0Gb/s, and 6.0Gb/s data rates
- Power management features: supports partial and slumber modes

Triple-Speed Gigabit Ethernet

The four tri-speed Ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

- Compatible with IEEE Std 802.3 and supports 10/100/1000Mb/s transfer rates (Full and Half duplex)
- Supports jumbo frames
- Built-in Scatter-Gather DMA capability
- Statistics counter registers for RMON/MIB
- Multiple I/O types (1.8, 2.5, 3.3V) on RGMII interface with external PHY
- GMII interface to PL to support interfaces as: TBI, SGMII, and RGMII v2.0 support
- Automatic pad and cyclic redundancy check (CRC) generation on transmitted frames
- Transmitter and Receive IP, TCP, and UDP checksum offload
- MDIO interface for physical layer management
- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Supports IEEE Std 1588 v2

CAN

- Conforms to the ISO 11898 -1, CAN2.0A, and CAN 2.0B standards
- Both standard (11-bit identifier) and extended (29-bit identifier) frames
- Bit rates up to 1Mb/s
- Transmit and Receive message FIFO with a depth of 64 messages
- Watermark interrupts for TXFIFO and RXFIFO
- Automatic re-transmission on errors or arbitration loss in normal mode
- Acceptance filtering of 4 acceptance filters
- Sleep Mode with automatic wake-up
- Snoop Mode
- 16-bit timestamping for receive messages
- Both internal generated reference clock and external reference clock input from MIO
- Guarantee clock sampling edge between 80 to 83% at 24MHz reference clock input
- Optional eFUSE disable per port

USB 3.0/2.0

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 Endpoints. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

USB 2.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Host, device and On-The-Go (OTG) modes
- High Speed, Full Speed, and Low Speed
- Up to 12 Endpoints
- 8-bit ULPI External PHY Interface
- The USB host controller registers and data structures are compliant to Intel xHCI specifications.
- 64-bit AXI master port with built-in DMA
- Power management features: hibernation mode

USB 3.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Up to 5.0Gb/s data rate
- Host and Device modes
  - Super Speed, High Speed, Full Speed, and Low Speed
  - Up to 12 Endpoints
  - The USB host controller registers and data structures are compliant to Intel xHCI specifications
  - 64-bit AXI master port with built-in DMA
  - Power management features: Hibernation mode

UART

- Programmable baud rate generator
- 6, 7, or 8 data bits
- 1, 1.5, or 2 stop bits
- Odd, even, space, mark, or no parity
- Parity, framing, and overrun error detection
- Line break generation and detection
- Automatic echo, local loopback, and remote loopback channel modes
- Modem control signals: CTS, RTS, DSR, DTR, RI, and DCD (from EMIO only)

SPI

- Full-duplex operation offers simultaneous receive and transmit
- 128B deep read and write FIFO
- Master or slave SPI mode
- Up to 3 chip select lines
- Multi-master environment
- Identifies an error condition if more than one master detected
- Selectable master clock reference
- Software can poll for status or be interrupt driven

I2C

- 128-bit buffer size
- Both normal (100kHz) and fast bus data rates (400kHz)
- Master or slave mode
- Normal or extended addressing
- I2C bus hold for slow host service

DisplayPort Controller

- 4K Display Processing with DisplayPort output
  - Maximum resolution of 4K x 2K-30 (30Hz pixel rate)
  - DisplayPort AUX channel, and Hot Plug Detect (HPD) on the output
  - RGB YCbCr, 4:2:0; 4:2:2, 4:4:4 with 6, 8, 10, and 12b/c
  - Y-only, xvYCC, RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2, and YCbCr 4:2:0 video format with 6,8,10 and 12-bits per color component
  - 256-color palette
  - Multiple frame buffer formats
  - 1, 2, 4, 8 bits per pixel (bpp) via a palette
  - 16, 24, 32bpp
  - Graphics formats such as RGBA8888, RGB555, etc.
- Accepts streaming video from the PL or dedicated DMA controller
- Enables Alpha blending of graphics and Chroma keying
- Audio support
  - A single stream carries up to 8 LPCM channels at 192kHz with 24-bit resolution
  - Supports compressed formats including DRA, Dolby MAT, and DTS HD
  - Multi-Stream Transport can extend the number of audio channels
  - Audio copy protection
  - 2-channel streaming or input from the PL
  - Multi-channel non-streaming audio from a memory audio frame buffer
- Includes a System Time Clock (STC) compliant with ISO/IEC 13818-1
- Boot-time display using minimum resources

Hardware and Software Debug Support

The debug system used in XQ Zynq UltraScale+ MPSoCs and RFSoCs is based on the Arm CoreSight architecture. It uses Arm CoreSight components including an embedded trace controller (ETC), an embedded trace Macrocell (ETM) for each Cortex-A53 and Cortex-R5F processor, and a system trace Macrocell (STM). This enables advanced debug features like event trace, debug breakpoints and triggers, cross-trigger, and debug bus dump to memory. The programmable logic can be debugged with the Xilinx Vivado Logic Analyzer.

Debug Ports

Three JTAG ports are available and can be chained together or used separately. When chained together, a single port is used for chip-level JTAG functions, Arm processor code downloads and run-time control operations, PL configuration, and PL debug with the Vivado Logic Analyzer. This enables tools such as the Xilinx Software Development Kit (SDK) and Vivado Logic Analyzer to share a single download cable from Xilinx.

When the JTAG chain is split, one port is used to directly access the Arm DAP interface. This CoreSight interface enables the use of Arm-compliant debug and software development tools such as Development Studio 5 (DS-5™). The other JTAG port can then be used by the Xilinx FPGA tools for access to the PL, including configuration bitstream downloads and PL debug with the Vivado Logic Analyzer. In this mode, users can download to and debug the PL in the same manner as a stand-alone FPGA.

GPU and VCU Details

Graphics Processing Unit (GPU)

XQ Zynq UltraScale+ MPSoCs include a GPU available in the devices designated with the EG suffix. The GPU is located in the PS and is designed to operate in conjunction with the APU.

- Supports OpenGL ES 1.1 & 2.0
- Supports OpenVG 1.1
- Operating target frequency: up to 667MHz
- Single Geometry Processor and two Pixel processor
- Pixel Fill Rate: 2 Mpixel/sec/MHz
- Triangle Rate: 0.11 Mtriangles/sec/MHz
- 64KB Level 2 Cache (read-only)
- 4X and 16X Anti-aliasing Support
- ETC1 texture compression to reduce external memory bandwidth
- Extensive texture format support
    - RGBA 8888, 565, 1556
    - Mono 8, 16

  - YUV format support
- Automatic load balancing across different graphics shader engines
- 2D and 3D graphic acceleration
- Up to 4K texture input and 4K render output resolutions
- Each geometry processor and pixel processor supports 4KB page MMU
- Power island gating on each GPU engine and shared cache
- Optional eFUSE disable

Video Encoder/Decoder (VCU)

XQ Zynq UltraScale+ MPSoCs include a Video codec (encoder/decoder) available in the devices designated with the EV suffix. The VCU is located in the PL and can be accessed from either the PL or PS.

- Simultaneous Encode and Decode through separate cores
- H.264 high profile level 5.2 (4Kx2K-60)
- H.265 (HEVC) main, main10 profile, level 5.1, high Tier, up to 4Kx2K-60 rate
- 8 and 10 bit encoding
- 4:2:0 and 4:2:2 chroma sampling
- 8Kx4K-15 rate
- Multi-stream up to total of 4Kx2K-60 rate
- Low Latency mode
- Can share the PS DRAM or use dedicated DRAM in the PL
- Clock/power management
- OpenMax Linux drivers

RF Data Converter and SD-FEC Details

RF Data Converter Subsystem

XQ Zynq UltraScale+ RFSoCs contain an RF data converter subsystem consisting of multiple RF-ADCs and RF-DACs.

RF-ADCs

12-bit RF-ADCs are arranged in tiles with each tile consisting of multiple RF-ADC instances. There are two types of RF-ADCs in XQ Zynq UltraScale+ RFSoCs. With the first type, used by most family members, an RF-ADC tile contains two 4.096GSPS converters. These converters can be configured individually for real input signals or as a pair for I/Q input signals. With the second type, used by the ZU29DR device, an RF-ADC tile contains four 2.058GSPS converters arranged in two pairs. Each of these converters can be

configured individually for real input signals or as a pair for I/Q input signals. The RF-ADC tile has one PLL and a clocking instance. Decimation filters in the RF-ADCs can operate at 1X (therefore acting as a bypass filter), 2X, 4X, or 8X at 80% of Nyquist bandwidth with 89dB stop-band attenuation. Each RF-ADC contains a 48-bit numerically controlled oscillator (NCO) and a dedicated high-speed, high-performance, differential input buffer with on-chip calibrated 100Ω termination.

RF-DACs

14-bit RF-DACs are arranged in tiles of four RF-DACs per tile. Each RF-DAC runs at a data rate up to 6.554GSPS. Each of these converters can be configured individually for real outputs or as a pair for I/Q output signal generation. The RF-DAC tile has one PLL and a clocking instance. Interpolation filters in the RF-DACs can operate at 1X (therefore acting as a bypass filter), 2X, 4X, or 8X at 80% of Nyquist bandwidth with 89dB stop-band attenuation. Each RF-DAC contains a 48-bit NCO.

Soft-Decision Forward Error Correction (SD-FEC)

Some members of the XQ Zynq UltraScale+ RFSoC family contain integrated SD-FEC blocks capable of encoding and decoding using LDPC codes and decoding using Turbo codes.

LDPC Decoding/Encoding

A range of quasi-cyclic codes can be configured over an AXI4-Lite interface. Code parameter memory can be shared across up to 128 codes. Codes can be selected on a block-by-block basis with the encoder able to reuse suitable decoder codes. The SD-FEC uses a normalized min-sum decoding algorithm with a normalization factor programmable from 0.0625 to 1 in increments of 0.0625. There can be between 1 and 63 iterations for each codeword. Early termination is specified for each codeword to be none, one, or both of the following:

- Parity check passes
- No change in hard information or parity bits since last operation

Soft or hard outputs are specified for each codeword to include information and optional parity with 6-bit soft log-likelihood ratio (LLR) on inputs and 8-bit LLR on outputs.

Turbo Decoding

In Turbo mode, the SD-FEC can use the Max, Max Scale, or Max Star algorithms. When using the Max Scale algorithm, the scale factor is programmable from 0.0625 to 1 in increments of 0.0625. There can be between 1 and 63 iterations for each codeword, specified using the AXI4-Stream control interface. Early termination is specified for each codeword to be none, one, or both of the following:

- CRC passes
- No change in hard decision since last iteration

Soft or hard outputs are specified for each codeword to include systematic and optionally parity 0 and parity 1 with 8-bit soft LLR on inputs and outputs.

Configuration

The UltraScale architecture-based devices support secure and non-secure processing system boot and programmable logic configuration with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms.

UltraScale architecture-based devices store their customized programmable logic configuration in SRAM-type internal latches. The programmable logic configuration is volatile and must be reloaded whenever the device is powered up. Several methods determined by the mode pins and data formats are available for loading configuration.

Flexible reprogrammability with support for secure configuration, affords designers the ability to satisfy initial design and time-to-market objectives while simultaneously allowing a roadmap for feature upgrades of fielded systems. UltraScale architecture-based devices can additionally support multiple configurations during device operation through dynamic partial reconfiguration.

Booting MPSoCs and RFSoCs

XQ Zynq UltraScale+ MPSoCs and RFSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5F, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

After copying the FSBL to OCM, the processor executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL) such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or executable after boot.

See UG1085, *Zynq UltraScale+ Device Technical Reference Manual*, for more details about Zynq UltraScale+ MPSoC and RFSoC processing system boot and programmable logic configuration.

Configuring FPGAs

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

See UG570, *UltraScale Architecture Configuration User Guide*, for more details about configuring UltraScale architecture FPGAs.

Packaging

Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 19 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 19: **UltraScale and UltraScale+ 3D IC SLR Count and Dimensions**

	Kintex UltraScale	Virtex UltraScale+	
Device	KU115	VU7P	VU11P
# SLRs	2	2	3
SLR Width (in regions)	6	6	8
SLR Height (in regions)	5	5	4

The UltraScale devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale+ devices in the B2104 packages are compatible with Kintex UltraScale devices in the B2104 packages. All valid XQ ruggedized device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to UG583, *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

XQ Package Support in Vivado Design Suite

The XQ ruggedized devices are supported in the Vivado Design Suite with XQ part and package options. Users should select the correct XQ device and speed-grade option when designing for these devices.

XQ UltraScale+ devices are additionally available in non-ruggedized packages. Non-ruggedized package construction adds Sn/Pb lead balls on the exterior as well as the XQ anti-counterfeit marking, but the package is otherwise the same as the equivalent commercial-grade (XC) device. This option is not a ruggedized package, and it is not offered in extended temperature range nor with the qualifications of an XQ ruggedized offering. This variant of XQ device is supported in the Vivado tools by selecting the XC equivalent device part number. All package and speed-file parameters are equivalent to the XC offering. The XQ variant is available for all equivalent XC devices with industrial temperature range support and speed-grades. These device variants are supported by Xilinx for applications that do not require other features of the full XQ ruggedized device, to allow the end-user an option instead of re-balling XC devices, which voids the Xilinx device warranty. See ordering information for package ordering codes. Consult sales for further information about the non-ruggedized XQ devices.

Ordering Information

Table 20 shows the speed and temperature grades available in the different device families. V_{CCINT} supply voltage is listed in parentheses.

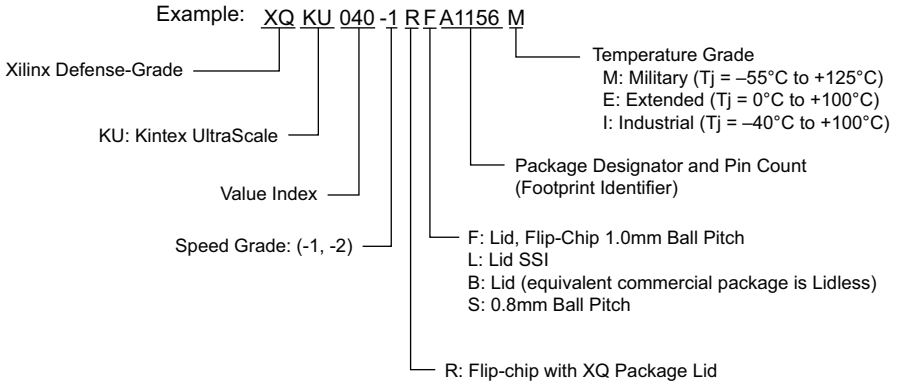
Table 20: **Speed Grade and Temperature Grade**

Device Family	XQ Devices	Speed Grade and Temperature Grade			
		Military (M)	Industrial (I)	Extended E	
		–55°C to +125°C	–40°C to +100°C	0°C to +100°C	0°C to +110°C
XQ Kintex UltraScale	XQKU040 XQKU060 XQKU095		-2I (0.95V)	-2E (0.95V)	
		-1M (0.95V)	-1I (0.95V)		
	XQKU115		-2I (0.95V)	-2E (0.95V)	
			-1I (0.95V)		
XQ Kintex UltraScale+	XQKU5P XQKU15P		-2I (0.85V)		
		-1M (0.85V)	-1I (0.85V)		
			-1LI (0.85V or 0.72V)		
XQ Virtex UltraScale+	XQVU3P		-2I (0.85V)		-2LE (0.85V or 0.72V)
		-1M (0.85V)	-1I (0.85V)		
	XQVU7P XQVU11P		-2I (0.85V)		-2LE (0.85V or 0.72V)
			-1I (0.85V)		
XQ Zynq UltraScale+	EG EV DR(1)		-2I (0.85V)		
		-1M (0.85V)	-1I (0.85V)		
			-1LI (0.85V or 0.72V)		

Notes:

1. -2LI (0.85V or 0.72V) available on the XQZU48DR and XQZU49DR.

The ordering information shown in Figure 3 applies to all packages in the XQ Kintex UltraScale FPGAs. Refer to the Package Marking section of UG575, *UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide* for a more detailed explanation of the device markings.



1) All XQ package have eutectic tin lead solder balls and internal solder contents are > 3%.
2) See UG575: *Kintex UltraScale and Virtex UltraScale FPGAs Packaging and Pinouts User Guide* for more information.
3) All packages other than RS are flip-chip with 1.0mm ball pitch

DS895_03_102418

Figure 3: **XQ Kintex UltraScale FPGA Ordering Information**

The ordering information shown in Figure 4 applies to all packages in the XQ Kintex UltraScale+ and XQ Virtex UltraScale+ FPGAs, and Figure 5 applies to XQ Zynq UltraScale+ MPSoCs and RFSoCs.

The -1L and -2L speed grades in the UltraScale+ families can run at one of two different V_{CCINT} operating voltages.

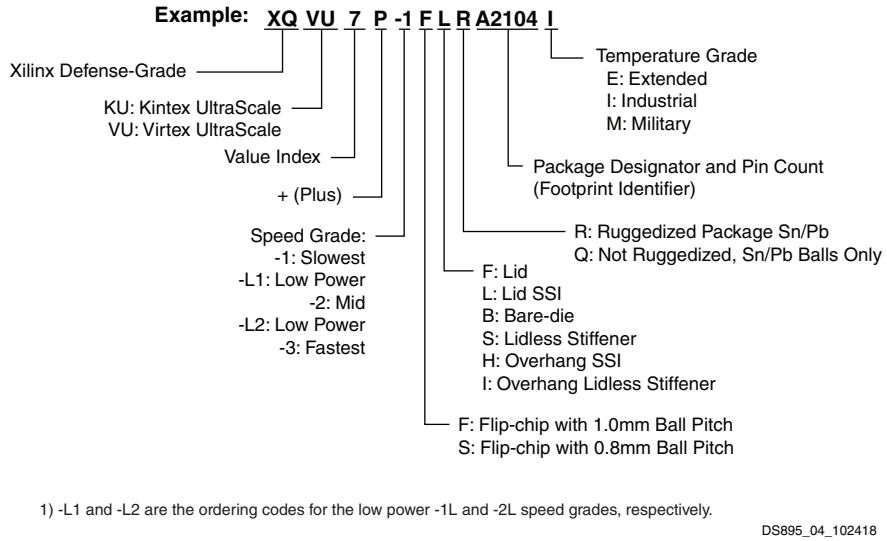


Figure 4: **XQ UltraScale+ FPGA Ordering Information**

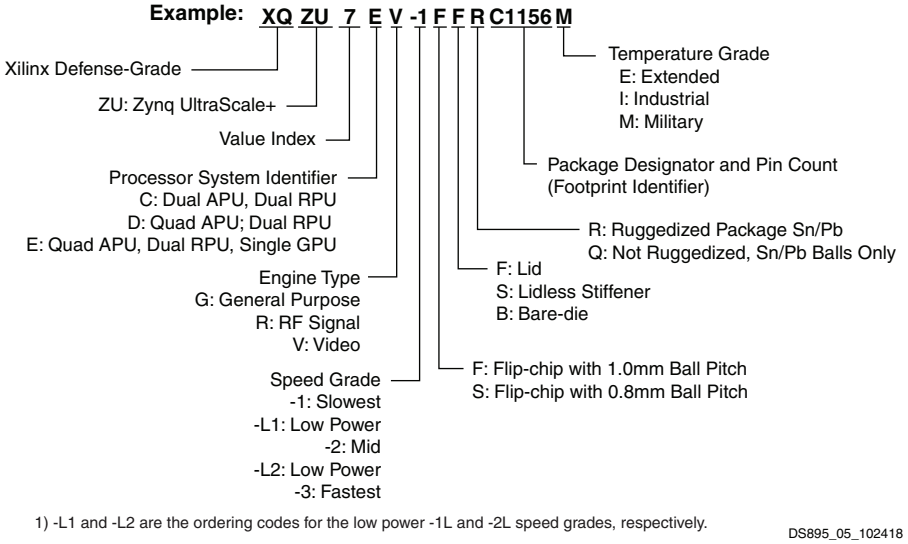


Figure 5: **XQ Zynq UltraScale+ MPSoC and RFSoC Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/09/2021	2.1	Added XQZU48DR and XQZU49DR. Updated XQ Zynq UltraScale+ RFSoCs, Table 11, Table 12, and Table 20 (added note about -2LI availability in DR devices).
11/15/2018	2.0	Added XQ Kintex UltraScale+, XQ Virtex UltraScale+, XQ Zynq UltraScale+ MPSoC, and XQ Zynq UltraScale+ RFSoC information throughout document.
01/31/2017	1.0	Initial Xilinx release.

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