SiGe Power Amplifier for GSM 900

Description

The TST0912 is a monolithic integrated power amplifier IC. The device is manufactured using Atmel Wireless & Microcontrollers' Silicon-Germanium (SiGe) technology and has been designed for use in GSM 900-MHz mobile phones.

With a single supply voltage operation of 3 V and a neglectable leakage current in power-down mode, the TST0912 needs few external components and reduces system costs.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- 35 dBm output power
- Power-added efficiency (PAE) 50%
- Single supply operation at 3 V
  no negative voltage necessary
- Current consumption in power-down mode ≤ 10 µA,
  no external power-supply switch required
- Power-ramp control
- Simple input and output matching
- Simple output matching for maximum flexibility
- SMD package (PSSOP16 with heat slug)

Block Diagram

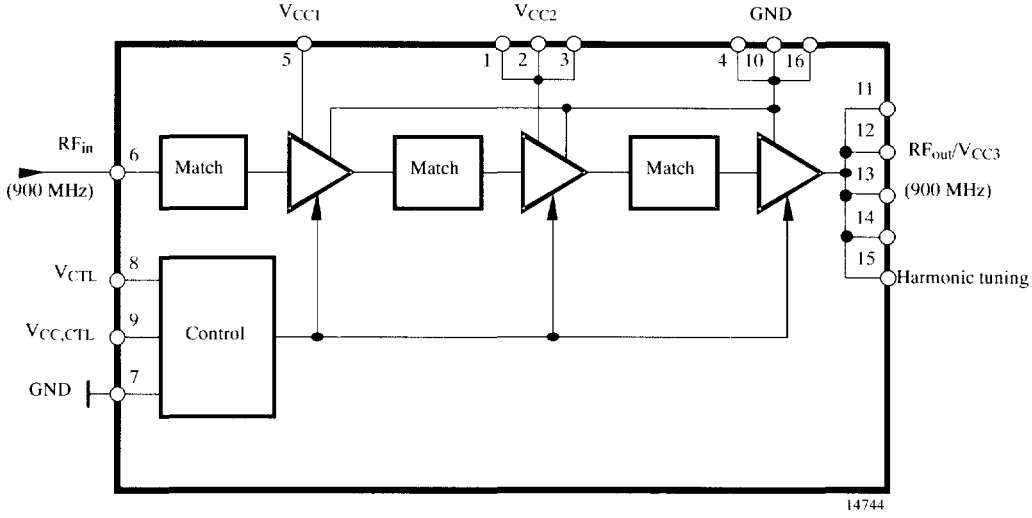

Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
TST0912-TJS	PSSO16	Tube
TST0912-TJQ	PSSO16	Taped and reeled

Preliminary Information

Pin Description

Pin	Symbol	Function
1	V_{CC2}	Supply voltage 2
2	V_{CC2}	Supply voltage 2
3	V_{CC2}	Supply voltage 2
4	GND	Ground
5	V_{CC1}	Supply voltage 1
6	RF_{in}	RF input
7	GND	Ground (control)
8	V_{CTL}	Control input
9	$V_{CC,CTL}$	Supply voltage for control
10	GND	Ground (optional)
11	RF_{out}/V_{CC3}	RF output / supply voltage 3
12	RF_{out}/V_{CC3}	RF output / supply voltage 3
13	RF_{out}/V_{CC3}	RF output / supply voltage 3
14	RF_{out}/V_{CC3}	RF output / supply voltage 3
15	RF_{out}/V_{CC3}	RF output / harmonic tuning
16	GND	Ground

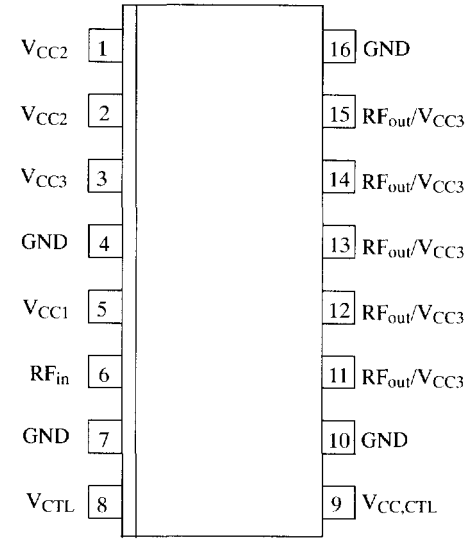

Figure 2. Pinning

Absolute Maximum Ratings

All voltages refer to GND

Parameter		Symbol	Min.	Max.	Unit
Supply voltage V_{CC}	Pin 5 Pins 1, 2 and 3 Pins 11, 12, 13 and 14 Pin 9	V_{CC1} V_{CC2} V_{CC3} $V_{CC, CTL}$		5.0	V
Input power	Pin 6	P_{in}		12	dBm
Gain control voltage	Pin 8	V_{CTL}	0	2.2	V
Duty cycle for operation				25	%
Burst duration		t_{burst}		1.2	ms
Junction temperature		T_j		+150	°C
Storage temperature		T_{stg}	- 40	+150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	t.b.d.	K/W

Operating Range

All voltages refer to GND

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_{CC}	V_{CC1}, V_{CC2}, V_{CC3}, $V_{CC, CTL}$	2.4	3.5	4.5	V
Ambient temperature	T_{amb}	- 25		+ 85	°C
Input frequency	f_{in}		900		MHz

Electrical Characteristics

Test conditions: $V_{CC} = V_{CC1}$ to V_{CC3}, $V_{CC, CTL}$ = 3.5 V, V_{CTL} = 1.5 V, T_{amb} = + 25°C, t_{burst} = 0.577 ms, t_{period} = 4.615 ms (see application circuit)

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Supply voltage		V_{CC}	2.4	3.5	4.5	V
Current consumption	Active mode P_{out} = 34.5 dBm, PAE = 50%	I		1.7		A
Current consumption (leakage current)	Power-down mode $V_{CTL} \leq 0.2$ V	I			10	µA
RF input						
Frequency range		f_{in}	880	900	915	MHz
Input impedance *)		Z_i		50		Ω
Input power		P_{in}		3	12	dBm
Input VSWR *)	P_{in} = 0 to 12 dBm, P_{out} = 34.5 dBm	VSWR			2 : 1	
RF output						
Output impedance *)		Z_o		50		Ω
Output power	P_{in} = 3 dBm, $R_L = R_G$ = 50 Ω V_{CC} = 3.5 V, T_{amb} = +25°C V_{CC} = 2.7 V, T_{amb} = +85°C	P_{out}	34.3 32.0	34.8 33.0		dBm dBm
Minimum output power	V_{CTL} = 0.3 V			- 20		dBm
Power-added efficiency	V_{CC} = 3 V, P_{out} = 28 dBm V_{CC} = 3 V, P_{out} = 30 dBm V_{CC} = 3 V, P_{out} = 33.5 dBm	PAE	25 35 50			%
Stability	T_{amb} = -25 to + 85 °C no spurious ≥ -60 dBc	VSWR			10 : 1	
Load mismatch (stable, no demage)	P_{out} = 34.5 dBm, all phases	VSWR			10 : 1	
Second harmonic distortion		2fo			-35	dBc
Third harmonic distortion		3fo			-35	dBc
Noise power	P_{out} = 34 dBm, RBW = 100 kHz f = 925 to 935 MHz f ≥ 935 MHz			- 73 - 85	- 70 - 82	dBm dBm

Preliminary Information

Electrical Characteristics (continued)

Test conditions: $V_{CC} = V_{CC1}$ to V_{CC3}, $V_{CC, CTL}$ = 3.5 V, V_{CTL} = 1.5 V, T_{amb} = + 25°C, t_{burst} = 0.577 ms, t_{period} = 4.615 ms (see application circuit)

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Rise and fall time		t_r, t_f			0.5	µs
Isolation between input and output	P_{in} = 0 to 10 dBm, $V_{CTL} \leq$ 0.2 V (power down)		50			dB
Power control						
Control curve slope	$P_{out} \geq$ 25 dBm				150	dB/ V
Power-control range	V_{CTRL} = 0.3 to 2.0 V		50			dB
Control-voltage range		V_{CTL}	0.3		2.0	V
Control current	P_{in} = 0 to 10 dBm, V_{CTL} = 0 to 2.0 V	I_{CTL}			200	µA

*) with external matching (see application circuit)

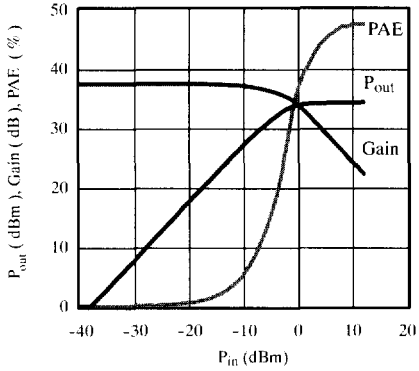

Figure 3. Gain, P_{out} and PAE versus P_{in}

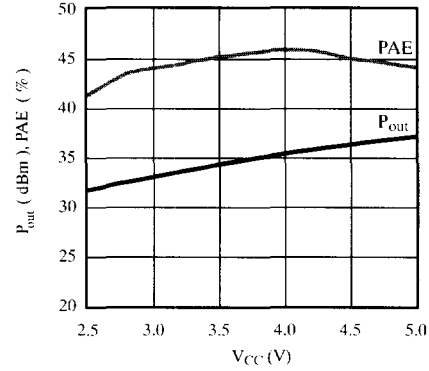

Figure 5. P_{out}, PAE versus V_{CC}

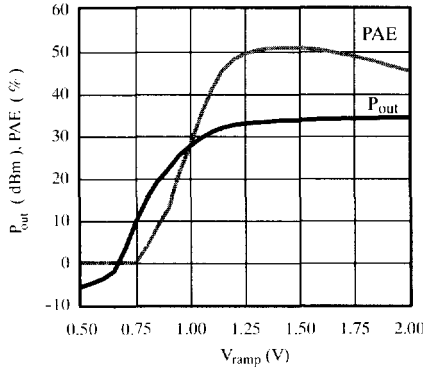

Figure 4. P_{out}, PAE versus V_{ramp}

Remarks for the Application Circuit

All components Tx are microstrip lines:
FR4, epsilon(r) = 4.3, metal: Cu 3.5 µm;
distance: 1. layer to RF ground = 0.5 mm

Name	l mm	w mm	Name	l mm	w mm
T1	20.5	1.0	T5	2.5	1.0
T2	1.3	1.0	T6	43.1	0.5
T3	14.8	0.5	T7	6.0	1.25
T4	14.2	0.5	T8	10.0	0.5

Application Circuit

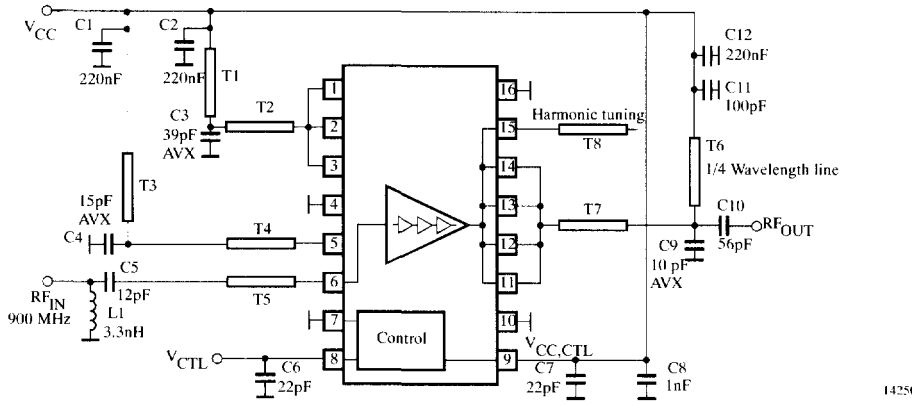

Figure 6.

Package Information