MICRONAS

April 1993

MAS7534

µP-Compatible 14-bit DAC

GENERAL DESCRIPTION

The MAS 7534 is a 14-bit monolithic CMOS multiplying D/A converter where excellent linearity is achieved without the use of laser trimming.

The device is configured to accept right-justified data in two bytes from an 8-bit data bus. Standard chip select and memory write logic is used to access the DAC. Address lines A0 and A1 control internal register loading and transfer.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external schottky diodes on the use of FET input op.amp. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

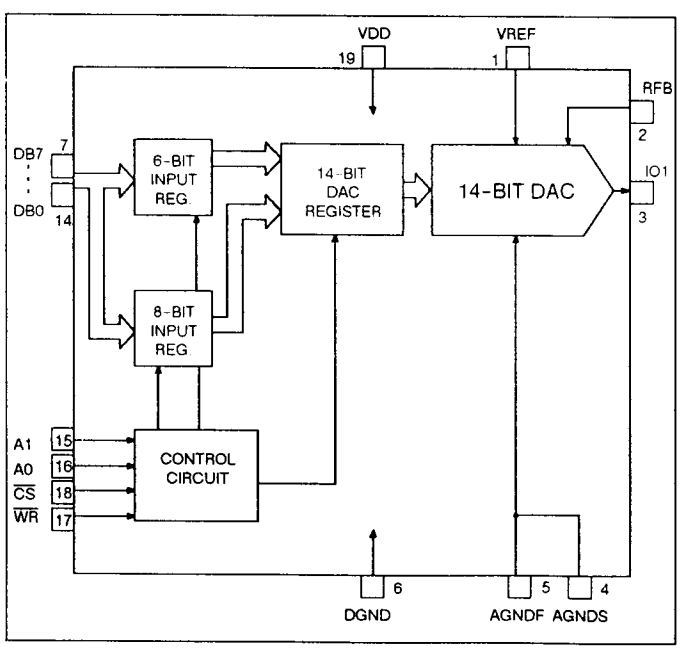
FEATURES

- 3-bit Monotonic Over Full Temperature Range
- No Laser Trimming
- Monolithic CMOS Construction
- Double-Buffered Digital Inputs
- High Stability
- All 16.384 Codes Tested
- Direct Replacement for AD7534
- 20-pin DIP Package

APPLICATION

- Digital Audio
- µP Based Control Systems
- Automatic Test Equipment
- Precision Servo Control

BLOCK DIAGRAM



PRODUCT INFORMATION

	Relative Accuracy	Gain Error	Temperature Range and Package
			Commercial
	Tmin-Tmax	Tmin-Tmax	0°C to +70°C
MAS7534N	±2 LSB	±16 LSB	20 Pin PDIP

ELECTRICAL CHARACTERISTICS

VDD = + 15V, VREF = 10V, IO1 = AGNDF = AGNDS = DGND = 0V, Unipolar unless otherwise specified

		Ta = + 25 °C			Tmin-Tmax		
Parameter	Symbol	MIN	TYP	MAX	Limits	Units	Test Conditions/Comments
STATIC PERFORMANCE Resolution Integral Nonlinearity[1] Differential Nonlinearity[2] Gain error Output Leakage Current Ilkg at IO1 (pin 3)	 N INL DNL GFE 	 14 	 	 ± 2 ± 1 ± 16 ± 5	 14 ± 2 ± 1 ± 16 ± 10	 Bits LSB LSB LSB nA	 Relative Accuracy 12 bit Monotonic to 14 bits Measured Using Internal Rfb DAC Register Loaded With All 1s All Digital Inputs = 0V
TEMPERATURE STABILITY Gain error TC[3]	TCGFE		± 0.5	± 2.0	± 2.0	ppm/°C	
REFERENCE INPUT Input Resistance	Rref	3.5	5	6.5		kΩ	
DIGITAL INPUTS Input High Voltage Input Low Voltage Input Current[4] Input Capacitance[3]	 VIH VIL Iin Cin	 2.4 -0.3 	 	 VDD 0.8 ± 1 7	 2.4 0.8 ± 10 7	 V V µA pF	Unipolar Coding: Binary Bipolar Coding: Offset Binary
SWITCHING CHARACTERISTICS Address Valid to Write Setup Time Address Valid to Write Hold Time Data Setup Time Data Hold Time Chip Select to Write Setup Time Chip Select to Write Hold Time Write Pulse Width	 t1 t2 t3 t4 t5 t6 t7	 0 0 140 20 0 0 170	 	 	 0 0 160 20 0 0 200	 ns ns ns ns ns ns 	See Timing Diagram
POWER SUPPLY VDD Range Supply Current	 VDD IDD IDD	 11.4 	 15 	 15.75 3.0 0.5	 3.0 0.5	 V mA mA	 All Dig. Inputs VIL or VIH All Dig. Inputs 0V or 5V to VDD
TEMPERATURE RANGE		0		+ 70		°C	

NOTES:
1. Integral Nonlinearity is measured as the arithemetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any given input combination.
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3. Guaranteed by design but not production tested.
4. Logic inputs are MOS gates. Iin typical is less than 1 nA at 25 °C.

AC PERFORMANCE CHARACTERISTICS

These Characteristics are included for design guidance only and are subject to sample testing only.
VDD = + 15V, VREF = 10V, IO1 = AGNDF = AGNDS = DGND = 0V except where stated.

		Ta = +25°C			Tmin-Tmax		
Parameter	Symbol	MIN	TYP	MAX	Limits	Units	Test Conditions/Comments
CURRENT SETTLING TIME Full Scale Transition	ts		0.8	1.5		us	Settling ti 0.003% F.S.R Iout load = 100 Ohm, Cext = 13 p DAC register alternately loaded all 1's and all 0's.
OUTPUT CAPACITANCE CIO1 (Pin 3) CIO1 (Pin 3)	Co		150 75	260 130	260 130	pF pF	DAC register loaded with all 1's DAC register loaded with all 0's
DIGITAL TO ANALOG GLITCH ENERGY	Q		100			nVs	VREF = 0V; DAC register alternatel loaded with all 0's and all 1's Iout load = 100 Ohm, Cext = 13 p
MULTIPLYING FEEDTHROUGH ERROR AT IO1	FT IO1		3.0		5.0	mVpp	VREF = 20Vpp; f = 10kHz sine wave DAC register loaded with all 0's
POWER SUPPLY REJECTION RATIO	PSRR		±0.002	±0.01	±0.02	%/%	VDD = 14-16V

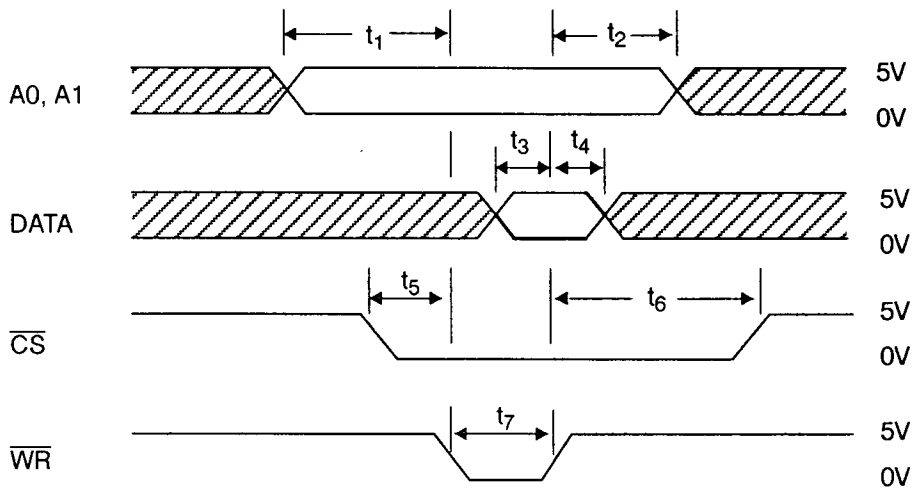
ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

VDD to GND	-0.3V, +17V
Digital Input Voltage to GND	-0.3V, VDD +0.3V
VREF or VRFB to GND	+/-25V
Output Voltage (Pin 3)	-0.3V, VDD + 0.3V
Power Dissipation (Any Package) to +75°C	450 mW
Derates above 75°C by	6 mW/°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 secs)	+300°C

CAUTION:
1. Do not apply voltages higher than VDD or less than GND potential on any terminal other than VREF or RFB.
2. The digital inputs are diode clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

MAS7534 TIMING DIAGRAM

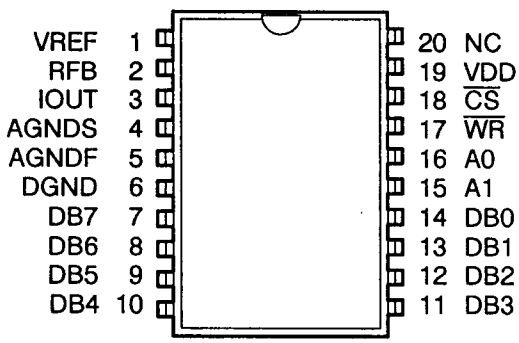


NOTES: 1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_r = t_f = 20$ ns.
2. Timing measurement reference level is $\frac{Vih + Vil}{2}$

$\overline{WR}$	$\overline{CS}$	A1	A0	Function
X[1]	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus[2]
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Register

NOTES : 1. X = Don't Care
2. When $A_1 = 0$, $A_0 = 0$ all DAC registers are transparent, so by placing all 0s or 1s on the data inputs the user can load the DAC to zero or full-scale output in one write operation. This facility simplifieis system calibration.

PIN CONFIGURATION



PIN DESCRIPTION

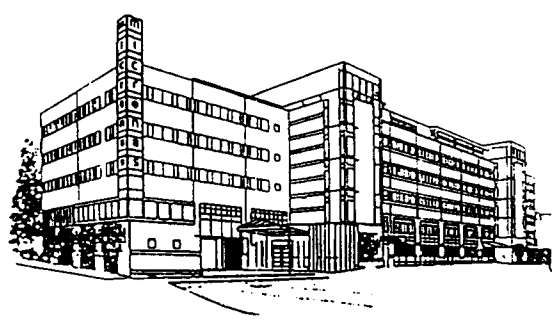
Pin name	Pin No.	I/O	Function
VREF	1	I	Reference Voltage Input
RFB	2	I	Feedback Resistor
IO1	3	O	Current Output
AGNDS	4	G	Analog ground sense line. Reference point for external circuitry. This pin should
			carry minimal current.
AGNDF	5	G	Analog ground force line; carries current from internal analog ground connec-
			tions. AGNDF and AGNDS are tied together internally.
DGND	6	G	Digital Ground
DB7	7	I	Data BIT7
DB6	8	I	Data BIT6
DB5	9	I	Data BIT5 or Data BIT 13 (DAC MSB)
DB4	10	I	Data BIT4 or Data BIT12
DB3	11	I	Data BIT3 or Data BIT 11
DB2	12	I	Data BIT2 or Data BIT10
DB1	13	I	Data BIT1 or Data BIT9
DB0	14	I	Data BIT0 or Data BIT8
A1	15	I	Address line 1
A0	16	I	Address line 0
$\overline{WR}$	17	I	Write, Active Low
$\overline{CS}$	18	I	Chip Selection, Active Low
VDD	19	P	Positive Power Supply
NC	20		No Connection

ORDERING INFORMATION

Product code	Product	Package	Comments
MAS7534N	µP-Compatible 14-bit DAC	20 Pin PDIP	

LOCAL DISTRIBUTOR

FACTORY CONTACT INFORMATION



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