

MN74HC161/MN74HC161S

Synchronous Binary Counter with Asynchronous Clear

■ Outline

The MN74HC161/MN74HC161S is a presettable synchronous binary (hexadecimal) counter. It has adopted the internal carry look ahead system so that it can also serve as a high speed counter. The output of every flip-flop changes at the rising edge of the clock input.

The counter output can be optionally preset into either the "H" level or the "L" level by using the load input because this counter is entirely programmable. The four flip-flops are preset synchronously with the rising edge of the clock input. When the level of the load input is "L", the counter stops its function, and data corresponding to the input data to be set with the next clock pulse appears on the output irrespectively of the enable input level. The counter does not function even if the level of the load input becomes "H" before detection of the rising edge of the clock input. The clear function is asynchronous, and when the level of the clear input is "L", it remains valid irrespectively of the level of the clock input, load input, or enable input. The carry look ahead circuit is used for cascade connection of the n-bit synchronous counter without any additional parts. It is the two active "High" enable inputs (ENP, ENT) and the ripple carry (RC) output that fulfill this function. When the levels of the enable inputs ENP and ENT are both "H", the counting function remains valid. The width of the ripple carry output is almost the same as of the "H" level of the output Q_A . The overflow ripple carry pulse of the "H" level can sequentially enable each stage connected with the cascade.

Owing to the silicon gate CMOS process, this counter has realized low power consumption high noise immunity and the operation speed as high as of an LS TTL. To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the V_{CC} and the GND. The pin assignment and the function are the same as those of the standard 54LS/74LS logic family.

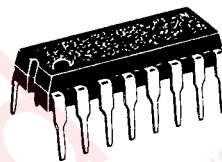
■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
×	L	×	×	×	Clear
×	H	H	L	H	Count & RC disabled
×	H	L	H	H	Count disabled
×	H	L	L	H	Count & RC disabled
↗	H	×	×	L	Load
↗	H	H	H	H	Increment Counter

Note) 1. ↗ : In leading of clock from "L" to "H" increment count is performed.
When load is "L" input data are loaded.

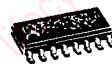
2. × : "H" or "L" either will do.

P-3



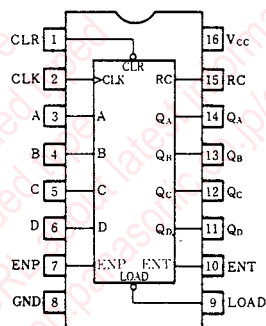
16-pin plastic DIL package

P-4

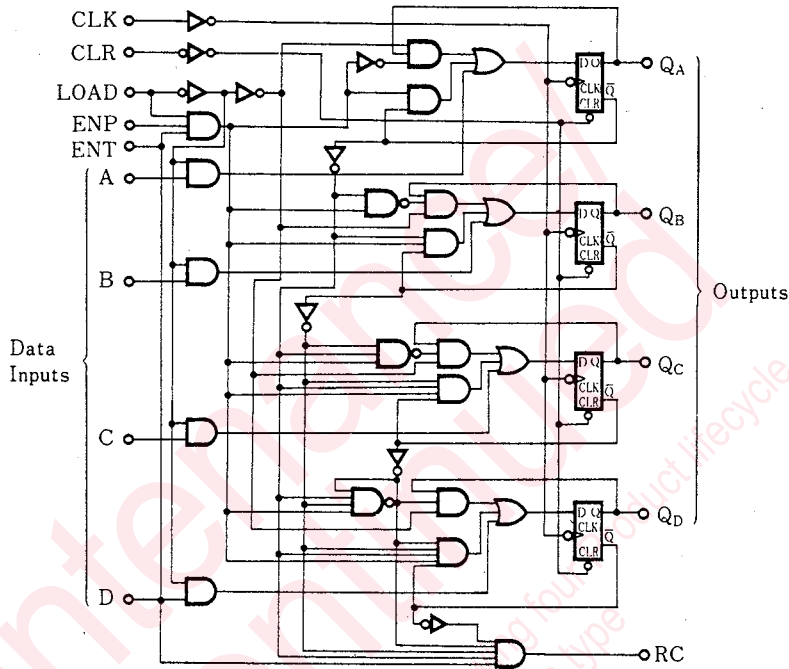


16-pin PANAFLAT package (SO-16D)

Pin Configuration



■ Logic Diagram



■ Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	-0.5~+7.0	V
Input output voltage		V_I, V_O	-0.5~ $V_{CC}+0.5$	V
Input protective diode current		I_{IK}	±20	mA
Output parasitic diode current		I_{OK}	±20	mA
Output current		I_O	±25	mA
Supply current		I_{CC}, I_{GND}	±50	mA
Storage temperature		T_{strg}	-65~+150	°C
Power dissipation	MN74HC161	$T_a = -40 \sim +60^\circ\text{C}$	400	mW
		$T_a = +60 \sim +85^\circ\text{C}$		
	MN74HC161S	$T_a = -40 \sim +60^\circ\text{C}$	275	mW
		$T_a = +60 \sim +85^\circ\text{C}$		

■ Recommended Operating Conditions

Item	Symbol	$V_{CC}(V)$	Rating	Unit
Operating power supply voltage	V_{CC}		1.4~6.0	V
Input output voltage	V_I, V_O		0~ V_{CC}	V
Operating temperature	T_A		-40~+85	°C
Input rise, fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Item	Symbol	V _{CC} (V)	Test Condition			Temperature					Unit
			V _I	V _O	Unit	T _a =25°C			T _a =-40~+85°C		
						min.	typ.	max.	min.	max.	
Input voltage high level	V _{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V _{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V _{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V _{IL}	-4.0	mA	3.92			3.84		
		6.0		-5.2	mA	5.48			5.34		
Output voltage low level	V _{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V _{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V _{IL}	4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I _I	6.0	V _I =V _{CC} or GND					±0.1		±1.0	μA
Static supply current	I _{CC}	6.0	V _I =V _{CC} or GND, I _O =0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤ 6ns, C_L=50pF)

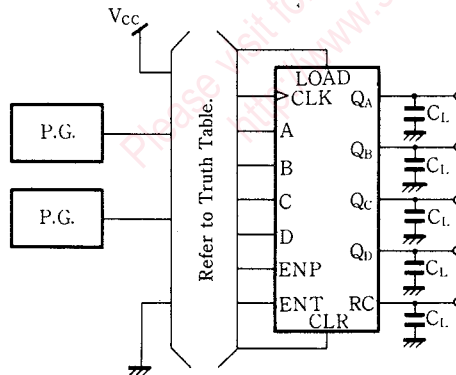
Item	Symbol	V _{CC} (V)	Test Condition	Temperature					Unit	
				T _a =25°C			T _a =-40~+85°C			
				min.	typ.	max.	min.	max.		
Output rise time	t _{TLH}	2.0				25	75		95	ns
		4.5				8	15		19	
		6.0				7	13		16	
Output fall time	t _{THL}	2.0				19	75		95	ns
		4.5				5	15		19	
		6.0				3	13		16	
Propagation time CLK→Q _A ~Q _D (L→H)	t _{PLH}	2.0				42	150		190	ns
		4.5				17	30		38	
		6.0				14	26		33	
Propagation time CLK→Q _A ~Q _D (H→L)	t _{PHL}	2.0				42	150		190	ns
		4.5				17	30		38	
		6.0				14	26		33	
Propagation time CLK→RC (L→H)	t _{PLH}	2.0				40	175		220	ns
		4.5				17	35		44	
		6.0				15	30		37	
Propagation time CLK→RC (H→L)	t _{PHL}	2.0				37	175		220	ns
		4.5				17	35		44	
		6.0				14	30		37	

■ AC Characteristics (cont.)

Item	Symbol	V _{CC} (V)	Test Condition	Temperature					Unit
				Ta=25°C			Ta=-40~+85°C		
				min.	typ.	max.	min.	max.	
Propagation time ENNT→RC (L→H)	t _{PLH}	2.0			29	100		125	ns
		4.5			12	20		25	
		6.0			10	17		21	
Propagation time ENT→RC (H→L)	t _{PHL}	2.0			33	125		155	ns
		4.5			14	25		31	
		6.0			12	21		26	
Propagation time CLR→Q _A ~Q _D (H→L)	t _{PHL}	2.0			35	150		190	ns
		4.5			15	30		38	
		6.0			12	26		33	
Propagation time CLR→RC (H→L)	t _{PHL}	2.0			30	175		220	ns
		4.5			14	35		44	
		6.0			12	30		37	
Minimum set-up time LOAD	t _{su}	2.0			39	100		125	ns
		4.5			13	20		25	
		6.0			10	17		21	
Minimum set-up time A, B, C, D	t _{su}	2.0			18	100		125	ns
		4.5			5	20		25	
		6.0			4	17		21	
Minimum hold time	t _h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width CLR	t _w	2.0			13	100		125	ns
		4.5			8	20		25	
		6.0			6	17		21	
Minimum recovery time	t _{rem}	2.0			13	75		95	ns
		4.5			4	15		19	
		6.0			3	13		16	
Maximum clock frequency	f _{max}	2.0			6	27		4	MHz
		4.5			28	40		22	
		6.0			33	54		26	

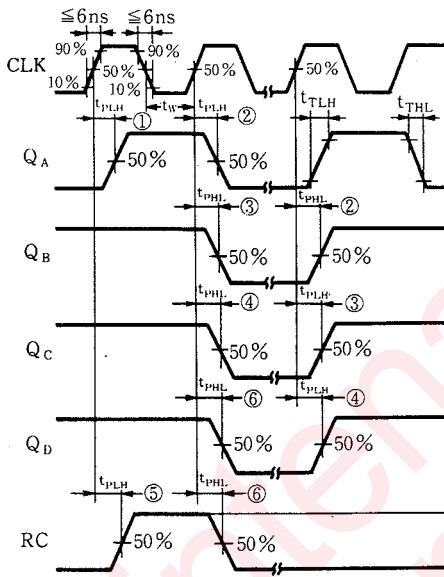
• Switching time measuring circuit and waveforms

1. Measuring circuit

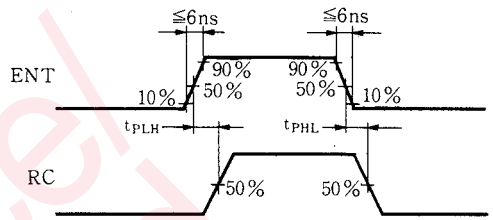


2. Switching waveforms

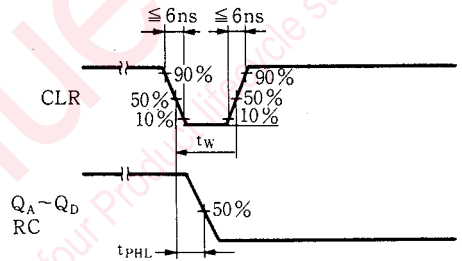
1 t_{PLH} , t_{PHL} (CLK → Q_A~Q_D, RC)



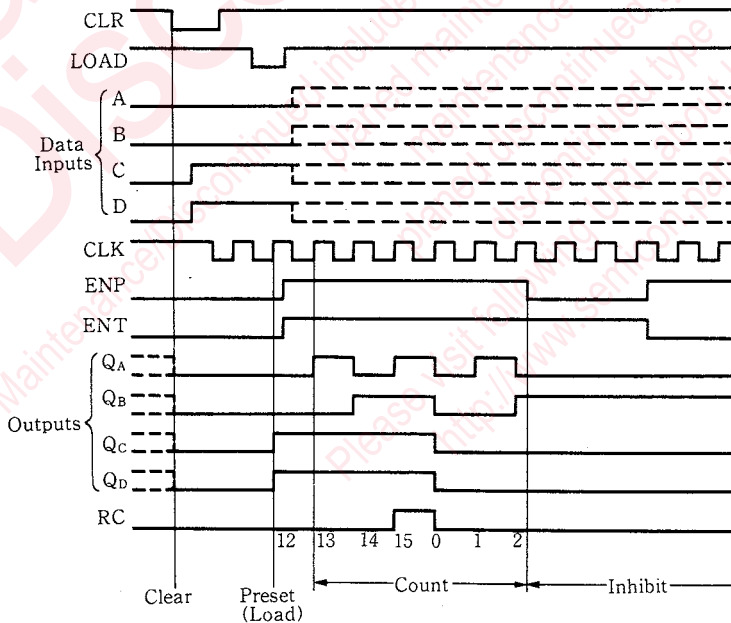
2 t_{PLH} , t_{PHL} (ENT → RC)



(3) t_{PHL} (CLR → Q_A~Q_D, RC)



■ Typical Operating Condition



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