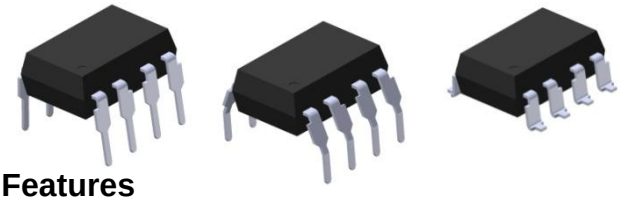
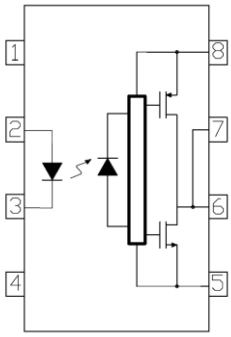
DATASHEET

8PIN DIP IGBT/MOSFET
1.0A Output Current GATE DRIVER PHOTOCOUPLER
EL3150



Schematic



Pin Configuration

1, NC
2, Anode
3, Cathode
4, NC
5, V_{EE}
6, V_{O2}
7, V_{O1}
8, V_{CC}

Features

- Guaranteed performance from -40 to 100℃
- Peak Output Current : I_{OP} = ±1.0A (max)
- Threshold Input Current: I_{FLH} = 5 mA (max)
- Common mode transient immunity : ±15kV/μ s （min）
- High isolation voltage between input and output (Viso=5000 V rms)
- Pb free and RoHS compliant.
- **c**UL approved (E214129)
- VDE approved (40028391)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved

Description

The EL3150 consists of an infrared light emitting diodes and integrated high gain, high-speed photo detectors. The device is housed in a 8 pin DIP package.

The photo detector has an internal shield that provides a guaranteed common-mode transient immunity of ±15 kV/μs. It is suitable for direct gate driving circuit for IGBTs or power MOSFETs

Applications

- Isolated IGBT/Power MOSFET gate drive
- Industrial Inverter
- AC brushless and DC motor drives
- Inverter for home appliances

Truth Table (Positive Logic)

Input	V_{CC}-V_{EE} Positive Going	V_{CC}-V_{EE} Negative Going	Output
L	0 to 30 V	0 to 30V	L
H	0 to 11.5V	0 to 10V	L
H	11.5 to 13.5V	10 to 12V	Transition
H	13.5 to 30V	12 to 30V	H

Absolute Maximum Ratings (T_A=25℃)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	25	mA
	Pulse Forward Current*1	I_{FP}	1	A
	Reverse voltage	V_R	5	V
Output	"H" Peak Output current*2	I_{OPH}	-2	A
	"L" Peak Output Current*2	I_{OPL}	2	A
	Pear Output Voltage	V_O	35	V
	Supply Voltage	V_{CC}- V_{EE}	0 to 35	V
	Power Dissipation	P_C	250	mW
Operating frequency*3		f	50	mW
Isolation voltage *4		V_{ISO}	5000	V rms
Total Power Dissipation		P_T	300	°C
Operating temperature		T_{OPR}	-40 ~ +100	°C
Storage temperature		T_{STG}	-55 ~ +125	°C
Soldering temperature *5		T_{SOL}	260	°C

Notes:

*1 Pulse width ≤ 1 μs, 300pps.

*2 Max. pulse width=10us, max. duty cycle =0.2%

*3 Exponential waveform pulse width P_W ≤ 0.3us, I_{OPH}≥-1.5A, I_{OPL}≤1.5A

*4 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1 to 4 are shorted together, and pins 5 to 8 are shorted together.

*5 For 10 seconds.

Electrical Characteristics

Apply over all recommended condition, typical value is measured at V_{CC}=30V, V_{EE}= ground, T_A=25°C unless specified otherwise.

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	I_F = 10mA
Reverse voltage	V_R	5.0	-	-	V	I_R = 10μA
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/°C	I_F =10mA
Input capacitance	C_{IN}	-	60	-	pF	V_F=0, f=1MHz

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I_{CCH}	-	1.7	5	mA	I_F=7mA to16mA, V_O= Open
Low level supply current	I_{CCL}	-	1.7	5	mA	V_F=0 to 0.8V, V_O= Open

Transfer Characteristics

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High Level Output Current*[6]	I_{OH}	-0.2	-	-	A	V_O=V_{CC}-0.75V
	I_{OH}	-1	-	-	A	V_O=V_{CC}-4V
Low Level Output Current*[6]	I_{OL}	0.2	-	-	A	V_O=V_{EE} +0.75V
	I_{OL}	1	-	-	A	V_O=V_{EE} +4V
High Level Output Voltage	V_{OH}	V_{CC}-4	-	-	V	I_F=10mA, I_O=-1A
	V_{OH}	V_{CC}-0.5	-	-	V	I_F=10mA, I_O=-100mA
Low Level Output Voltage	V_{OL}	-	-	V_{EE}+4	V	I_F=0mA, I_O=1A
	V_{OL}	-	-	V_{EE}+0.5	V	I_F=0mA, I_O=100mA
Input Threshold Current	I_{FLH}	-	2.3	5	mA	I_O=0mA, V_O >5V
Input Threshold Voltage	V_{FHL}	0.8	-	-	V	I_O=0mA,, V_O <5V
Under Voltage Lockout Threshold	V_{UVLO+}	11	-	13.5	V	I_F=10mA,, V_O >5V
Under Voltage Lockout Threshold	V_{UVLO-}	9.5	-	12.0	V	I_F=10mA,, V_O <5V

Switching Characteristics

Apply over all recommended condition, typical value is measured at V_{CC}=30V, V_{EE}= ground, T_A=25°C unless specified otherwise.

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output High level*5 (Fig.12)	t_{PHL}	100	200	500	ns	I_F= 7 to16mA C_L = 10nF, R_L=20Ω, f=10kHz, Duty=50%, T_A=25°C
Propagation delay time to output Low level*6 (Fig.12)	t_{PLH}	100	180	500	ns	
Pulse width distortion	$\|t_{PHL} - t_{PLH}\|$	-	20	100	ns	
Propagation Delay Skew*7	t_{PSK}	-350		350	ns	
Output rise time	t_r	-	60	-	ns	
Output fall time	t_f	-	60	-	ns	
UVLO Turn on Delay	$t_{UVLO\ ON}$	-	30	-	us	I_F=10mA, V_O>5V
UVLO Turn off Delay	$t_{UVLO\ OFF}$	-	0.4	-	us	I_F=10mA, V_O<5V
Common Mode Transient Immunity at Logic High*8	CM_H	-15	-	-	kV/μS	I_F = 7 to 16mA , V_{CC}=30V, R_L=350Ω, T_A=25°C V_{CM}=2kV
Common Mode Transient Immunity at Logic Low*9	CM_L	15	-	-	kV/μS	V_F = 0V , V_{CC}=30V, R_L=350Ω, T_A=25°C V_{CM}=2kV

Notes:

*6 Max. pulse width=10us, max. duty cycle =1.1%

*7 Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. t_{PHL} or t_{PLH}) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

*8 Common mode transient immunity at output high is the maximum tolerable negative dv/dt on the trailing edge of the common mode impulse signal, V_{CM}, to assure that the output will remain high (i.e. V_O>15.0V)

*9 Common mode transient immunity at output low is the maximum tolerable positive dv/dt on the leading edge of the common mode pulse signal, V_{CM}, to assure that the output will remain low (i.e. V_O<1.0V)

Typical Electro-Optical Characteristics Curves

Figure 1. Output High Voltage Drop vs. Output High Current

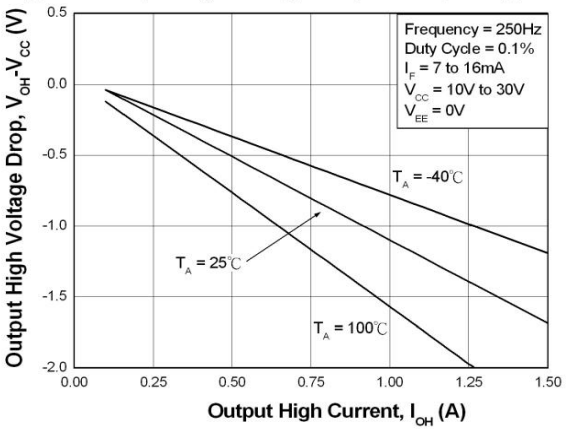


Figure 2. Output High Voltage Drop vs. Ambient Temperature

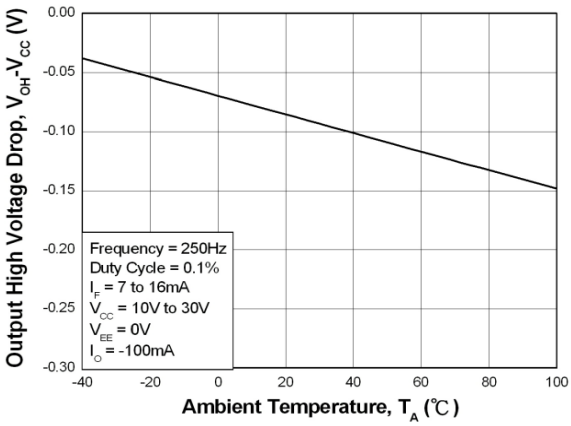


Figure 3. Output Low Voltage vs. Output Low Current

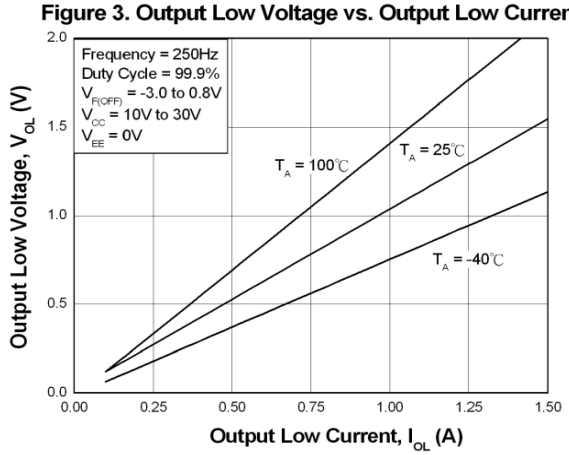


Figure 4. Output Low Voltage vs. Ambient Temperature

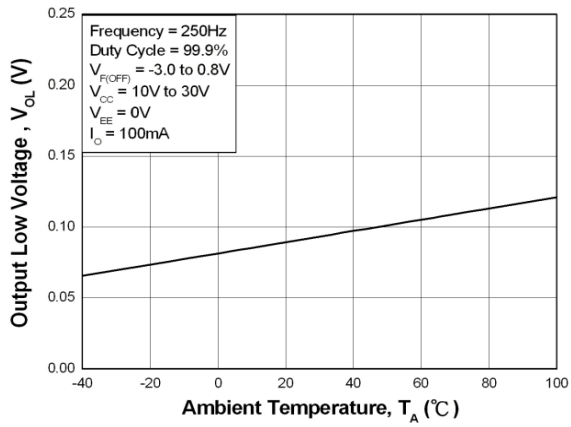


Figure 5. Supply Current vs. Ambient Temperature

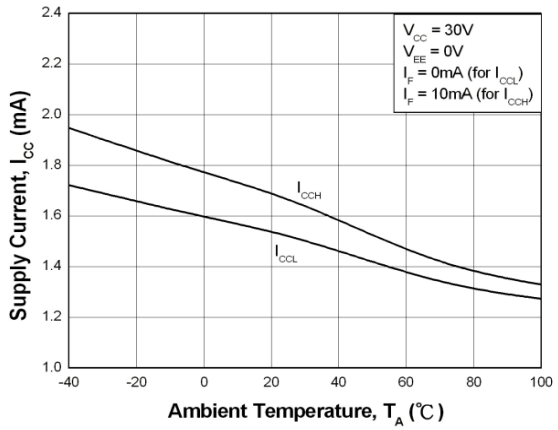


Figure 6. Supply Current vs. Supply Voltage

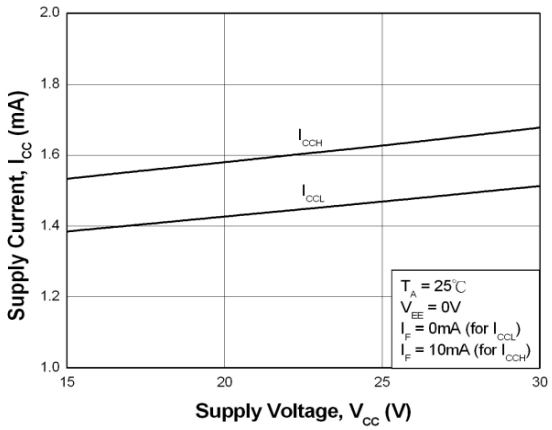


Figure 7. Low to High Input Current Threshold vs. Ambirnt Temperature

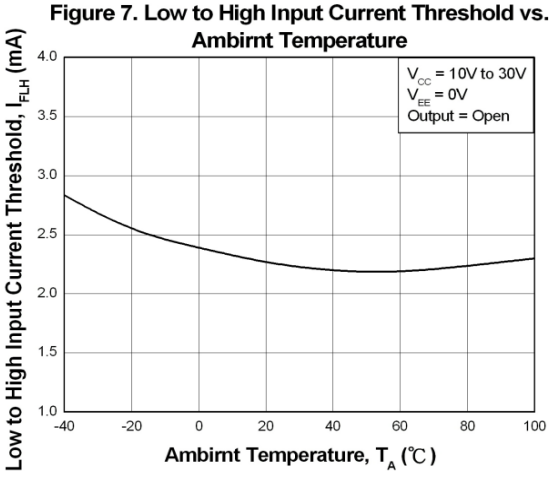


Figure 8. Propagation Delay vs. Supply Voltage

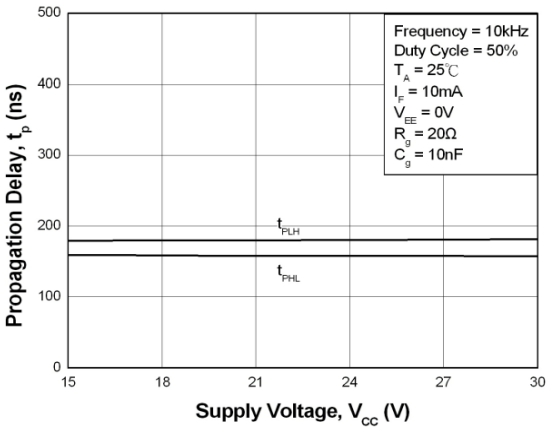


Figure 9. Propagation Delay vs. LED Forward Current

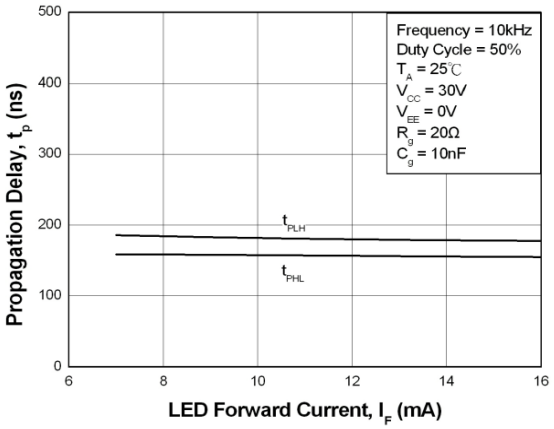


Figure 10. Propagation Delay vs. Ambient Temperature

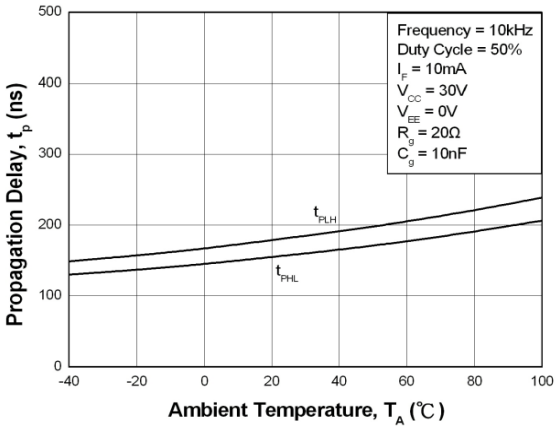


Figure 11. Propagation Delay vs. Sereies Load Resistance

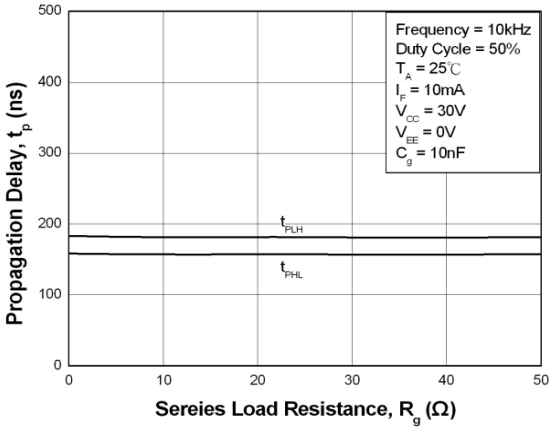


Figure 12. Propagation Delay vs. Load Capacitance

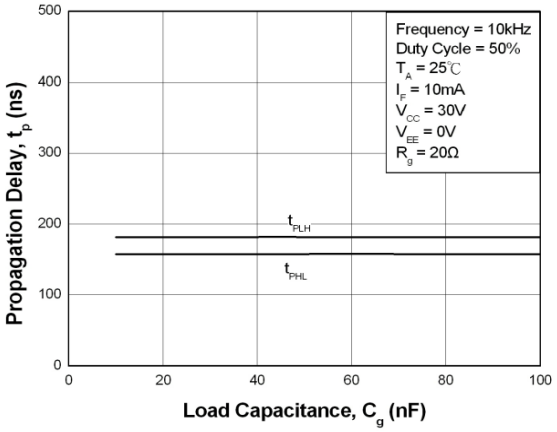


Figure 13. Transfer Characteristics

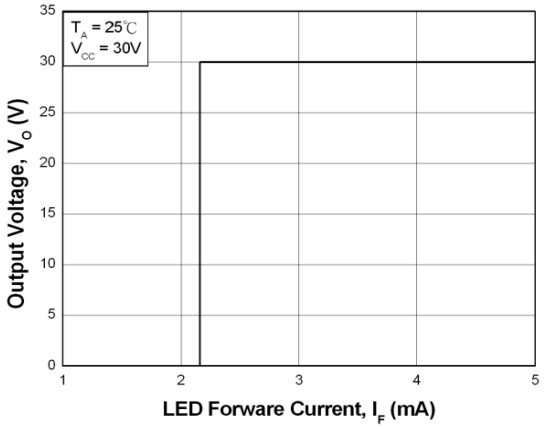


Figure 14. Input Forward Current vs. Forward Voltage

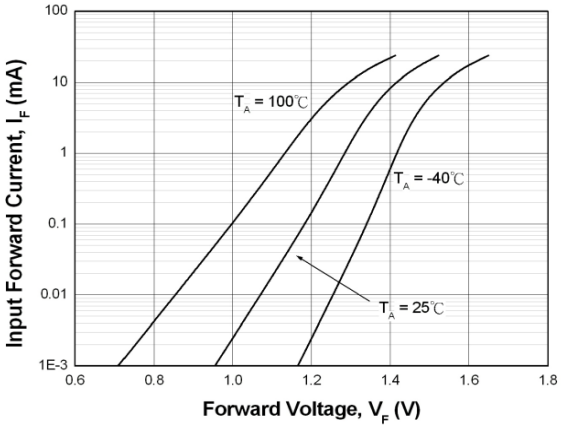
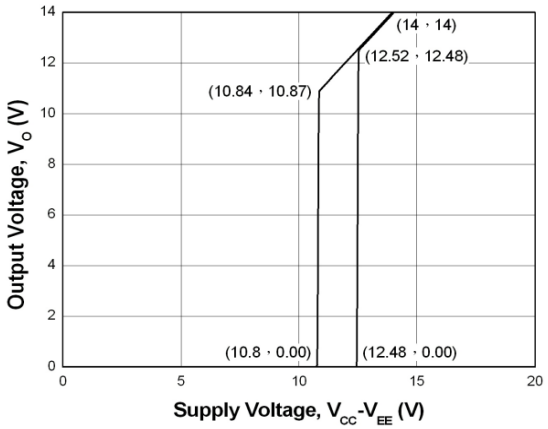
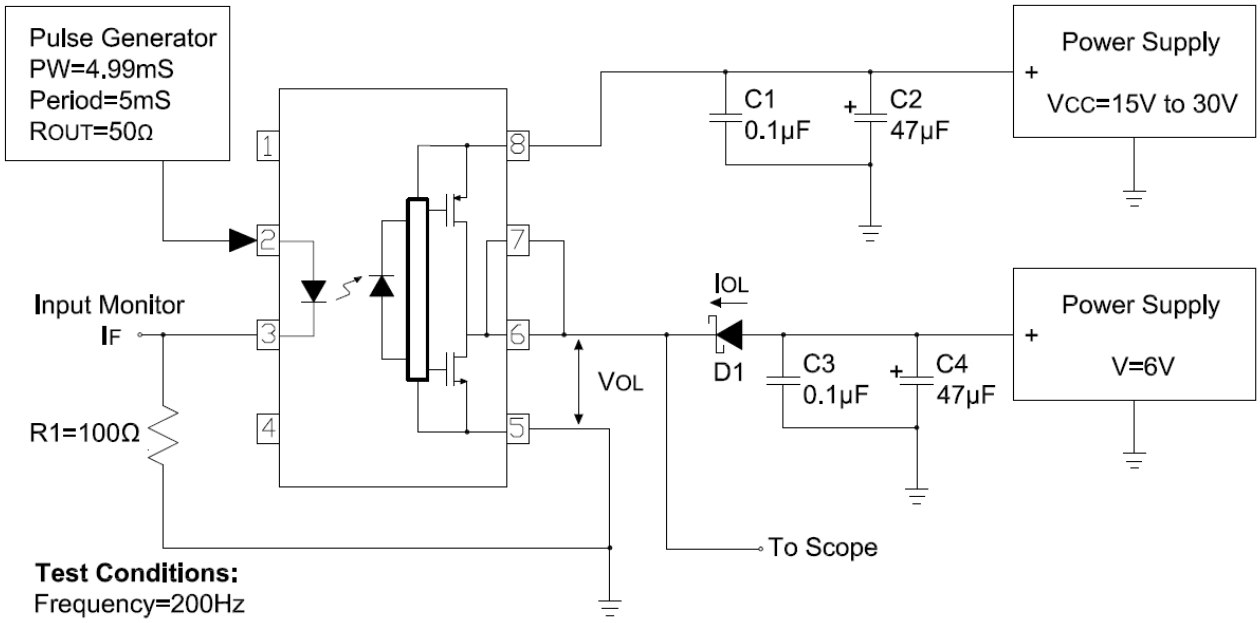


Figure 15. Under Voltage Lockout

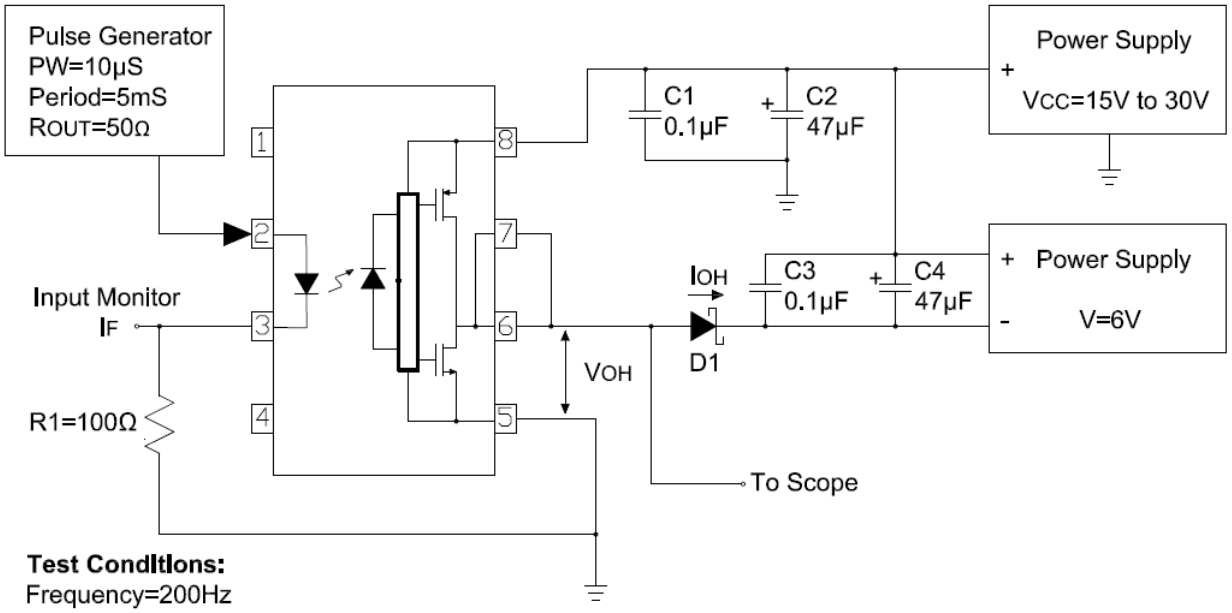


Test Circuit



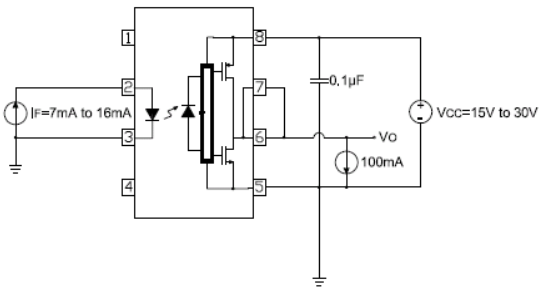
Test Conditions:
Frequency=200Hz
Duty Cycle=99.8%
VCC=15V to 30V
VEE=0V
VF(OFF)= -3.0V to 0.8V

I_{OL} Test Circuit

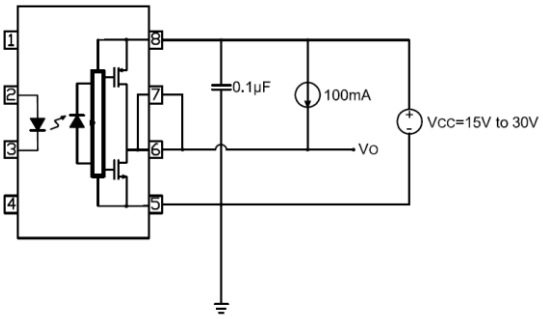


Test Conditions:
Frequency=200Hz
Duty Cycle=0.2%
VCC=15V to 30V
VEE=0V
IF=7mA to 16mA

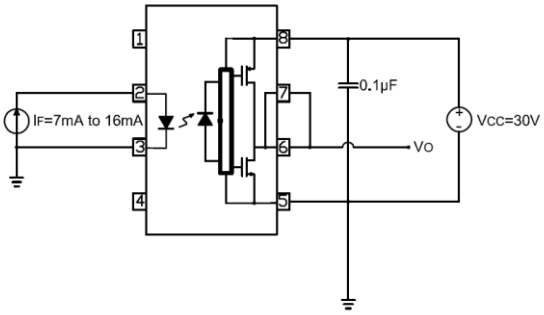
I_{OH} Test Circuit



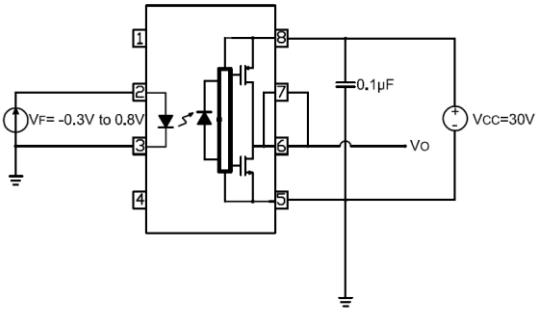
V_{OH} Test Circuit



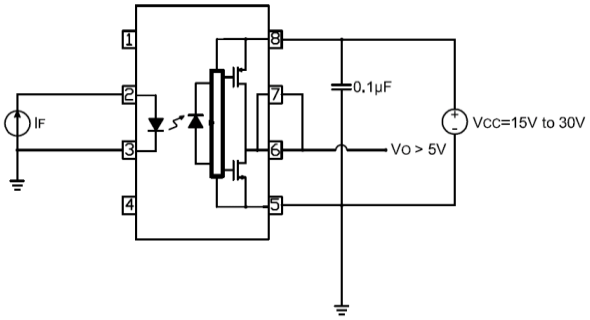
V_{OL} Test Circuit



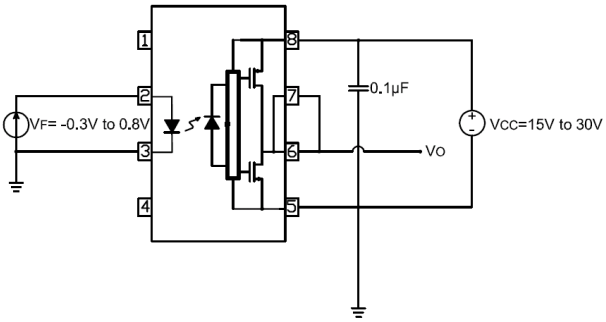
I_{CCH} Test Circuit



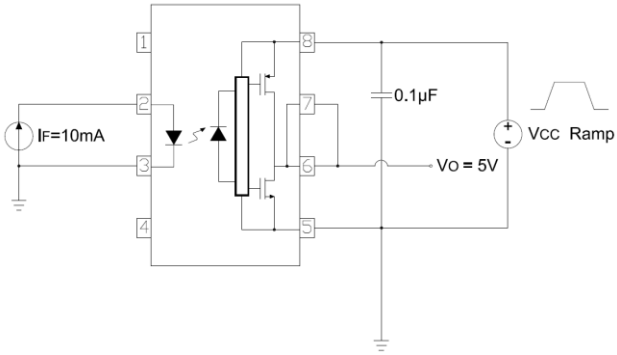
I_{CCL} Test Circuit



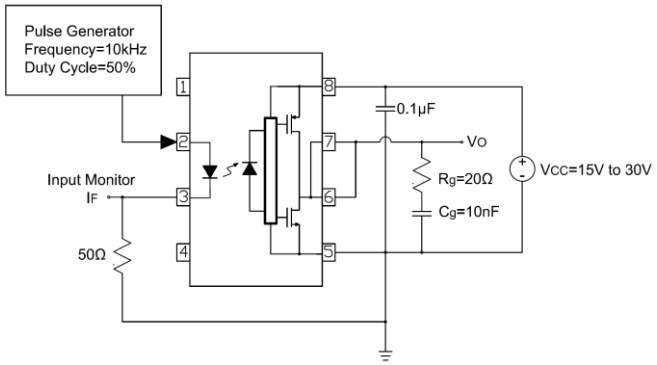
I_{FLH} Test Circuit



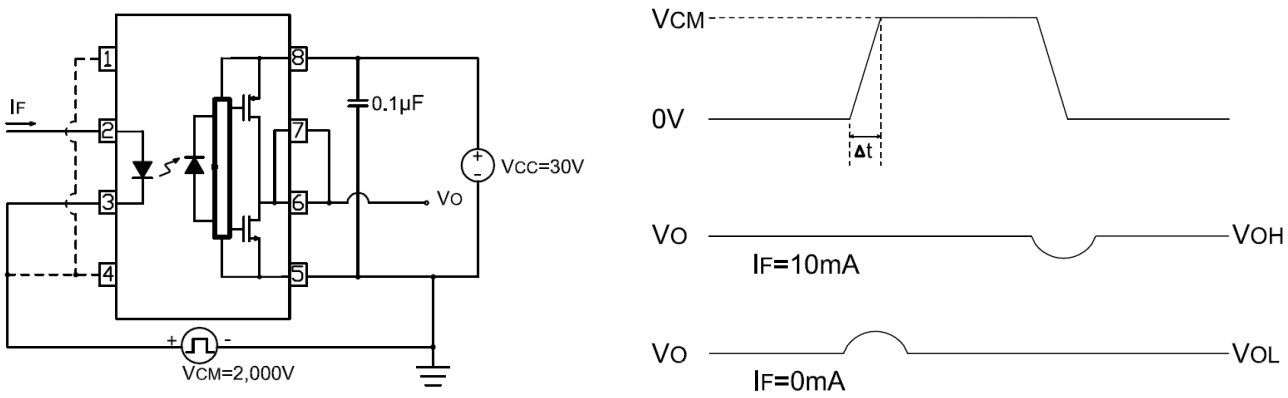
V_{FHL} Test Circuit



U_{VLO} Test Circuit



t_{PHL}, t_{PLH}, t_r and t_f Test Circuit and Waveforms



CMR Test Circuit and Waveforms

Order Information

Part Number

EL3150Y(Z)-V

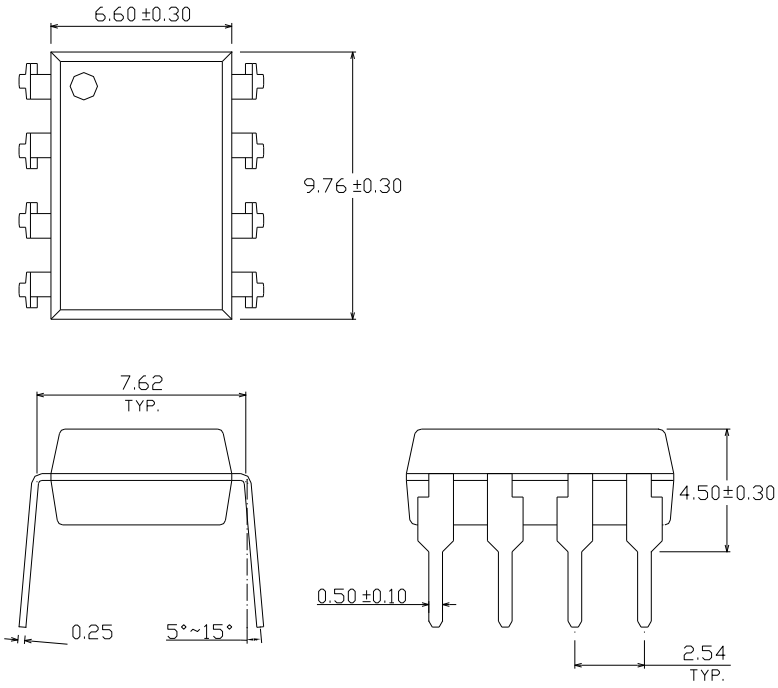
Note

Y = Lead form option (S, M or none)
Z = Tape and reel option (TA, TB or none).
V = VDE (optional)

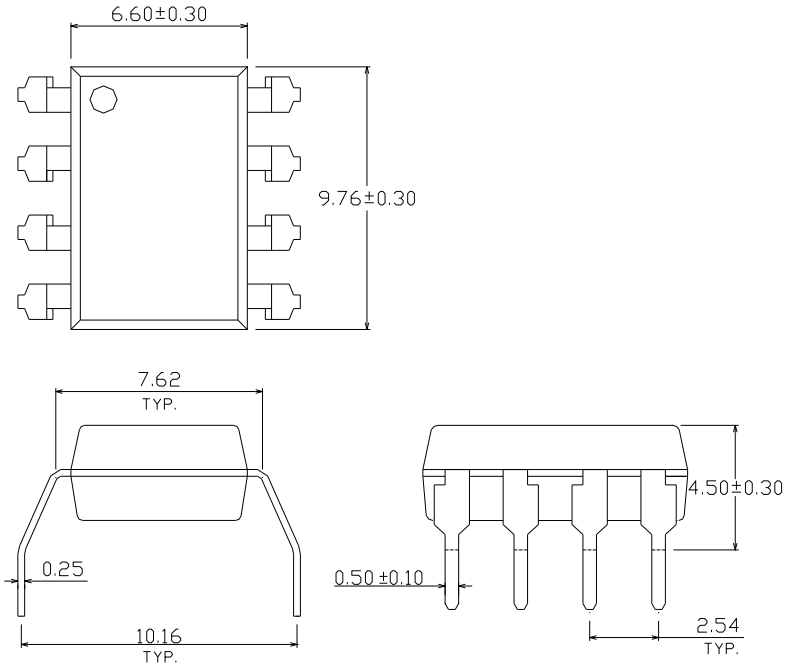
Option	Description	Packing quantity
None	Standard DIP-8	45 units per tube
M	Wide lead bend (0.4 inch spacing)	45 units per tube
S (TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
S (TB)	Surface mount lead form + TB tape & reel option	1000 units per reel

Package Dimension
(Dimensions in mm)

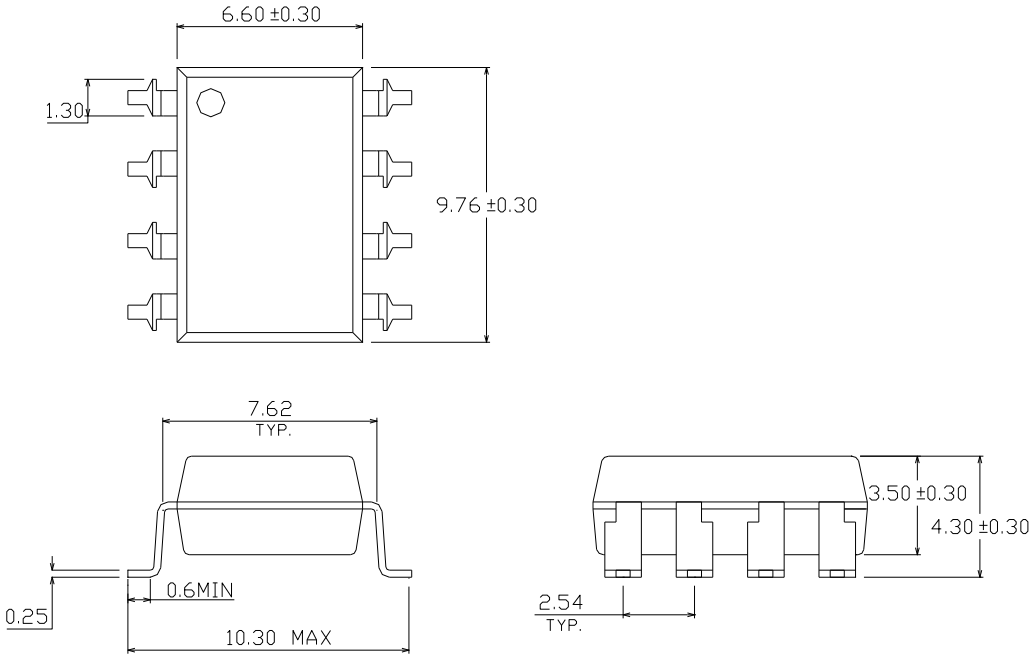
Standard DIP Type



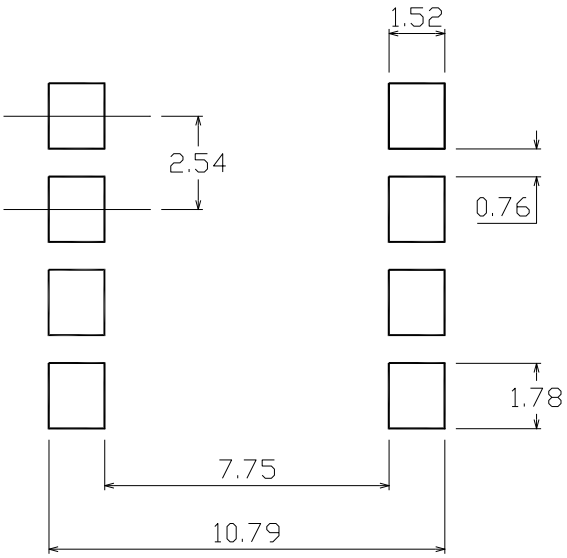
Option M Type



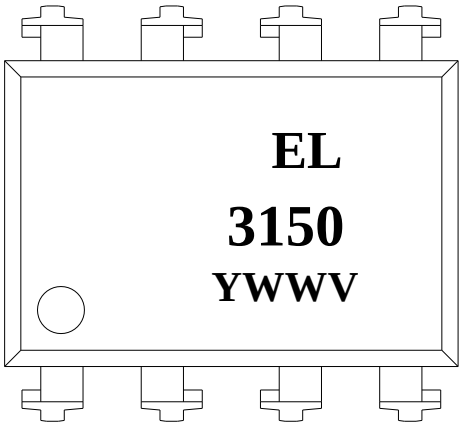
Option S Type



Recommended pad layout for surface mount leadform



Device Marking

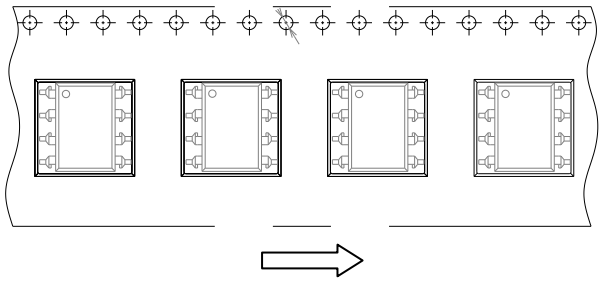


Notes

EL	denotes EVERLIGHT
3150	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

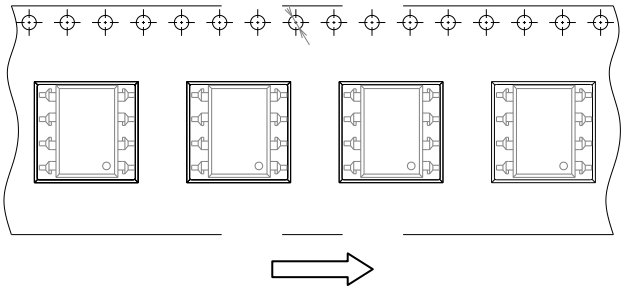
Tape & Reel Packing Specifications

Option TA



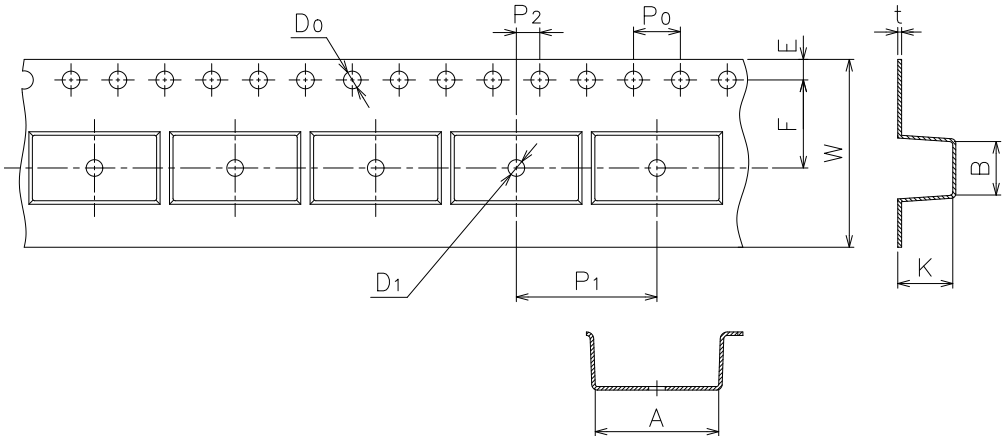
Direction of feed from reel

Option TB



Direction of feed from reel

Tape dimension

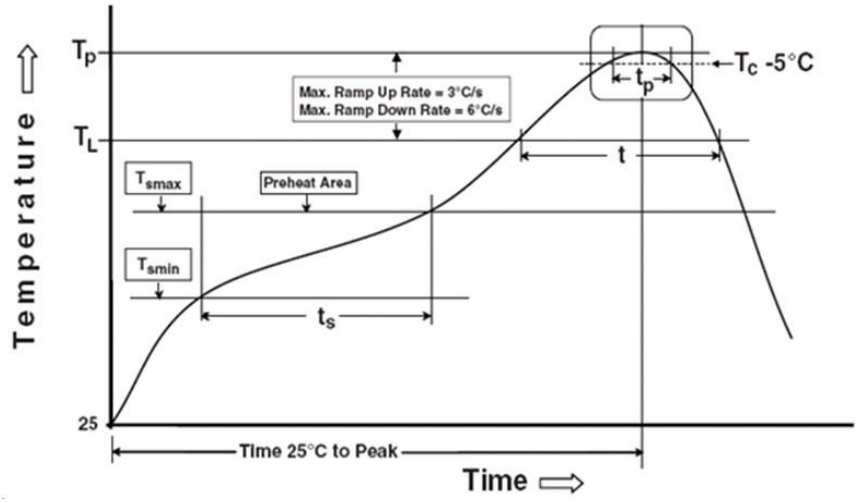


Dimension No.	**A**	**B**	**Do**	**D1**	**E**	**F**
Dimension(mm)	10.4±0.1	10.0±0.1	1.5+0.1/-0	1.5±0.25/-0	1.75±0.1	7.5±0.1
Dimension No.	**Po**	**P1**	**P2**	**t**	**W**	**K**
Dimension(mm)	4.0±0.1	12.0±0.1	2.0±0.05	0.4±0.05	16.0±0.3/	4.5±0.1

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note: Reference: IPC/JEDEC J-STD-020D

Preheat	
Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max
Other	
Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260°C
Time within 5 °C of Actual Peak Temperature: T_P - 5°C	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

DISCLAIMER

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. When using this product, please observe the absolute maximum ratings and the instructions for using outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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