Features

- Operating Supply Range 3.0V to 3.6V
- Power Dissipation 600mW Max
- Low-power Sleep Mode (<0.5mW)
- RF Data Channel
  - Programmable Gain Mode or Automatic Gain Control
  - Wide Bandwidth VGA
  - VGA Accepts Inputs from 30 - 300mV Peak-to-Peak Differential (PPD), 60 - 600mV_{PPD} or 110 - 1100mV_{PPD}
  - Programmable Equalization Via 7th-Order Equiripple Filter with Programmable Symmetric Zeros
  - Programmable 5-to-1 Filter Cutoff Range
  - Data Slicer with DC Restore Circuit
  - Wide Frequency Range Clock Extraction
  - Frequency Synthesizer with Independent 8-bit M and N Dividers, Better Than 1% Resolution
  - Highly Programmable to Accommodate DVD (1-5X) and CD (6X-30X)
  - Write Asymmetry Measurement For Adjusting Write Mode Power
  - Data Recovery Supports CLV, ZCLV, ZCAV Recording
- Servo Algebra for Focus and Tracking
  - 45 MHz Bandwidth for Differential Phase Tracking Detector
  - Land and Groove Detector for DVD RAM
  - Supports One Beam Push Pull Tracking Output
  - Supports One Beam Differential Phase Tracking
  - Focus Error Signal Output
  - Focus OK Signal
  - Track Crossing Detection
  - Mirror Signal Output
  - Wobble Detection for DVD RAM
  - Header Detection for DVD RAM
  - Optional Internally Generated Timing for AGC and Timing Recovery

Description

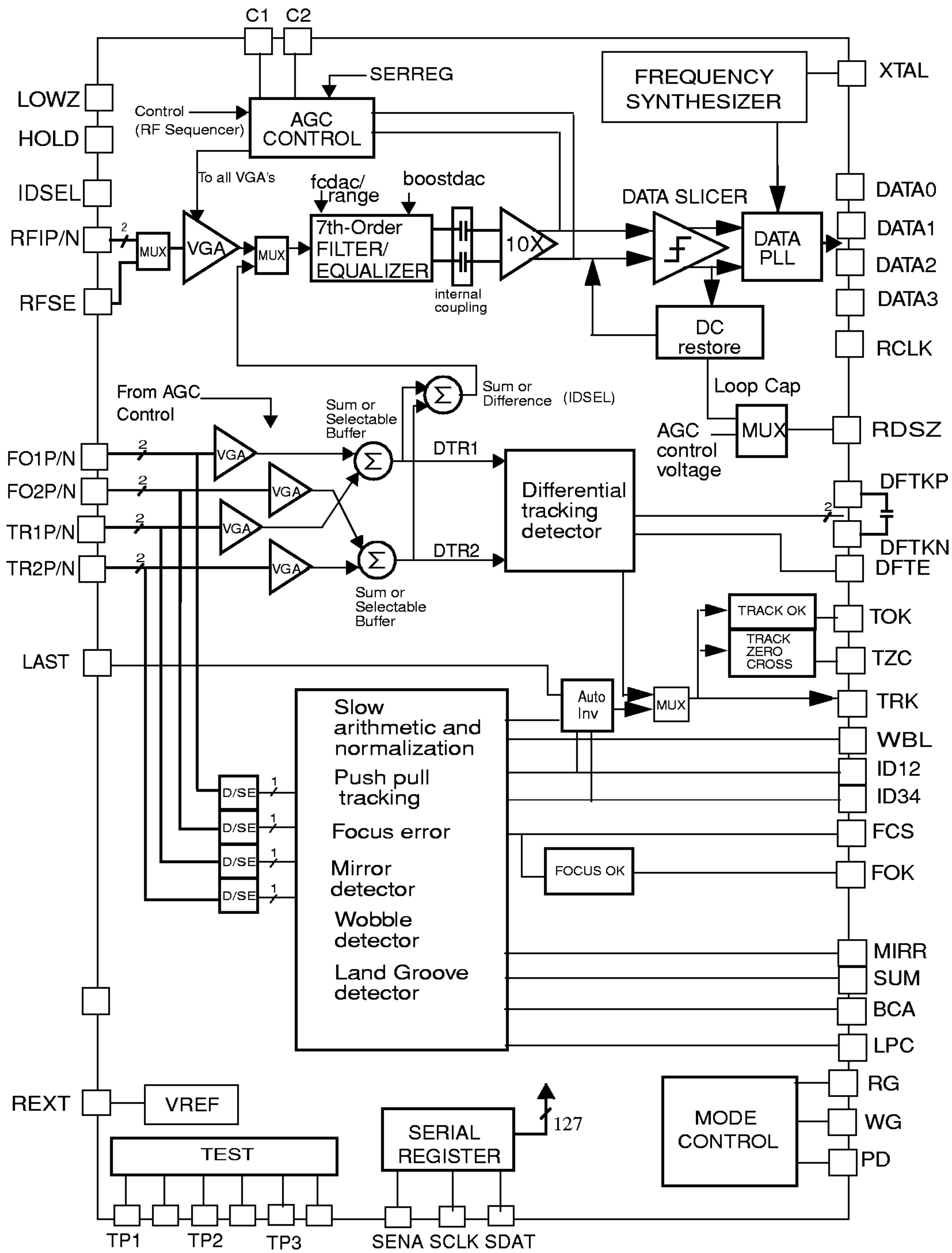
The AT78C1503 is a programmable DVD/CD channel responsible for servo algebra, gain control, equalization, bit detection and clock extraction for CD-ROM, DVD-ROM and DVD-RAM data. Programmable features allow data rates up to 5X DVD. Also for DVD-RAM functionality, the channel serves the write path providing laser power control and pit asymmetry detection. The CMOS channel operates from a single 3.3V supply and is fully programmable through a serial interface for both CD and DVD modes. The IC contains two separate processing channels. One for RF signal detection and synchronization, and the other for focus and tracking servo control. These are referred to as the RF channel and the servo channel respectively.

DVD/CD Read Channel

AT78C1503 Preliminary

Rev. 1214A–11/98

Figure 1. AT78C1503 Block Diagram



Functional Description

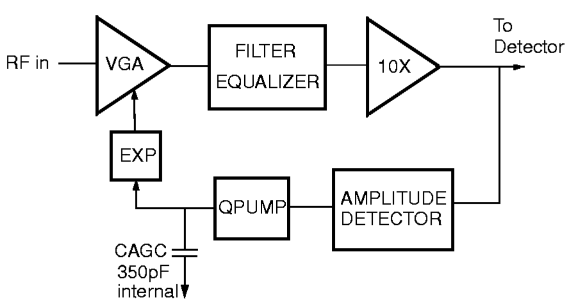
RF Channel Overall Description

The RF channel consists of gain control, equalization, bit detection and clock extraction and is shown in the block diagram of Figure 1. The readback signal is AC coupled from the preamplifier to the channel input RFP/RFN. A variable gain amplifier (VGA) is used for gain control of the readback signal. A 7th-order equiripple filter/equalizer is used for noise filtering and equalization of the signal before detection. The output of the equalizer feeds a fixed gain of ten stage which brings the internal level up to approximately 1V peak-to-peak differential (PPD). The output of the 10X amplifier enters the AGC control block which closes the AGC loop to maintain a $1V_{PPD}$ slicer input level while RF P/N is allowed to vary ten to one. The data slicer has a programmable slicing level or an adaptive DC restore system to maintain a DC free output of the slicer. The data slicer output is a digital stream and is sent to the clock extraction and synchronization circuitry. Clock extraction is performed with the data PLL which is operated in phase/frequency mode during write and idle modes and phase only mode when reading data. An on-board frequency synthesizer is used for locking the data PLL to a close initial frequency upon start up. Various test outputs are provided to aid the evaluation of the system. In addition an offset calibration routine executed on power up eliminates the need for internal AC coupling by correcting internal offsets over the parts operating conditions.

Gain Control

The AGC loop consists of VGA, 7th-order filter/equalizer, fixed gain of 10 amplifier, amplitude detector, dual-rate charge pump, internal loop filter and exponentiator as shown in Figure 2.

Figure 2. AGC Loop Block Diagram



The RF signal may be generated in several ways and the appropriate signal selected via the serial register as shown in the following table.

Table 1. RF Selection

RFSEL<1:0>	Operating Mode
00	Differential RF
01	Single-ended RF
10	RF internally Generated (FO1, FO2, TR1 and/or TR2)
11	RF internally Generated (FO1, FO2, TR1 and/or TR2)

If the RF signal is generated internally the configuration may be selected from the following table.

Note: FO1, FO2, TR1 and TR2 are defined in Table 17.

Table 2. Sum Mode Selection (IDSEL = 0)

SUM MODE <1:0>	Operating Mode
00	FO1 + FO2
01	TR1 + TR2
10	FO1 + FO2 + TR1 + TR2
11	FO1 + FO2 + TR1 + TR2

In order to read ID fields in DVD RAM the difference channel is selected as the RF input to the channel. The difference channel is selected when IDSEL (user input pin) is high.

This automatically deselects the RFP/N and RFSE inputs. In this mode the SUMMODE<1:0> bits can be programed to result in the following sum/differences.

Table 3. Sum Mode Selection (IDSEL = 1)

SUMMODE <1:0>	Operating Mode
00	FO1 - FO2
01	TR1 - TR2
10	FO1 - FO2 + TR1 - TR2
11	FO1 - FO2 + TR1 - TR2

Thus there are four ways in which RF signal is generated/chosen.

1. Dedicated differential RF inputs (RFP/N) which come from the preamp and are AC coupled.
2. Single-ended AC coupled RF which is generated by the preamp or by the CD section of the channel.
3. Generated from FO1, FO2, TR1 and/or TR2 inputs. These are AC coupled internal to the channel. No external AC coupling required.

If option 3 is chosen either FO1 + FO2, TR1 + TR2 or the sum FO1 + FO2 + TR1 + TR2 can be used as the RF input to the channel.

4. Generated from FO1, FO2, TR1 and/or TR2 inputs and IDSEL user input high.

If option 4 is chosen either FO1 - FO2, TR1 - TR2 or the sum/difference FO1 - FO2 + TR1 - TR2 can be used as the RF input to the channel.

The input signal range for any of the differential inputs: RFP/N, FO1P/N, FO2P/N, TR1P/N or TR2P/N can be selected via the serial register as shown in the following table.

Table 4. RF Input Range Selection

VGAMODE <1:0>	Operating Mode
00	110 - 1100mV
01	60 - 600mV
10	30 - 300mV
11	30 - 300mV

AGC mode is initiated by read gate (RG) high. The input impedance can be squelched during the initial start of AGC operation in order to quickly recover the AC coupling networks at the input to the RF channel and internal to the channel. This squelching period is referred to as LOWZ mode and the duration is set by the user either by the external LOWZ pin (high) or the internal RF sequencer. During LOWZ the AGC loop is set in hold mode so that no gain corrections are made. An external HOLD pin is also provided for the user to initiate agc loop hold when desired. After LOWZ a user programmable period is designated as fast mode. This period is set by either the external AGCFST pin (high) or by the internally generated fast sequence using the RF sequencer. During fast mode the AGC loop capacitor is quickly charged/discharged until the lock voltage is $1V_{PPD}$ and the remaining duration of the fast mode the AGC loop is in a high-bandwidth mode where the charge pump currents are 4 times that in normal operation. After fast mode the normal AGC operation starts and continues until RG goes low. For user programmable timing refer to the section on the RF sequencer.

The AGC loop is of the peak sampling type in which asymmetric charge/discharge currents are used to lock the peaks of the signal to a known voltage. This is accomplished by a 16-to-1 discharge to charge ratio. Minimum charge current is set nominally for 0.7µA and is continuously charging the AGC capacitor. The current is derived from the external resistor Rext and the internal bandgap voltage, thus resulting in a near zero temperature coefficient. The absolute value is process dependent on the internal bandgap (±5%) and the tolerance of the external resistor. The charge pump current may be scaled up via the serial register using the following serial register table.

Table 5. Charge Pump Current Selection (charging current)

AGCQP<3:0>	Charging Current
0000	TBD
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

When the signal hits the 100% threshold (i.e. $1V_{PPD}$) a discharge current of 16X (the user programed charging current) occurs for the duration that the signal is over 100%. The large discharge/charge ratio causes the loop to adjust the peaks of the output to the 100% threshold. Thus the input to the VGA is allowed to vary over a 10:1 range while the data slicer input is locked to a known value ($1V_{PPD}$).

When the device is in ID mode (IDSEL high) a second internal loop capacitor (CEXT2) is used as the loop integration capacitor. The voltage on CEXT1 is held while in ID mode and likewise in DATA mode (IDSEL low) the voltage on CEXT2 is held. This allows faster lock of the gain loop when switching between these two modes because the voltages are held close to their prior values. As stated previously CEXT1 and CEXT2 are internal 350pF capacitors however each has its own external pin which the user can monitor the control voltage on these caps. External access also allows the user to use external capacitors in parallel if lower loop bandwidth is desired in the system.

The VGA's may also be operated in a fixed gain mode by setting the appropriate register bit and using the gain control 4 bit DAC via the serial interface in accordance to the following table.

Table 6. PGC Mode Gain Settings

PGC<3:0>	Gain
0000	TBD
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

The AGC loop has several test points which can be monitored by the user. Test points designated as TP1 and TP3 are dedicated to the AGC circuitry. TP1 allows the user to monitor the inputs and outputs of all five VGA's as well as the signals out of the three summer/buffers as shown in Fig. 1. Each test point has a selection bit and an address bit. TP1EN and TP3EN bits are used to enable the test point output drivers. Also AGCCALTST should be asserted low for TP1<3:0> or TP3<1:0> to select the appropriate test point. If bit AGCCALTPON is set high TP1/TP3 control is overridden by CALADDR<6:0>, which is the calibration test point address selection. Calibration is an internal offset cancellation scheme used at various points throughout the channel. For more information refer to the calibration section. The test point maps for TP1, TP3 and calibration are as follows.

Table 7. Test Point 1 selection address

TP1 <3:0>	Gain
0000	VGA0 input
0001	VGA0 output
0010	VGA1 input
0011	VGA1 output
0100	VGA2 input
0101	VGA2 output
0110	VGA3 input
0111	VGA3 output
1000	VGA4 input
1001	VGA4 output
1010	DTR1 (Differential Tracking 1)
1011	DTR2 (Differential Tracking 2)

Table 8. Test Point 3 Selection Address

TP3 <1:0>	Gain
0000	AC couple input
0001	AMP10 input
0010	AMP10 output
0011	NA

Table 9. Test Point 1 and 3 Calibration Selection Address

CALADDR <6:0>	Gain
000000	NA
000001	VGA0 internal node
000010	VGA1 internal node
000011	VGA2 internal node
000100	VGA3 internal node
000101	VGA4 internal node
000110	AMP10 output

The test point gains are not unity and are actually lower depending on the test point in question. This means the voltages monitored on the test points are not the true internal voltages. TP1 has a gain of 0.8 from the internal nodes and TP3 has a gain of 0.65 from the internal nodes. These gains must be used in calculating certain absolute voltages stated in the spec. Example: the AGC lock voltage of $1V_{PPD}$.

7th-Order Filter/Equalizer

The on board filter/equalizer is implemented as a 7 pole 2 symmetric zero 0.05 degree equiripple phase lowpass filter. Cutoff frequency for the filter spans 4 - 26 MHz and is programmable through a 7 bit DAC. Two symmetric zeros provide user controlled boost up to 13dB from the low frequency gain. Group delay variation is maintained within $\pm$4% out to 1.5 times the cutoff frequency. The filter cutoff is stabilized over supply and temperature variations by using an external resistor and an internal control loop. Absolute cutoff is guaranteed within $\pm$10% of the specified value. The filter is incorporated into the AGC loop along with a final gain of 10 amplifier to bring the final detector input up to $1V_{PPD}$. Input and output to the CTF are available via TP2 for testing and system evaluation.

RF Data Detector and DC Restore

The output of the gain of 10 amplifier is the input to the RF detector. The detector is a slicer with the slicing threshold set by an internal feed back loop. The loop consists of a charge pump and an internal integrating capacitor. The digital output of the slicer is integrated and subtracted from the output of the gain of 10 amplifier removing any baseline variation. The charge pump current and capacitor values used in the detector are selectable through the serial register. It is also possible to disable the feedback loop and set the slicing threshold manually by programming a DAC through the serial register. The same DC restore circuitry is used in the asymmetry detection for determining written pit asymmetry. In this mode the slicer level is set to zero and the voltage on the integrating capacitor is output to pins TRTP1. Other internal signals that are also routed to TRTP1 include the slicer input, slicer output & charge-pump currents.

Figure 3. Data Slicer with DC Restore

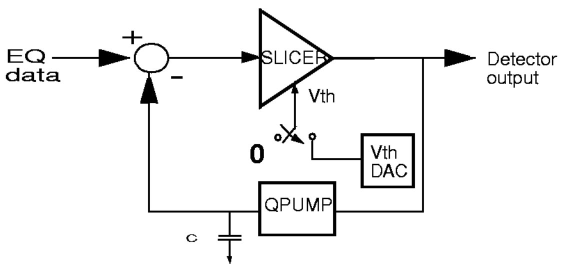


Table 10. Detector Modes of Operation

DETMODE <1:0>	Operating Mode
00	DC Restore Mode
01	Write Power Test Mode
10	don't use
11	Charge-pump Test Mode

Table 11. Detector Charge Pump Currents

DETIGM <1:0>	Current (µA)
01	5
00	20
10	40
11	don't use

Table 12. Detector Charge Pump current multiplier

DETKCP <1:0>	Multiplier
01	1.0
00	1.2
10	1.4
00	2.0 (don't use with DETIGM<1> = 1)

Table 13. Detector Capacitor Values

DETHPFILT <2:0>	Capacitance (pF)
000	don't use
001	20
010	40
011	60
100	80
101	100
110	120
111	140

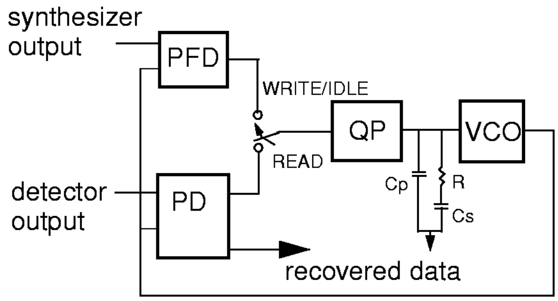
Physical ID Detection

The difference between the sum of the outputs of photodiodes (A + B) and (C + D) is sent differentially to the read channel pins DFP/N from the Atmel AT78C1505 preamplifier. When the channel is reading header information on the disk the IDSEL pin is asserted and the difference data from the preamp is muxed into the input pins of the AGC. The data is equalized and detected the through the RF channel. The detection of the ID fields to notify the controller are explained along with the Land/Groove detection in the servo section.

Timing Recovery PLL

The digital data out of the RF data detector is input to the data PLL. The purpose of the data PLL is to extract the system clock from the detected data and synchronize the detected data. The data PLL consists of phase/frequency comparator, phase only comparator, 2 to 1 multiplexer, charge pump, internal loop filter and VCO. Two outputs are generated, one is the retimed data available to the controller on a 4 bit bus and recovered clock with frequency equal to the recovered channel data rate divided by 4. Prior to the start of a read operation, the data PLL VCO is locked to the frequency synthesizer output which is programmed to the desired channel rate. This sets the data PLL VCO close to the desired frequency for read back. Locking the two PLL's is accomplished by choosing the frequency synthesizer output and the data PLL VCO as the inputs to the data PLL phase/frequency detector (PFD). When RG is asserted the detector output is used instead of the frequency synthesizer output for the phase comparison. In this mode the phase only comparator is used. The loop filter is implemented with on chip components, the transient characteristics of the loop are set internally based on the DVD readback rate. The loop filter components and charge pump currents are programmed using the serial register. The loop filter component values and currents are chosen such that the loop filter damping factor equals 1.2. The loop filter crossover frequency is nominally set to 1% of the data rate during acquisition and 0.5% of the data rate during track. The loop filter charge pump current values and loop filter component values are listed in Table 16. A block diagram of the data PLL is shown in Figure 4.

Figure 4. Timing recovery phase locked loop



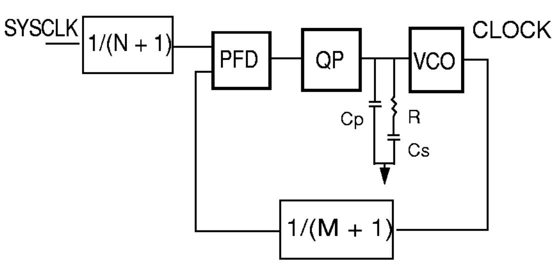
Frequency Synthesizer PLL

The frequency synthesizer is used for data PLL lock (write and idle modes) and for generating write data for DVD/RAM mode. A block diagram of the synthesizer is shown in Figure 5. The frequency synthesizer consists of phase/frequency comparator, charge pump, internal loop filter, VCO and internal dividers for generating all frequencies needed for DVD and CD operation. The frequency can be programmed with an accuracy better than 1%. The internal loop filter is fully differential to suppress common mode noise.

An external CMOS level clock reference divided by a programmable 8 bit counter and is used as a stable reference input to the phase frequency detector. The second input is the VCO divided by M, where M is an 8 bit programmable counter value. Frequencies from 26 MHz to130 MHz are supported with better than 1% resolution. The CLOCK frequency output to the data recovery section of the AT78C1503 is;

$$F_{CLOCK} = F_{SYSCLK}*(M + 1)/(N + 1)$$

Figure 5. Synthesizer phase locked loop



TR and Synthesizer Loop Parameters

V - to - I g_m = 98µA/V (HiGM = 1),
70µA/V (HiGM = 0)

K_{ICO} = 50% of f_c/100µA

The product of the two above parameters gives:

$g_m K_{ICO} = K_{VCO}$ = 49% of f_c/V (HiGM = 1),
35% of f_c/V (HiGM = 0)

TR and Synthesizer Loop Equations

$$\omega n = \sqrt{\frac{(In \cdot Kvco)/(2\pi)}{Cs}}$$

$$\zeta = (R/2) \cdot \sqrt{(In \cdot Cs \cdot Kvco)/(2\pi)}$$

where:

- ωn = loop's natural frequency (rad/s)
- ζ = damping factor
- In = Charge pump current divided by average number of bit times per VCO update (A) For reading random data, divide charge pump current by four to get In
- Cs = series capacitor in loop filter (F)
- R = resistor in loop filter (Ω)
- Kvco = VCO gain (rad/sV)
- Cp = Cs/20 (F)

Table 14. Charge Pump currents vs. HiIP and LoIP

HiIP	LoIP	Current (µA)
0	1	5
0	0	20
1	0	40
1	1	don't use

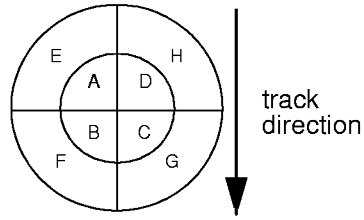
Table 15. Charge Pump current multiplier vs. KCP<1:0>

KCP<1:0>	Multiplier
01	1.0
00	1.2
10	1.4
00	2.0 (don't use with HiIP = 1)

Table 16. TR and synthesizer nominal loop filter components and charge pump settings.

R (KΩ)	Charge pump (µA)	Cs (pF)	f_c (MHz)	z
22.1	40	111	0.37	1.2
22.1	40	55	0.74	1.2
22.1	40	37	1.11	1.2
22.1	40	27	1.48	1.2
22.1	40	22	1.85	1.2
31.4	20	111	0.262	1.2
31.4	20	55	0.523	1.2
31.4	20	37	0.785	1.2
31.4	20	27	1.046	1.2
31.4	20	22	1.308	1.2
62.8	5	111	0.131	1.2
62.8	5	55	0.262	1.2
62.8	5	37	0.392	1.2
62.8	5	27	0.523	1.2
62.8	5	22	0.654	1.2

Figure 6. Photo diode array



Servo Channel Description

The AT78C1503 servo channel can process data from two types of photodiode arrays. The most common type is the A,B,C,D only array. In this case astigmatic focus is used. The other type of array is the 8 element array (see Figure 6). In this case ring focus is used. As shown in Figure 1 there are 4 differential signals: FO1P/N, FO2P/N, TR1P/N, TR2P/N. These inputs can also be used in a single-ended fashion by not connecting the negative side and also setting the appropriate bit TBD in the serial register to indicate that a single-ended interface has been selected.

Table 17.

Input Mode	1	2	3	4	5
Description of Operation Mode	Custom Ring Focus Mode	DVD ROM with Ring Focus	Standard DVD ROM	Standard DVD RAM	A,B,C,D Mode
FO1P/N	A + B + C + D	A + B + C + D	A + C	A + C	A
FO2P/N	E + F + G + H	E + F + G + H	B + D	B + D	B
TR1P/N	A + B + E + F	A + C + E + G	A + C	A + B	C
TR2P/N	C + D + G + H	B + D + F + H	B + D	C + D	D

Servo algebra is performed for focus, push-pull tracking, differential phase tracking, tangential push pull and land/groove detection. Table 17 shows a detailed explanation of the different modes of operation, and what signals are sent on FO1, FO2, TR1, TR2. Modes 1,2 are used for a custom mode of operation which has DVD ROM capability. Modes 3 and 4 are the standard DVD ROM/RAM for a 4 diode photodiode array. Mode 5 can also be used for the same purpose (DVD ROM/RAM) however internal switching is used to create equivalent FO1P/N FO2P/N TR1P/N TR2P/N signals.

A block diagram of the fast servo arithmetic functions are shown in Figure 1 and a block diagram of the slow servo arithmetic functions are shown in Figure 3.

Fast Servo Arithmetic Functions

Differential Phase Tracking

The differential phase tracking signal is generated using the ac coupled outputs of the diagonal elements in the fast diode array in Figure 6. The sums (A + C) and (B + D) are independently equalized by an equalizer with the transfer function shown in Figure 2 The unity gain frequency of the equalizers can be set from 995 kHz to 5 MHz with serial register TBD. The output of the equalizers EQ are compared to an offset voltage programmed by serial register TBD. The phases of the outputs of the comparators are compared by the phase detector PD shown Figure 1. The phase detector output lead/lag signals are lowpass filtered with a single pole lowpass filter. The pole at the DVD 1X setting will be at 30 kHz and pole location will be programmed through serial register TBD.

Figure 7. Fast Servo Arithmetic

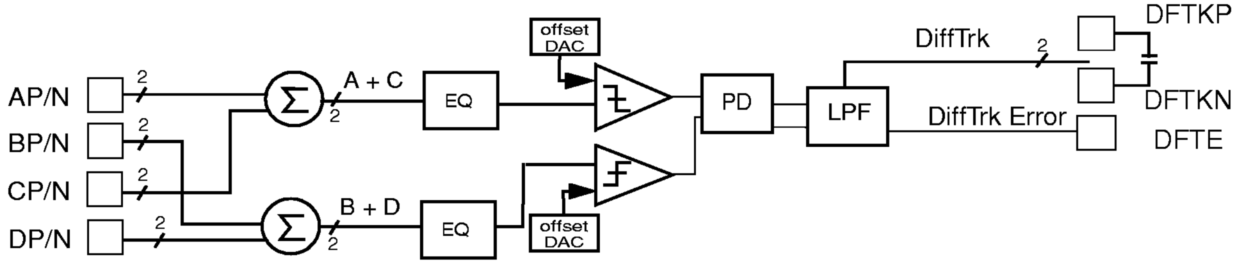
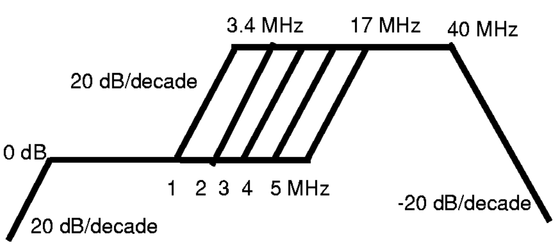


Figure 8. Differential phase tracking EQ transfer function



Slow Servo Arithmetic Functions

In Figure 9 is shown the top level diagram for the slow servo. The first block has inputs FO1, FO2, TR1, TR2 and its functionality is as follows:

First there is a Sample and Hold function on all the 4 inputs. The S/H is done from an external CMOS input pin TBD. The minimum amount of time for the Hold state is 30ns, and it should not exceed 200ns. The minimum amount of time for the Sample state depends on how much the signal changes between samples. For example if ak + 1 - ak is half of the dynamic range on FO1, FO2, TR1, TR2 then the sample state should not be less then 20ns. In reality the S/H signal will be slew rate limited by the CMOS I/O input.

Second there is a Differential to single-ended conversion and a VGA function on each input. The reference for the D2S function is referenced from the supply and it varies from VDD -1.5V to VDD -2V via a 3 bit D/A. This reference is also sent as an output off chip, in case it needs to be used to a reference in a preamp.The VGA range is between 0.3 to 4 (16 exponentially spaced steps) with a worst case bandwidth of 15 MHz. The VGA outputs go also to ID Detector, Wobble Detector, and Mirror Field Detector blocks. There is also an option which resets the values of FO1, FO2, TR1, TR2 to their midrange point (ex. 0V differential). This option is used for electronic offset correction on the Focus Error and Tracking Error signal described later in this section.

For the slow servo each of the four inputs contains a single pole low pass filter with a programmable cutoff frequency between 150 to 500 kHz. The cutoff frequency is programmable with a 3 bit SR control which does not track the channel data rate.

Next block is a Voltage to Current converter followed by a ±30% gain adjust (4 bits + sign) and a ±30% offset adjust (4 bits + sign) on each individual channel. As Table 17 shows for modes 1, 2, 3 and 4, the partial sums will have the gain and offset adjust. For mode 5, the signals A, B, C and D will get the gain and offset adjust.

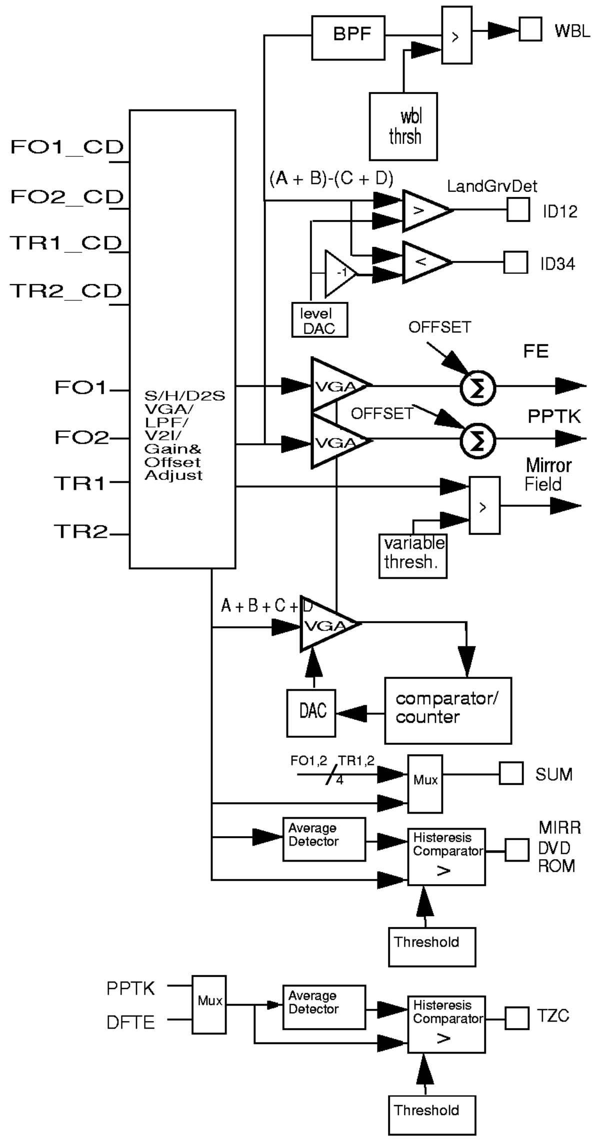
These gain and offset adjusted signals are now summed together and the sum feeds a digitally controlled AGC loop (also known as the normalization loop). Maintaining a constant output voltage at the output of the AGC loop normalizes the input to the focus and push-pull tracking error signals, so the error signals are not dependent on the strength of the light returned to the photo-diodes. This normalization alleviates differences due to media reflectivity. This loop consists of a VGA, counter (7 bits) and comparators. The clock for the counter is selectable: It can either be a divide by 3*X of the data rate (X ranges between 3 and 16) or a divide by 3*Y of the oscillator frequency (Y ranges between 1 and 16). The reason behind the two different clock domains is that when the normalization loop is used for normal operation (read, erase, write) collecting data along the tracks, will be desirable for the loop bandwidth to follow the data rate. For the Tracking error during a seek however, it might be desirable for the loop bandwidth to be independent of data rate. The normalization loop has a fast acquisition mode controlled by 2 bits TBD. Depending on this setting the counter can count by either 1, 2, 4, 8 every time when the error signal exceeds a threshold which is also programmable by 2 bits TBD. This feature helps the normalization loop track fast slewing signals in the A + B + C + B signal.

Focus error signal (FE) for modes 1, 2, 3, 4 is FO1 - FO2. For mode 5, FE = (A + C) - (B + D) = (FO1 + TR1) - (FO2 + TR2). The FE signal is then passed through a VGA which is slaved to the normalization loop. The dynamic range on the FE is between 0.5 to 2.5V centered around 1.5V. There is also a ±0.5 V offset added to the FE signal using a 3-bit + sign D/A. In addition, the gain on the Focus Error is adjustable between 1 to 5 using a 3 bit gain adjust (exponentially spaced). There is high gain chip input TBD which flips between gain = 1 and the gain set by the 3 bit gain adjust. For the gain of 1 setting the FE is linear and covers 0.5 - 2.5 range. For a gain higher then 1 the FE will saturate.

Push Pull Tracking error signal (PPTK) for modes 1, 2, 3 and 4 is TR1 - TR2. For mode 5, PPTK = (A + C) - (B + D) = (FO1 + FO2) - (TR1 + TR2). The PPTK signal is then passed through a VGA which is slaved to the normalization loop. The dynamic range on the PPTK is between 0.5V to 2.5V centered around 1.5V. There is also a ±0.5 V offset added to the PPTK signal using a 3bit + sign D/A. In addition, the gain on the Tracking error is adjustable between 1 to 5 using a 3 bit gain adjust (exponentially spaced). For the gain of 1 setting the PPTK is linear and covers 0.5 - 2.5 range. For a gain higher than 1 the PPTK will saturate.

The Track Zero Crossing (TZC) signal is needed for counting tracks during a seek operation. Part of the TZC function is an Average Detector function (see Figure 3) which follows the average of either the PPTK or DFTE (Differential Phase tracking error) signals. The architecture of the Average Detect Function (ADF) is similar to the normalization loop. The only difference is that rather then keeping a constant output this loop follows the input with different bandwidths. The clock frequency for this ADF block is a divide by 2*X of the crystal, where X is between 1 and 2048. The maximum clock frequency however should not exceed 8 MHz. This bandwidth is controlled by 2 input pins (BWUP, BWDWN). When each of these pins is toggled by the servo chip the bandwidth of the ADF macro goes UP or DOWN by a factor of 2. There are 11 steps for the bandwidth. This big bandwidth range is helpful because it can track in real time the head velocity during a seek. When BWUP and BWDWN are both high, the loop bandwidth point to a location in the serial register.

Figure 9. Slow Servo Arithmetic



The comparator which compares the output of the ADF block with the incoming signal (PPTK or DFTE) has a programmable hysteresis with a maximum value between 50 to 300mV. For a given setting the hysteresis goes down at 6dB/octave (4 points) as soon as TZC bandwidth equals the bandwidth at the front-end of the servo block (200K to 500K). The total range that the hysteresis varies is 4 to 1. This is done in order to reduce the hysteresis of the comparator as signals faster then the servo LPF setting (200k - 500k) are passed through the system. For example assume the front-end LP is set at 200k and the comparator hysteresis is set at 100mV.

Then, as the bandwidth of the TZC goes higher the 200K the hysteresis is as shown Table 18.

Table 18.

TZC Bandwidth	Comparator Hysteresis
128 k	100mV
256k	70mV
512k	50mV
1M	35mV

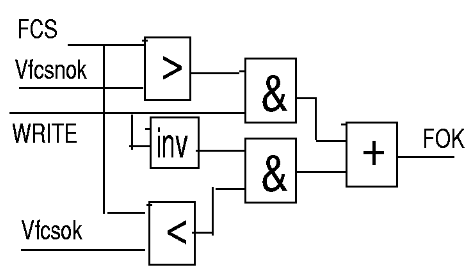
The mirror circuit for DVD ROM has the same function as the Track Zero Crossing. The only difference is that its input is the total sum A + B + C + D. This circuit shares the same BWUP, BWDWN inputs as the TZC circuit and also shares the same register location for the default bandwidth. The hysteresis however for its output comparator is a different register location (50 - 300mV).

The total sum A + B + C + D is sent off chip to the servo controller. The dynamic range is 0.5 to 2.5 volts. On the same output pin we also mux FO1, FO2, TR1, TR2 in order to do the ±30% gain and offset adjust discussed earlier. The bandwidth of the total sum output is 100 kHz. There is also going to be a reference pin (typically 1.5V from ground) which when configured as an output, the signals going to the servo ADC are internally referenced, When the reference is configured as an input (with a SR bit TBD) then the external reference is used to output the signals to the servo ADC.

The mirror field detector is different then the mirror for DVD ROM. This circuit monitors the total sum before the 200 - 500k LP and using a programmable threshold comparator controlled by bits TDB in the SR flags the mirror field.

The focus OK and track OK signals output a CMOS logic high signal during write when the focus error signal or tracking error signal is too large. The signals are derived from the WRITE gate input signal being TRUE and their respective error signals being greater than a preset value. This is schematically drawn in Figure 4 for the focus OK signal.

Figure 10. Focus NOK



The slow servo channel also provides the ID field indication and wobble signal detector blocks.

ID Header Detection

The difference between the sum of the outputs of photodiodes (A + B) and (C + D) is determined in the slow servo block. The difference signal passes through a fixed gain of 3 V/V before passing through a programmable gain of 3 to 0.2 V/V. This difference signal is then internally AC coupled with the pole set at 4 kHz. The signal then goes to a 2nd order lowpass filter for the ID header detection and a 5th order band pass filter for wobble detection.

The 2nd order lowpass filter used for ID header detection has a programmable cutoff of 100 kHz times the DVD rate and a low frequency gain of 2 V/V. The output of this filter is used as the input to the ID header detector.

Following a long region of user data, the ID detector has been reset and is ready for header detection. When the lowpassed difference signals absolute value exceeds the programmable threshold set by IDTHRES<3:0>, (0 - 450mV), the ID12 pin is asserted indicating the detection of ID header 1 & 2. The following threshold crossing of opposite polarity will cause the ID34 pin to be asserted indicating the second header field has been detected. The sign of the signal for ID12 determines if the push-pull tracking error is negated or not, i.e. indicating the start of a land or a groove. If the polarity is positive then a groove region is being entered and the polarity of the tracking error is not negated. If the polarity of the signal is negative then a land region is being entered and the sign of the tracking error is negated.

The comparators used for header detection are clocked from a system clock derived from the frequency synthesizer at a XX rate. The ID detector resets itself after 512 bytes if it has failed to detect the absence of ID header 3 & 4.

RF Sequencer

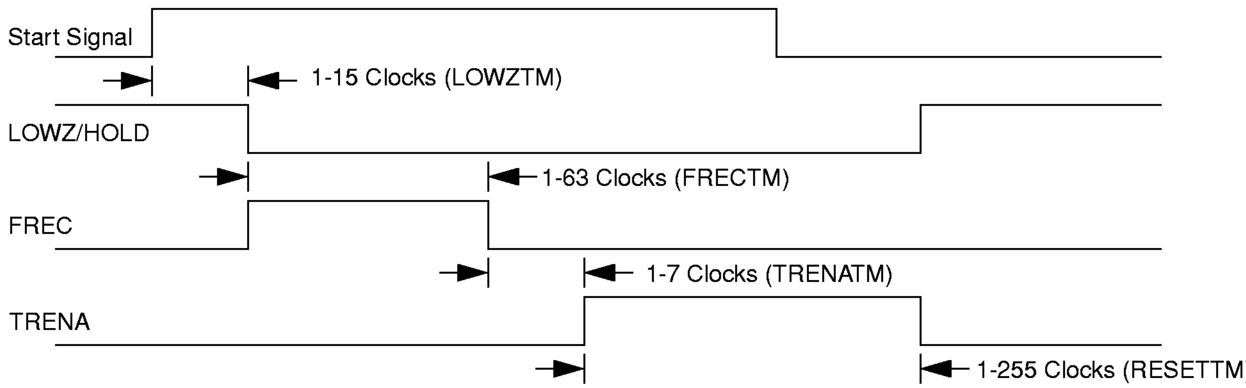
The RF sequencer provides the capability to internally control the RF paths timing sequence when entering a header area for RAM or user data for any supported media. The RF signals which it can control are the AGCs LOWZ, HOLD and Fast RECovery signals and also the signal to indicate the need to switch to data mode in the timing recovery block (TRENA). When enabled, the sequencers outputs are logically OR'ed with the corresponding external pins and is especially useful at start-up when the controller doesn't know the exact laser position yet.

The sequencer may be started in several ways, all of which may be enabled or disabled. In DVD RAM header mode, the sequencer may be started with the assertion of the internally generated ID12 and ID34 or the external input pin IDSEL.

The choice of which mode the sequencer starts with is determined by the state of the header hold (HDHLD) pin. If HDHLD is asserted, logically high, the internally generated ID12 signal is used to start the sequencer. This is useful under the condition the controller does not yet know the laser location or the controller does not contain the circuitry required to generate the RF control signals or the user believes the channel chip can more accurately detect the headers then the controller can time them. If HDHLD is not asserted, logically low, then the external pin IDSEL may be used to start the RF sequencer. This mode would be useful if the controller does not contain the required logic to generate the RF signals or if fewer inter-connects between the controller and channel were desired. In all types of media, the RF sequencer may also be started with the assertion of the pin RG. This again would be useful if the controller does not contain the required logic.

The RF sequencers system clock is derived from the frequency synthesizer divided by four so it is therefore clocked at a nibble rate with respect to the RF channel rate. As stated above, the start signal for the sequencer can be one of several possibilities. The lengths of each timing field are user programmable and are all stated in terms of nibble rate. Figure 5 shows the generated signals and the amount of programmability for each field.

Figure 11. RF Path Timing Sequence



Auto Inverter

The auto inverter stage passes the tracking signal after the last sector in a track is read and the sequence of signs of DFP/N is positive then negative and the transition is from a groove to a land track. If the sequence of signs of the difference data is negative then positive at the last sector in a track the tracking signal is negated. The controller chip will send a logic signal to the read channel chip that the sector being read is the last sector on the LAST pin. The auto inverter block holds the sign of the tracking error signal for the complete track. The AT78C1503 requires the controller to signal the sector being read is the last sector.

Wobble Signal Detect

Like the ID header signal, the wobble signal is detected using the difference between the outputs of photodiode (A + B) and (C + D). This difference signal is processed identically to the ID header signal up to the point of filtering.

The wobble signal is extracted with a bandpass filter centered at 157 kHz times the DVD rate which has 20 dB of passband gain. The output of the fifth order bandpass filter is synchronously compared to the WBL DAC setting. If the level of the bandpass filter output is above the DAC level a CMOS level high signal is output on the WBL pin. The clocked used to strobe the comparator is derived from the frequency synthesizer at a TBD rate.

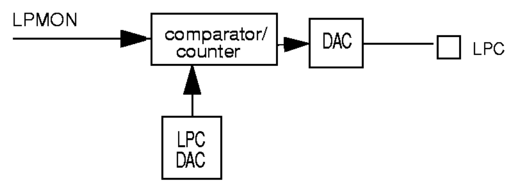
Burst Cutting Area and Defect Detection

The Burst Cutting Area (BCA) pin provides BCA and defect detect information. BCA/defect detection is accomplished by comparing the SLOSUM value to a percentage of the peak value of the SLOSUM signal. When the SLOSUM signal is greater than the held peak value a CMOS high is set on the BCA pin.

Laser Power Control

The Laser power control block is shown in Figure 6. The system varies the LPC output pin to control the read laser and keep the output power at a constant level during reads. The output of the read laser monitor diode is fed from the preamp to the AT78C1503 LPMON pin and compared to a nominal setting. If the value of the LPMON is higher than the nominal value the counter will count down, the laser reference voltage output will then decrease, likewise if the LPMON signal is lower than the nominal value the counter will count up. The output of the counter drives a DAC that sends a reference voltage to the laser.

Figure 12. Laser Power Control



Note: Disclaimer to users of this table. The location of some (if not all) of the bits in this serial register will probably change. Write your code in order to minimize the impact of such changes, e.g. define these bit locations in only one place in your program.

Table 19. Serial Register Bit Map

Register	Bit(s)	Description
		**** All bits active high unless otherwise noted** **** All DACs Linear unless otherwise noted**
0	0	SLEEP, Power down chip
	1	PGCEN, Programmable gain mode
	2:5	PGC<3:0>, Programmable gain magnitude
	6:3	AGCCALTPON, enable cal test point selection, disable TP1<3:0> TP3<1:0> from controlling the outputs on TP1 and TP3 respectively
	7	AGCHLD, AGC Programmable Hold
1	3:0	AGCQP<3:0>, AGC loop charge pump currents
	4	AGCHBW, Enable AGC High Band Width mode during fast recovery
	7:5	VGAMODE<2:0>, Selects input range for the VGA's 30 - 300mV, 60 - 600mV, 110 - 1100mV
2	2:0	RFSEL<2:0>, Selects which signal is used as the internal RF in which the channel processes: RFPN, RFSE or internally generated partial sum of FO1, FO2, TR1 and/or TR2 inputs
	3	ACBYP, bypass the internal AC coupling before the gain of ten amplifier
	4	FLTBYP, bypass the filter
	7:5	SUMMODE<2:0>, user defines which signals FO1, FO2, TR1 and/or TR2 to use for DTR1, DTR2 and RF generated signals
3	3:0	TP1<3:0>, Test point 1 select address
	4	TP1EN, Test point 1 output driver enable
	5:6	TP3<1:0>, Test point 3 select address
	7	TP3EN, Test point 3 output driver enable
4		LEAVE OPEN MOVE ALL REGISTERS DOWN BY ONE
4 MOVE to 5 etc.	5:0	TP2<5:0>, Test Point 2 Select, see Table 22
	6	MONINT, Selects BQDs internal nodes to be output for test
	7	NOBST, Disables Boost feature

Table 19. Serial Register Bit Map

Register	Bit(s)	Description
		**** All bits active high unless otherwise noted** **** All DACs Linear unless otherwise noted**
5	4:0	BOOST<4:0>, Filter Boost
	7:5	FLTRSELI<2:0>, Determines offset current in filter
6	3:0	FC<3:0>, Filter Cutoff
	6:4	RANGE<2:0>, Filter Cutoff Range Select
7		
8	1	DETRST
	2	DETRPDN
	3	DETRPUP
	5:4	DETKCP<1:0>
	7:6	DETIGM<1:0>
9	0	DETTHRESH_RNG
	7:1	DETTHRES<6:0>
10	2:0	DETQPOFF_RNG<2:0>
	4:3	DETMODE<1:0>
	7:5	DETTHPFILT<2:0>
11	7:0	ACQ_CNT<7:0>, Acquisition Count. Following the rising edge of RG, acquisition mode lasts (Acquisition Count + 1)×4×TR VCO cycles.
12	3:0	TPD<3:0>, Test Point Digital
	4	TPDEN, Test Point Digital Enable
	7:5	DVDX, DVD speed, where X = 1 - 5; 0 = disabled
13	ACQ_FLT<7:0>, TR Loop Filter Acquisition setting	
	0	Add Cs = 37.1 pF, Cp = 1.86 pF to loop filter
	1	Add Cs = 24.7 pF, Cp = 1.24 pF to loop filter
	2	Add Cs = 16.5 pF, Cp = 0.83 pF to loop filter
	3	Add Cs = 10.9 pF, Cp = 0.55 pF to loop filter
	4	Add Cs = 22.0 pF, Cp = 1.10 pF to loop filter
	5	Remove R = 9.3 KΩ from loop filter
	6	Remove R = 22.2 KΩ from loop filter
	7	Remove R = 31.4 KΩ from loop filter
14	7:0	TRK_FLT<7:0>, TR Tracking Filter setting, use ACQ_FLT table

Table 19. Serial Register Bit Map

Register	Bit(s)	Description
		**** All bits active high unless otherwise noted** **** All DACs Linear unless otherwise noted**
15		ACQ_CPI<1:0>, TR Acquisition Charge Pump Current, see Table 14
	0	LoIP
	1	HiIP
		TRK_CPI<1:0>, TR Tracking Charge Pump Current, see Table 14
	2	LoIP
	3	HiIP
	5:4	TRKCP<1:0>, TR Charge Pump Gain, see Table 15
	6	TRHIGM, TR Hi g_m K_{VCO} = 49% of f_c/V (HiGM = 1), 35% of f_c/V (HiGM = 0)
	7	RITPLLOD, Increase TR Q Pump Offset Calibration Range by 25%
16	2:0	TRTP1<2:0>, TR Test Point 1 Select, see Table 26
	5:3	TRTP2<2:0>, TR Test Point 2 Select, see Table 27
	6	TRTST, TR Test mode enabled
17	0	TRR_DIV4, Reset Divide by 4 flip-flops in TR phase-frequency detector
	1	TRR_PUPD, Reset PU and PD flip-flops in TR phase-frequency detector
	2	TRS_PU, Set PU flip-flop in TR phase-frequency detector
	3	TRS_PD, Set PD flip-flop in TR phase-frequency detector
	4	R_DAT, Reset Data flip-flops in detector
	5	NRZ, recovered data in NRZ format (NRZ high) recovered data 1 on transition, 0 otherwise (DVD format) (NRZ low)
	6	PD_RE, TR Phase detector active on data rising edge only
	7	PD_FE, TR Phase detector active on data falling edge only
18	0	SLEEP_TR, independently sleeps TR
	1	SLEEP_SY, independently sleeps Synthesizer
	4:2	unused
	5	EXDATA, External Data muxed into TR detector
	6	EXTRV, External TR VCO substituted for regular TR VCO
	7	TRSHRTC, Shorts TR filter
19		
20	7:0	SYN_FLT<7:0>, Synthesizer Filter setting, use ACQ_FLT table

Table 19. Serial Register Bit Map

Register	Bit(s)	Description
		**** All bits active high unless otherwise noted** **** All DACs Linear unless otherwise noted**
21		SYN_CPI<1:0>, Synthesizer Charge Pump Current, see Table 14
	0	LoIP
	1	HiIP
	3:2	unused
	5:4	SYKCP<1:0>, Synthesizer Charge Pump Gain, see Table 15
	6	SYHIGM, Synthesizer Hi g_m K_{VCO} = 49% of f_c/V (HiGM = 1), 35% of f_c/V (HiGM = 0)
	7	RISPLLOD, Increase Synth Q Pump Offset Calibration Range by 25%
22	1:0	SYTP1<1:0>, Synthesizer Test Point 1 Select, see Table 28
	5:3	SYTP2<2:0>, Synthesizer Test Point 2 Select, see Table 29
	6	SYTST, Synthesizer Test Mode Enabled
	7	SEL_ZTC, Select ZTC ICO reference instead of slaved to Synthesizer
23	0	SYR_DIV4, Reset Divide by 4 ff's in Synth phase-frequency detector
	1	SYR_PUPD, Reset PU and PD ff's in Synth phase-frequency detector
	2	SYS_PU, Set PU flip-flop in Synth phase-frequency detector
	3	SYS_PD, Set PD flip-flop in Synth phase-frequency detector
	4	R_SYNDIV, Reset flip-flops in synthesizer's M counter
	5	EXSYCK, External Reference Clock mux'd into Synth detector
	6	EXSYV, External Synth VCO substituted for regular Synth VCO
	7	Unused
24		
25	<5:0>	Offset Calibration Starting Pointer
	6	DISINIT, Disables the serreg reset at the beginning of offset calibration
	7	CALENBLE, OR'ed with TBD pin's rising edge to start calibration,
26	<5:0>	Offset Calibration Ending Pointer
	<7:6>	OFFCLKSEL, Master clocks frequency for the offset calibration
		*** The following are internal adjusts which are NOT meant to adjusted by user ***
60	<3:0>	FCTRIM, Filter Center Frequency Trim
61	3:0	VGAGAIN, VGA Gain Trim
	7:4	ZERO, Filter Parasitic Zero Adjust
62	4:0	SYICOTRM, Synthesizer ICO Trim
	7:5	SELEXTRM, Bandgap Voltage Trim
63	4:0	TRICOTRM, Timing Recovery ICO Trim

Table 20. Internal Calibration DACs and Test Addresses

Register	Cal Addr	Bit(s)	Description (** DACs are Sign Magnitude unless otherwise stated**)
64	0	Test	NA
65	1	4:0	VGA0 internal node (output before output driver) (RF amp)
66	2	4:0	VGA1 internal node (FO1 amp)
67	3	4:0	VGA2 internal node (FO2 amp)
68	4	4:0	VGA3 internal node (TR1 amp)
69	5	4:0	VGA4 internal node (TR2 amp)
70	6	5:0	AMP10 output (gain of 10 amplifier)
71	7		DPD Master
72	8	Test	
73	9	6:0	
74	10	6:0	DCROFF, DC Restore QPUMP Offset
75	11	6:0	TROFF, Timing Recovery QPUMP Offset
76	12	6:0	SYOFF, Synthesizer QPUMP Offset
77	13		Focus Error
78	14		Tracking Error
79	15		TBD
80	16	6:0	Filter MSTRM 1
81	17	6:0	Filter MSTRM 2
82	18	6:0	Filter MSTRM 3
83	19	6:0	Filter MSTRM 4
84	20	6:0	Filter MSTR1 1
84	21	6:0	Filter MSTR1 2
86	22	6:0	Filter MSTR1 3
87	23	6:0	Filter MSTR1 4
88	24	6:0	Filter BQD1 1
89	25	6:0	Filter BQD1 2
90	26	6:0	Filter BQD1 3
91	27	6:0	Filter BQD1 4
92	28	6:0	Filter MSTR2 1
93	29	6:0	Filter MSTR2 2
94	30	6:0	Filter MSTR2 3
95	31	6:0	Filter MSTR2 4
96	32	6:0	Filter BQD2 1
97	33	6:0	Filter BQD2 2
98	34	6:0	Filter BQD2 3

Table 20. Internal Calibration DACs and Test Addresses

Register	Cal Addr	Bit(s)	Description (** DACs are Sign Magnitude unless otherwise stated**)
99	35	6:0	Filter BQD2 4
100	36	6:0	Filter MSTR3 1
101	37	6:0	Filter MSTR3 2
102	38	6:0	Filter MSTR3 3
103	39	6:0	Filter MSTR3 4
104	40	6:0	Filter BQD3 1
105	41	6:0	Filter BQD3 2
106	42	6:0	Filter BQD3 3
107	43	6:0	Filter BQD3 4

Table 21. Test Points 1 and 3 Mapping

TP1<3:0> TP3<1:0>	Test Point 1 (TP1P/N)	Test Point 3 (TP3P/N)
0	VGA0 input	AC couple input
1	VGA0 output	AMP10 input
2	VGA1 input	AMP10 output
3	VGA1 output	unused
4	VGA2 input	NA
5	VGA2 output	NA
6	VGA3 input	NA
7	VGA3 output	NA
8	VGA4 input	NA
9	VGA4 output	NA
10	DTR1	NA
11	DTR2	NA

Table 22. Test Point 2 Mapping

	Test Point 2 (TP2P/N)	
TP2<5:0>	MONINT = 0	MONINT = 1
16 - >19	MSTRM Shorted Output	
20 - >23	MSTR1 Shorted Output	
24 - >27	BQD1 Output	BQD1 Internal
28 - >31	MSTR2 Shorted Output	
32 - >35	BQD2 Output	BQD2 Internal
36 - >39	MSTR3 Shorted Output	
40 - >43	BQD3 Output	BQD3 Internal
44 - >47	LP Output	Filter Input on TP2, Filter Output on TP1 (w/TP1 Enabled)

Table 23. Digital Test Point Mapping

TPD<1:0>	Digital Test Point
0	Unused
1	TR Acquisition (low) or Tracking (hi) mode
2	TR Pump Up, Pump Down Clear
3	Unused

Table 24. TR and Synth Test Input 1 Mapping

TR and Synth Test Input 1
Replace TR VCO if serial register bit EXTRV is true
Replace Synth VCO if serial register bit EXSYV is true

Table 25. TR and Synth Test Input 2 Mapping

TR and Synth Test Input 2
Replace Raw Data input to TR if serial register bit EXDATA is true
Replace Synth VCO if serial register bit EXSYCK is true

Table 26. TR Test Point 1 Mapping

TRTP1<2:0>	TR Test Point 1
0	TR Pump Up
1	TR Raw Data (input data from DC Restore block)
2	Recovered Clock (recovered from raw data stream)
3	unused
4	DC Restore Slicer Charge Pump Currents
5	DC Restore Slicer Charge Pump Capacitor Voltage
6	DC Restore Slicer Threshold Voltage
7	Unused

Table 27. TR Test Point 2 Mapping

TRTP2<2:0>	TR Test Point 2
0	TR Pump Down
1	TR Recovered Data (serial stream)
2	(FLTB) TR Loop Filter, buffered
3	(FCSB) TR Loop Filter Large Cap, buffered
4	(FLTU) TR Loop Filter, unbuffered
5	(FCSB) TR Loop Filter Large Cap, unbuffered
6	Unused
7	Unused

Table 28. Synthesizer Test Point 1 Mapping

SYTP1<1:0>	Synthesizer Test Point 1
0	Synth Pump Up
1	Synth VCO divided by DVDX
2	Synth VCO
3	Synth VCO divided by 4

Table 29. Synthesizer Test Point 2 Mapping

SYTP2<2:0>	Synthesizer Test Point 2
0	Synth Pump Down
1	unused
2	(FLTB) Synth Loop Filter, buffered
3	(FCSB) Synth Loop Filter Large Cap, buffered
4	(FLTU) Synth Loop Filter, unbuffered
5	(FCSB) Synth Loop Filter Large Cap, unbuffered
6	unused
7	unused

Electrical Characteristics

Operating Conditions: V_{DD} = 3.0V to 3.6V and T_A = 0 to 70ºC.

Supply Specifications

Parameter	Sym	Conditions	Min	Typ	Max	Units
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Supply current	I_{DD}			100		mA
Sleep mode current	I_{DDS}				100	µA

Digital Input/Output (CMOS compatible)

Parameter	Sym	Conditions	Min	Typ	Max	Units
High level input voltage	V_{IH}		V_{DD} - 0.5			V
Low level input voltage	V_{IL}				0.5	V
High/Low level input current					10	mA
High level output voltage	V_{OH}	I_{OH} = 0.5mA	V_{DD}-0.2			V
Low level output voltage	V_{OL}	I_{OL} = 0.5mA			0.4	

Bandgap Reference

Parameter	Sym	Conditions	Min	Typ	Max	Units
Output Voltage	VBG		1.15	1.2	1.25	V
Reference Resistor	REXT	Reference resistor from VBG to V_{SS} (ground)		12		kΩ
Sleep Mode Current	IDDS				100	mA

Variable Gain Amplifier (VGA)

Parameter	Sym	Conditions	Min	Typ	Max	Units
Gain Range			1		10	V/V
Input Dynamic Range (Low Mode)	DRL		30		300	mV
Input Dynamic Range (High Mode)	DRH		60		600	mV
Bandwidth	AGCBW	-3dB	100			MHz
AGC Control Sensitivity		AGC mode		20		dB/V
AGC Locking Voltage (input to data slicer)	VAGC	Peak-to-peak differential (PPD) input to slicer in AGC mode		1		V
Total Harmonic Distortion	THD	Measured at the detector input. $1V_{PPD}$ lock in AGC mode			2	%
Common Mode Rejection Ratio	CMRR	Vin = 250mV common mode @10 MHz		40		dB
Power Supply Rejection Ratio	PSRR	Vsup = 250 mV @10 MHz		40		dB

7th-Order Equiripple Filter/Equalizer

Parameter	Sym	Conditions	Min	Typ	Max	Units
Filter Cutoff Frequency Programmability	Fc		4.4		22	MHz
Filter Boost Range	Fb	Measured from lowfrequency gain	0		13	dB
Cutoff Frequency Accuracy		All frequency ranges	-10		+10	%
Boost Accuracy		All frequency ranges	-2		+2	dB
Group Delay Variation		All frequency ranges	-4		+4	%

Data Phased Locked Loop

Paarameter	Sym	Conditions	Min	Typ	Max	Units
Frequency supported		DVD 1X = 26.16 MHz	1		5	X DVD
RMS Jitter				TBD		degrees
Acquisition time						bits
Pull-in range			-2.5		+2.5	%

Frequency Synthesizer

Parameter	Sym	Conditions	Min	Typ	Max	Units
Frequency Supported		DVD 1X = 26.16 MHz	1		5	X DVD
External Source				26.16		MHz

Serial Register

Parameter	Sym	Conditions	Min	Typ	Max	Units
Serial Clock Frequency	SCLK		0.01		20	MHz
SENA to SCLK Setup Time	TEC	Transition time serial enable to serial clock	10			ns
SCLK Pulse Width	TPW		20			ns
SCLK to SDATA Hold Time	THCD		10			ns
SDATA to SCLK Setup Time	TSDC		10			ns

Figure 13. Serial Port Timing Diagram

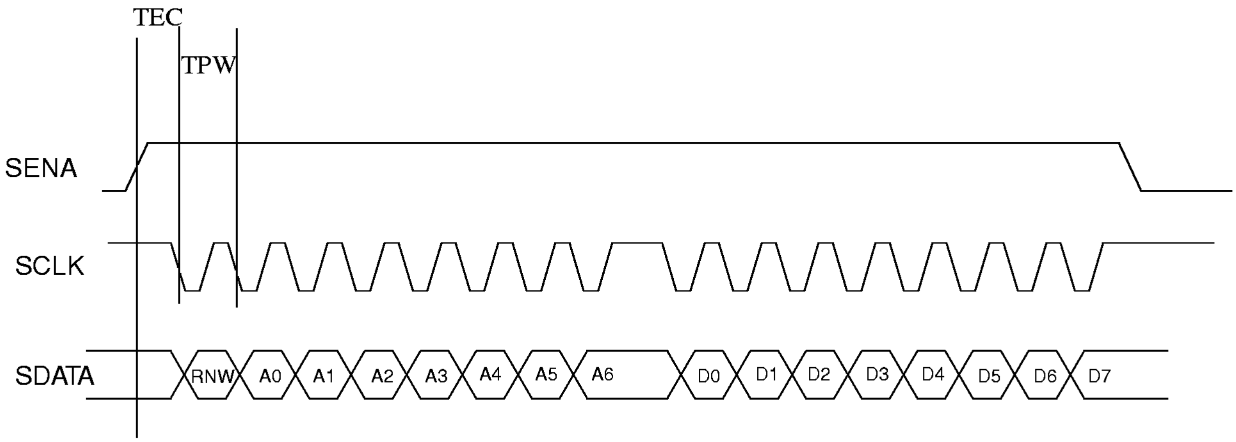


Table 30. Pin List

Pin #	Pin Name	Type	Description
1	CAGC	Passive	External capacitor for AGC loop
2	HOLD	Digital Input	Puts the AGC in loop into a hold or coast mode
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	RFP	Analog Input	High-speed signal input
10	RFN	Analog Input	High-speed signal input
11	VSS1	0V Supply	AGC/Bandgap Ground
12	NC		
13	NC		
14	VDD1	+3.3V Supply	AGC/Bandgap Supply
15	REXT	Passive	Passive
16	TRCST	Digital Input	Put TR charge pump in high impedance mode
17	TRTP1P	Diff Output	Timing Recovery Test Output 1
18	TRTP1N	Diff Output	Timing Recovery Test Output 1
19	TRTP2P	Diff Output	Timing Recovery Test Output 2
20	TRTP2N	Diff Output	Timing Recovery Test Output 2
21	VSS3	0 V Supply	DC Restore/Timing Recovery Ground
22	VDD3	+3.3V Supply	DC Restore/Timing Recovery Supply

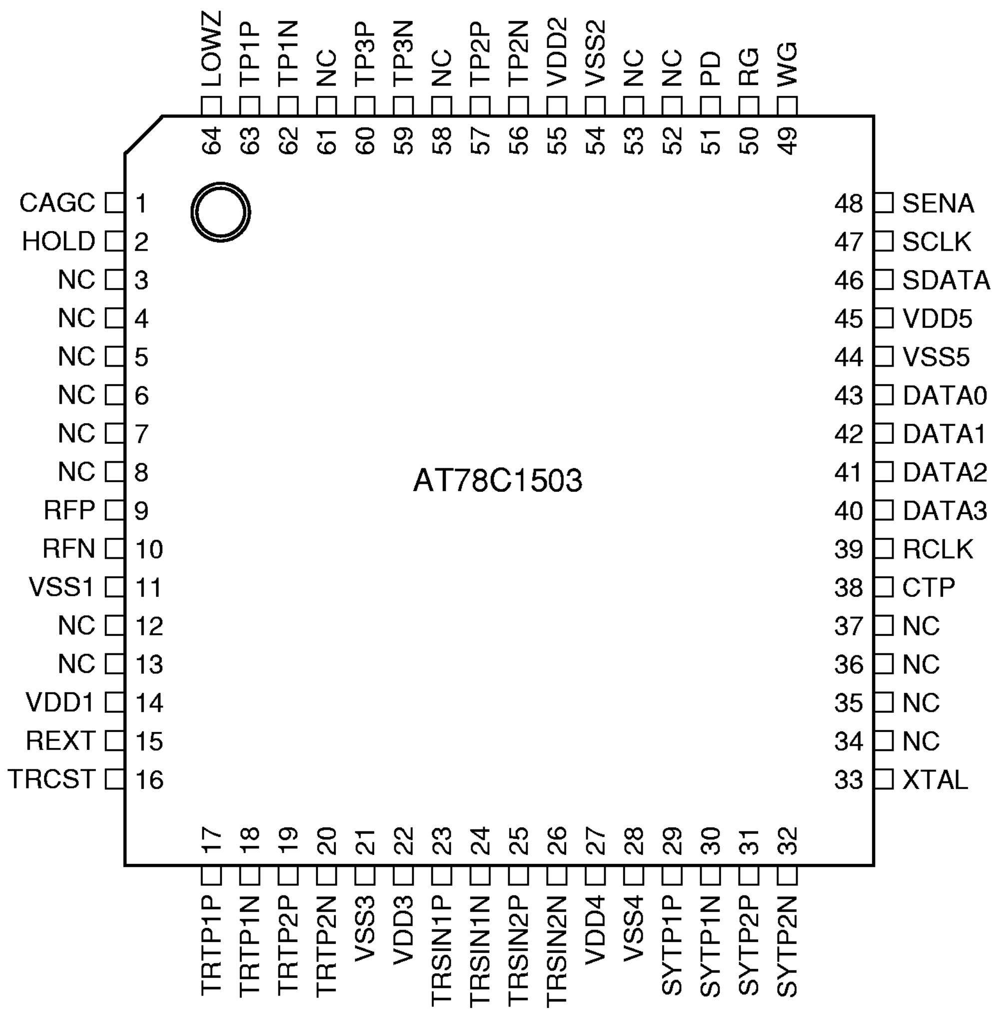
Table 30. Pin List

Pin #	Pin Name	Type	Description
23	TRSIN1P	Diff Input	Timing Recovery Test Input 1
24	TRSIN1N	Diff Input	Timing Recovery Test Input 1
25	TRSIN2P	Diff Input	Timing Recovery Test Input 2
26	TRSIN2N	Diff Input	Timing Recovery Test Input 2
27	VDD4	+3.3V Supply	Synthesizer Supply
28	VSS4	0V Supply	Synthesizer Ground
29	SYTP1P	Diff Output	Synthesizer Test Output 1
30	SYTP1N	Diff Output	Synthesizer Test Output 1
31	SYTP2P	Diff Output	Synthesizer Test Output 2
32	SYTP2N	Diff Output	Synthesizer Test Output 2
33	XTAL	Passive	26.16 MHz crystal connection
34	NC		
35	NC		
36	NC		
37	NC		
38	CTP	Digital Output	CMOS Test Output
39	RCLK	Output	Recovered clock out
40	DATA[3]	Output	Recovered data out, Bit 3 (first in time)
41	DATA[2]	Output	Recovered data out, Bit 2
42	DATA[1]	Output	Recovered data out, Bit 1
43	DATA[0]	Output	Recovered data out, Bit 0 (last in time)
44	VSS5	0V Supply	Digital CMOS Ground
45	VDD5	+3.3V Supply	Digital CMOS Supply
46	SDATA	Input/Output	Serial data, input (write data) or output (read data)
47	SCLK	Input	Serial data clock
48	SENA	Input	Serial data enable, must be high to read or write serial registers
49	WG	Input	Write Gate
50	RG	Input	Read Gate
51	PD	Input	Power down
52	NC		
53	NC		
54	VSS2	0V Supply	Lowpass Filter/Analog Test Supply
55	VDD2	+3.3V Supply	Lowpass Filter/Analog Test Ground
56	TP2N	Diff Output	Test Point 2 output
57	TP2P	Diff Output	Test Point 2 output
58	NC		

Table 30. Pin List

Pin #	Pin Name	Type	Description
59	TP3N	Diff Output	Test Point 3 output
60	TP3P	Diff Output	Test Point 3 output
61	NC		
62	TP1N	Diff Output	Test Point 1 output
63	TP1P	Diff Output	Test Point 1 output
64	LOWZ	Digital Input	Low Z Control for AGC Input

Figure 14. Chip Pin Out



Test Procedures

Synthesizer

Divide by x (x = 1 - 7) counter. This counter has two distinct modes. If the DVDX serial register equals zero or one, the clock is mux'd directly to TC (i.e. the input clock is mux'd directly to the output) and R_SYNDIV has no effect. Otherwise, after R_SYNDIV (reset synthesizer divider) is deasserted, TC (terminal count) will stay low for seven clock cycles and then go true on the falling clock edge after seven rising clock edges. After this, TC will go true for one clock cycle every x clock cycles, where x is the value of the DVDX register. TC always changes state on the falling edge of the clock.

TR Test Charge Pump Currents

Some of the following registers and tests depend on whether the part is in acquisition or tracking mode. You can monitor which mode the part is in by looking at the digital test point, #2 on pin CTP. Acquisition mode starts when RG goes high and last for four times the number programmed in serial register 11 (ACQ_CNT) number of clock cycles on the TRVCO input to the TR phase detector.

Set PLL loop filter so all capacitors are out of circuit (i.e. the filter is open). Serial registers 13 (acquisition mode) and 14 (tracking mode). Set the five LSBs in each of these registers to zeros.

Select FLTU (loop filter unbuffered as test output) TRTP2, 4. Measure charge pump currents at this test point.

The phase detector has serial register bits which can set the PU and PD signals to the charge pump, TRS_PU and TRS_PD.

Reset phase detector so both PU and PD are low: TRR_PUPD in serial register 17, bit 1.

Put the part in Read mode by raising the RG pin. Set the PU signal by using the serial register bit TRS_PU. You can monitor the TR PU and PD signals on TRTP1, 0 and TRTP2, 0. To test the TR PU current, only the TR PU output should be true.

The various serial register bits that control charge pump currents can be tested at this time. These include <5:0> bits in serial register 15: ACQ_CPI, TRK_CPI and TRKCP.

When the PU currents have been tested, pulse TRR_PUPD to clear the PU signal. Then set the PU signal by using the serial register bit TRS_PD. This will put the charge pump into PD mode. You can monitor the PD signal as described above. Measure the PD current.

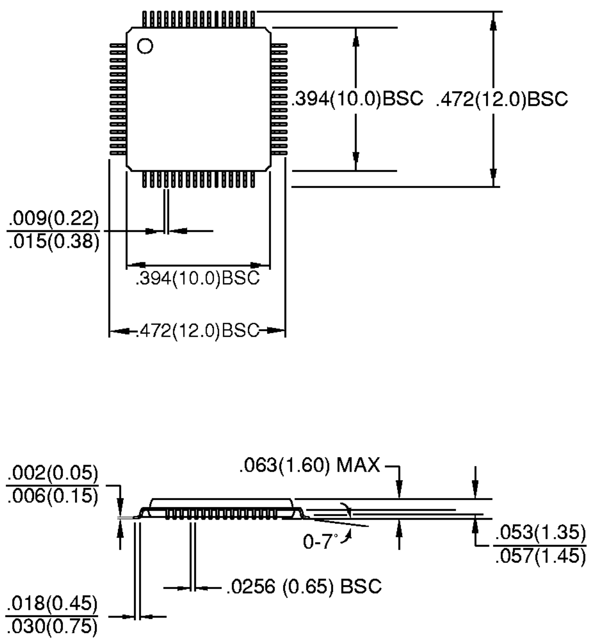
Ordering Information

Ordering Code	Package	Operation Range
AT78C1503-64TC	64 Pin TQFP	Commercial (0°C to 70°C)

Package Type	
64T	64-Lead Thin Quad Flat Pack (TQFP)

Packaging Information

64T, 64-Lead, Thin Quad Flat Pack (TQFP)
Dimensions in Inches and (Millimeters).



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