Signetics

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Status	Product Specification
FAST Products	

FAST 74F195
Shift Register

4-Bit Parallel-Access Shift Register

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195	115MHz	45mA

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Shift right and parallel load capability**
- **J - $\overline{K}$(D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F195 is a 4-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$

ORDERING INFORMATION

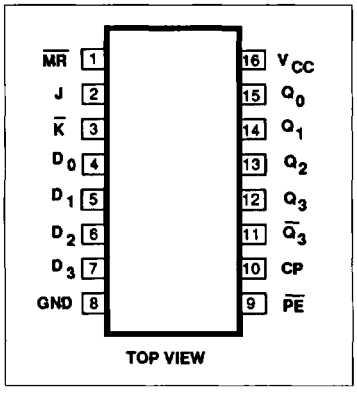
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F195N
16-Pin Plastic SO	N74F195D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/0.033	20μA/20μA
J, $\overline{K}$	J - K or D type serial inputs	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel Enable input	1.0/0.033	20μA/20μA
CP	Clock Pulse input (Active rising edge)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (Active Low)	2.0/0.066	40μA/40μA
Q_0 - Q_3, $\overline{Q}_3$	Data outputs	50/33	1.0mA/20mA

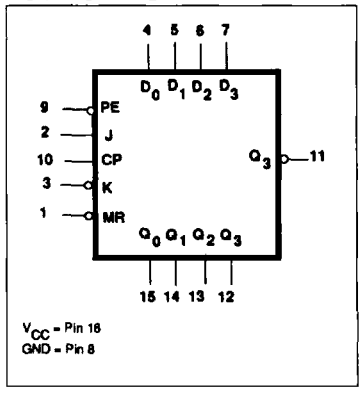
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

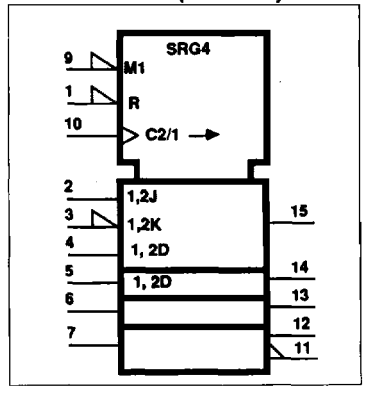


TOP VIEW

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	$\overline{PE}$ mode	Waveform 1	120	130		110		MHz
		Toggle mode		100	115		90		
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	9.5 9.0	4.0 4.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_3$		Waveform 1	7.0 4.5	10.0 7.0	13.0 9.0	7.0 4.0	13.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 2	5.0	7.5	10.5	5.0	11.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_3$		Waveform 2	7.0	10.0	13.5	7.0	14.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	3.0 4.0			3.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_w(H)$	CP Pulse width High	Waveform 1	6.0			6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	6.0			6.0		ns