128-bit THERMAL HEAD DRIVER S-4670A

The S-4670A is a CMOS thermal head driver containing 128-bit (64 x 2) shift registers and latches. High speed operation at 16 MHz clock frequency together with 2-divisible shift registers driven in each 64 bits makes the S-4670A best for applications such as video printers and graphic thermal print heads

■ FEATURES

- ♦ Low current consumption: 0.6 mA typ. (fclk = 4 MHz; the SI pin is fixed)
- ♦ High speed operation:
  16 MHz max. (a single die)
  16 MHz max. (cascade connection)
- ♦ Driver–OFF function when supply voltage drops.
- ♦ [64 bits x 2/128 bits x 1] shift register switching function
- ♦ Driver output withstand voltage: 36 V max.
- ♦ Driver output current: 15 mA typ.
- ♦ 128-bit shift registers and latches are built in.
- ♦ 1-division driver enable function at 128 bits
- ♦ 2-division driver enable function at every 64 bits

■ BLOCK DIAGRAM

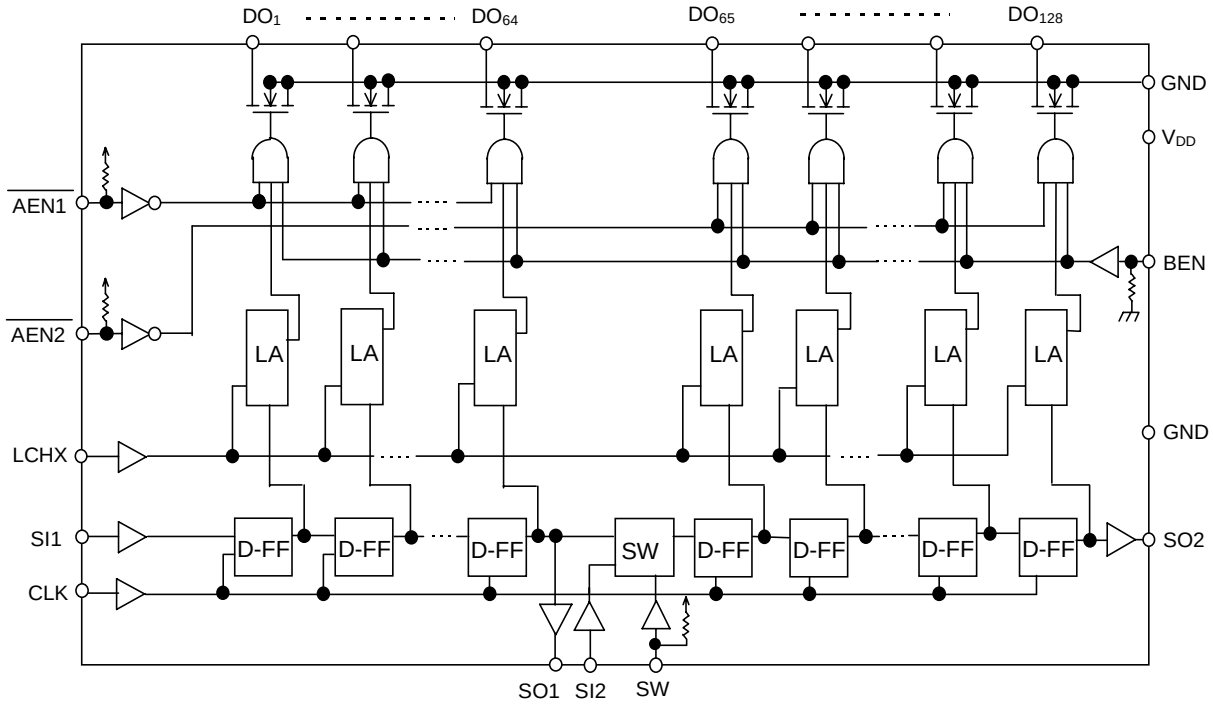


Figure 1 Block Diagram

■ OPERATION

When the SW pin is at “L” level, the shift register reads data, which is input in the SI1 pin at the rising edge of the clock input, in bits 1 through 128 of the shift register. Fix the SI2 pin when not in use to GND or VDD.

When the SW pin is at “H” level or open, the shift register reads data which is input in the SI1 or SI2 pin at the rising edge of the clock input. Data at the SI1 pin is read in bits 1 through 64 of the shift register; data at the SI2 pin is read in bits 65 through 128 of the shift register.

The latch circuit reads data of the shift register when the LCHX pin is at “L” level, and retains the preceding data of the shift register when the LCHX pin is at “H” level.

The latch data is output to the driver when pins $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ are at “L” level and the BEN pin is at “H” level. The driver output transistor is turned ON and OFF when the latch data is at “H” level and at “L” level, respectively. All driver output transistors to be controlled are turned OFF by setting pins $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ to "H" level or the BEN pin to "L” level.

The $\overline{\text{AEN1}}$ pin, $\overline{\text{AEN2}}$ pin and BEN pin control the driver output bits 1 through 64, 65 through 128 and 1 through 128, respectively.

While the power voltage is transiting from 0 to 5 V and vice versa, the driver output transistors are forcibly turned OFF.

■ DESCRIPTION OF PINS

Note: For pin assignment, refer to Figure 3, "Outline and Dimensions."

Table 1 Description of Pins

No.	Name	Description
1 to 128	DO1 to DO128	Driver output pins (Nch open-drain output)
142, 148	SO1, SO2	Serial data output pin for 64 bits × 2 shift registers
141	BEN	Driver enable input pin; Outputs the latch data (DO1 through DO128) to the driver when the BEN is at "H" level (a pull-down resistor with Rp =300 kΩ typ. is built in).
129 to 136	GND	GND pin (0 V)
139, 147	VDD	Positive power supply pin (+5 V)
140 146	$\overline{\text{AEN1}}$ $\overline{\text{AEN2}}$	Driver enable input pins: The $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ output the latch data (DO1 through DO64 and DO65 through DO128, respectively) to the driver when $\overline{\text{AEN1}}$ or $\overline{\text{AEN2}}$ is at "L" level (a pull-up resistor with Rp =300 kΩ typ. is built in).
145	LCHX	Data latch signal input pin: LCHX = "L": Reads data of the shift register. LCHX = "H": Retains the preceding data.
138	CLK	Clock input pin of the 64 bits x 2 shift register
143	SW	64 bits x 2/128 bits x 1 shift register switching input pin (a pull-up resistor with Rp =300 kΩ typ. is built in). SW = "H" or open: 64 bits x 2 shift register SW = "L": 128 bits x 1 shift register Input from the SI2 is not available.
137 144	SI1 SI2	Serial data input pin of the 64 bits x 2 shift register. Input conditions can be selected by the SW pin: SW = "H" or open: SI1 = Serial data input pin for DO1 through DO64 SI2 = Serial data input pin for DO65 through DO128 SW = "L": SI1 = Serial data input pin for DO1 through DO128. Fix the SI2 pin to GND or VDD.

■ ABSOLUTE MAXIMUM RATINGS

Table 2 Absolute Maximum Ratings

Name	Symbol	Standard	Unit
Power Supply Voltage	GND to V_{DD}	-0.4 to 7.0	V
Driver Output Withstand Voltage	V_{DOH}	36	V
Driver Output Current	I_{DOL}	24	mA
Input Voltage	VIN	GND -0.5 to V_{DD}+0.5	V
Output Voltage	VOUT	GND -0.5 to V_{DD}+0.5	V
Maximum Junction Temperature	Tjmax	125	°C
Operating Temperature Range	Topr	-10 to +80	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■ DC ELECTRICAL CHARACTERISTICS

Table 3 DC Electrical Characteristics

V_{DD} = 5.0 V ± 10%, Ta = -10 to +80 °C unless otherwise specified

Name	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Driver High Output Voltage	V_{DOH}	Heater resistance: RL= 2 kΩ min.		24	28	V
		Heater resistance: RL= 5 kΩ min.			32	
High Level Input Voltage	V_{IH}	CLK: f_{CLK} = fmax duty 50% T_{SUD} = T_{HD} = 100 nsec SI1, SI2: f_{SI} = 1/2 fmax	0.8 V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}	LCHX: T_{WLA} = 100 nsec $\overline{AEN1}$, $\overline{AEN2}$, BEN, SW: DC level	GND		0.2 V_{DD}	V
High Level Input Current	I_{IH}	BEN Note1 V_{IH} = V_{DD}		17	55	µA
		Other pins excl. BEN V_{IH} = V_{DD}			0.5	µA
Low Level Input Current	I_{IL}	$\overline{AEN1}$, $\overline{AEN2}$, SW Note2 V_{IL} = GND	-55	-17		µA
		Other pins excl. $\overline{AEN1}$, $\overline{AEN2}$, SW V_{IL} = GND	-0.5			µA
High Level Output Voltage	V_{OH}	SO1, SO2 I_{OH} = -0.5 mA	4.1			V
Low Level Output Voltage	V_{OL}	SO1, SO2 I_{OL} = 0.5 mA			0.4	V
Driver Low Output Voltage	V_{DOL}	V_{DD} = 5.0 V I_{OL} = 15 mA		0.8	1.6	V
Driver Leakage Current	I_{LEAK}	V_{DOH} = 28 V			1.0	µA
Current Consumption	I_{DD}	f_{CLK} = 4 MH_Z SI1, SI2: fixed; SW: open		0.6	1.5	mA
		f_{CLK} = 4 MH_Z SI1, SI2: HLHL; SW: open		2.2	3.5	mA
Current Consumption During Standby	I_S	CLK, LCHX: GND; Other input pins: open SI1, SI2: fixed		0.1	0.3	mA
Low Power Supply Voltage Detecting Circuit	V_{DET}		0.8	2.8	4.0	V

Note1 A pull-down resistor is built in.
Note2 A pull-up resistor is built in.

■ AC ELECTRICAL CHARACTERISTICS

Table 4 AC Electrical Characteristics

V_{DD} = 5.0 V ± 10%, Ta = -10 to +80 °C unless otherwise specified

Name	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK Pulse Width	T_{WCLK}	$V_{IH} = V_{DD}$, V_{IL} = 0 V; Rising and falling edges at 10 nsec or lower; Output load RL = 1 MΩ CL = 3 pF	30	—	—	nsec
Data Setup Time	T_{SUD}		20	—	—	nsec
Data Hold Time	T_{HD}		20	—	—	nsec
Latch Pulse Width	T_{WLA}		30	—	—	nsec
Latch Setup Time	T_{SULA}		30	—	—	nsec
Latch Hold Time	T_{HDLA}		30	—	—	nsec
CLK-SO Propagation Delay Time	T_{DSO}		—	25	40	nsec
EN-D0n Propagation Delay Time	T_{DDO}	V_{DOH} = 24 V RL = 3000 Ω	—	—	1.0	µsec
D0n Rising Time	T_{RDO}	V_{DOH} = 24 V RL = 3000 Ω	—	80	200	nsec
D0n Falling Time	T_{FDO}	V_{DOH} = 24 V RL = 3000 Ω	—	80	200	nsec
Clock Frequency	f_{CLK}	Single die	—	—	16	MHz
		Cascade connection	—	—	16	MHz

■ TIMING CHART

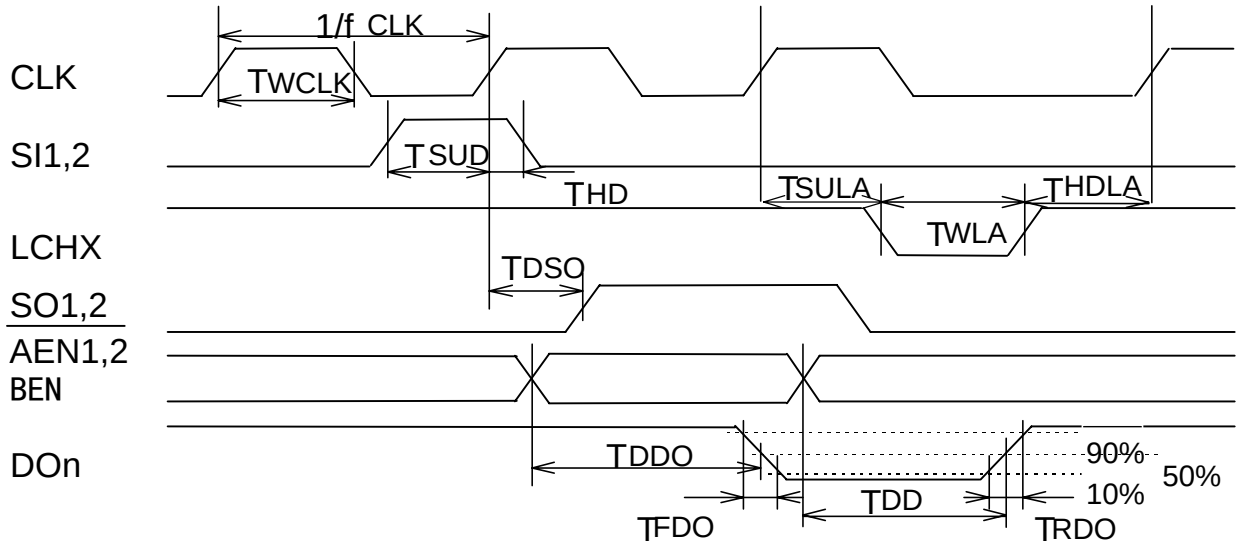


Figure 2 Timing Chart

■ QUALITY STANDARD

Table 5 Reliability Assessment Testing Specifications

No.	Test Item	Testing Conditions	Test Time or Frequency	LTFR
1	High Temperature and High Humidity Bias	Ta = 85 °C, RH = 85 %, Vabs. Max [Note 1] × 0.9	1000 h	10%
2	High Temperature Bias	Ta = 125 °C, Vabs. max [Note1] × 0.9	1000 h	10%
3	High Temperature Operation	Ta = 125 °C Vopr. max [Note2]	1000 h	10%
4	Static Electricity Resistance	C = 200 pF, V = 200 V, V_{SS} (or GND), V_{DD} (or V_{CC}) as reference; Positive/Negative	Once	-
5	Latch-up	V =±100 V, C = 200 pF, V = Vopr. max [Note2]	Once	-

[Note1] Vabs. max : Absolute maximum rating
[Note2] Vopr. max : Maximum operating voltage

Remark: Test samples are encapsuled in standard ceramic packages (resin is coated at humidity resistance test).

■ COORDINATES AND DIMENSIONS

Table 6-1 Pad Coordinates

Remark: The origin is at the center of the die.

No.	Pin name	Coordinates	No.	Pin name	Coordinates
1	DO1	(-3683.0 , 218.5)	43	DO43	(-1247.0 , 218.5)
2	DO2	(-3625.0 , 317.5)	44	DO44	(-1189.0 , 317.5)
3	DO3	(-3567.0 , 218.5)	45	DO45	(-1131.0 , 218.5)
4	DO4	(-3509.0 , 317.5)	46	DO46	(-1073.0 , 317.5)
5	DO5	(-3451.0 , 218.5)	47	DO47	(-1015.0 , 218.5)
6	DO6	(-3393.0 , 317.5)	48	DO48	(-957.0 , 317.5)
7	DO7	(-3335.0 , 218.5)	49	DO49	(-899.0 , 218.5)
8	DO8	(-3277.0 , 317.5)	50	DO50	(-841.0 , 317.5)
9	DO9	(-3219.0 , 218.5)	51	DO51	(-783.0 , 218.5)
10	DO10	(-3161.0 , 317.5)	52	DO52	(-725.0 , 317.5)
11	DO11	(-3103.0 , 218.5)	53	DO53	(-667.0 , 218.5)
12	DO12	(-3045.0 , 317.5)	54	DO54	(-609.0 , 317.5)
13	DO13	(-2987.0 , 218.5)	55	DO55	(-551.0 , 218.5)
14	DO14	(-2929.0 , 317.5)	56	DO56	(-493.0 , 317.5)
15	DO15	(-2871.0 , 218.5)	57	DO57	(-435.0 , 218.5)
16	DO16	(-2813.0 , 317.5)	58	DO58	(-377.0 , 317.5)
17	DO17	(-2755.0 , 218.5)	59	DO59	(-319.0 , 218.5)
18	DO18	(-2697.0 , 317.5)	60	DO60	(-261.0 , 317.5)
19	DO19	(-2639.0 , 218.5)	61	DO61	(-203.0 , 218.5)
20	DO20	(-2581.0 , 317.5)	62	DO62	(-145.0 , 317.5)
21	DO21	(-2523.0 , 218.5)	63	DO63	(-87.0 , 218.5)
22	DO22	(-2465.0 , 317.5)	64	DO64	(-29.0 , 317.5)
23	DO23	(-2407.0 , 218.5)	65	DO65	(29.0 , 218.5)
24	DO24	(-2349.0 , 317.5)	66	DO66	(87.0 , 317.5)
25	DO25	(-2291.0 , 218.5)	67	DO67	(145.0 , 218.5)
26	DO26	(-2233.0 , 317.5)	68	DO68	(203.0 , 317.5)
27	DO27	(-2175.0 , 218.5)	69	DO69	(261.0 , 218.5)
28	DO28	(-2117.0 , 317.5)	70	DO70	(319.0 , 317.5)
29	DO29	(-2059.0 , 218.5)	71	DO71	(377.0 , 218.5)
30	DO30	(-2001.0 , 317.5)	72	DO72	(435.0 , 317.5)
31	DO31	(-1943.0 , 218.5)	73	DO73	(493.0 , 218.5)
32	DO32	(-1885.0 , 317.5)	74	DO74	(551.0 , 317.5)
33	DO33	(-1827.0 , 218.5)	75	DO75	(609.0 , 218.5)
34	DO34	(-1769.0 , 317.5)	76	DO76	(667.0 , 317.5)
35	DO35	(-1711.0 , 218.5)	77	DO77	(725.0 , 218.5)
36	DO36	(-1653.0 , 317.5)	78	DO78	(783.0 , 317.5)
37	DO37	(-1595.0 , 218.5)	79	DO79	(841.0 , 218.5)
38	DO38	(-1537.0 , 317.5)	80	DO80	(899.0 , 317.5)
39	DO39	(-1479.0 , 218.5)	81	DO81	(957.0 , 218.5)
40	DO40	(-1421.0 , 317.5)	82	DO82	(1015.0 , 317.5)
41	DO41	(-1363.0 , 218.5)	83	DO83	(1073.0 , 218.5)
42	DO42	(-1305.0 , 317.5)	84	DO84	(1131.0 , 317.5)

Table 6-2 Pad Coordinates

No.	Pin name	Coordinates	No.	Pin name	Coordinates
85	DO85	(1189.0 , 218.5)	127	DO127	(3625.0 , 218.5)
86	DO86	(1247.0 , 317.5)	128	DO128	(3683.0 , 317.5)
87	DO87	(1305.0 , 218.5)	129	GND	(3248.0 , -38.0)
88	DO88	(1363.0 , 317.5)	130	GND	(2320.0 , -38.0)
89	DO89	(1421.0 , 218.5)	131	GND	(1392.0 , -38.0)
90	DO90	(1479.0 , 317.5)	132	GND	(464.0 , -38.0)
91	DO91	(1537.0 , 218.5)	133	GND	(-464.0 , -38.0)
92	DO92	(1595.0 , 317.5)	134	GND	(-1392.0 , -38.0)
93	DO93	(1653.0 , 218.5)	135	GND	(-2320.0 , -38.0)
94	DO94	(1711.0 , 317.5)	136	GND	(-3248.0 , -38.0)
95	DO95	(1769.0 , 218.5)	137	SI1	(-2898.0 , -319.0)
96	DO96	(1827.0 , 317.5)	138	CLK	(-2756.0 , -319.0)
97	DO97	(1885.0 , 218.5)	139	VDD	(-2065.0 , -292.0)
98	DO98	(1943.0 , 317.5)	140	$\overline{\text{AEN1}}$	(-1672.0 , -319.0)
99	DO99	(2001.0 , 218.5)	141	BEN	(-866.0 , -319.0)
100	DO100	(2059.0 , 317.5)	142	SO1	(-105.0 , -319.0)
101	DO101	(2117.0 , 218.5)	143	SW	(184.0 , -319.0)
102	DO102	(2175.0 , 317.5)	144	SI2	(1069.0 , -319.0)
103	DO103	(2233.0 , 218.5)	145	LCHX	(1695.0 , -319.0)
104	DO104	(2291.0 , 317.5)	146	$\overline{\text{AEN2}}$	(2040.0 , -319.0)
105	DO105	(2349.0 , 218.5)	147	VDD	(2610.0 , -292.0)
106	DO106	(2407.0 , 317.5)	148	SO2	(2838.0 , -319.0)
107	DO107	(2465.0 , 218.5)			
108	DO108	(2523.0 , 317.5)			
109	DO109	(2581.0 , 218.5)			
110	DO110	(2639.0 , 317.5)			
111	DO111	(2697.0 , 218.5)			
112	DO112	(2755.0 , 317.5)			
113	DO113	(2813.0 , 218.5)			
114	DO114	(2871.0 , 317.5)			
115	DO115	(2929.0 , 218.5)			
116	DO116	(2987.0 , 317.5)			
117	DO117	(3045.0 , 218.5)			
118	DO118	(3103.0 , 317.5)			
119	DO119	(3161.0 , 218.5)			
120	DO120	(3219.0 , 317.5)			
121	DO121	(3277.0 , 218.5)			
122	DO122	(3335.0 , 317.5)			
123	DO123	(3393.0 , 218.5)			
124	DO124	(3451.0 , 317.5)			
125	DO125	(3509.0 , 218.5)			
126	DO126	(3567.0 , 317.5)			

* Pad size is 80μm by 80μm

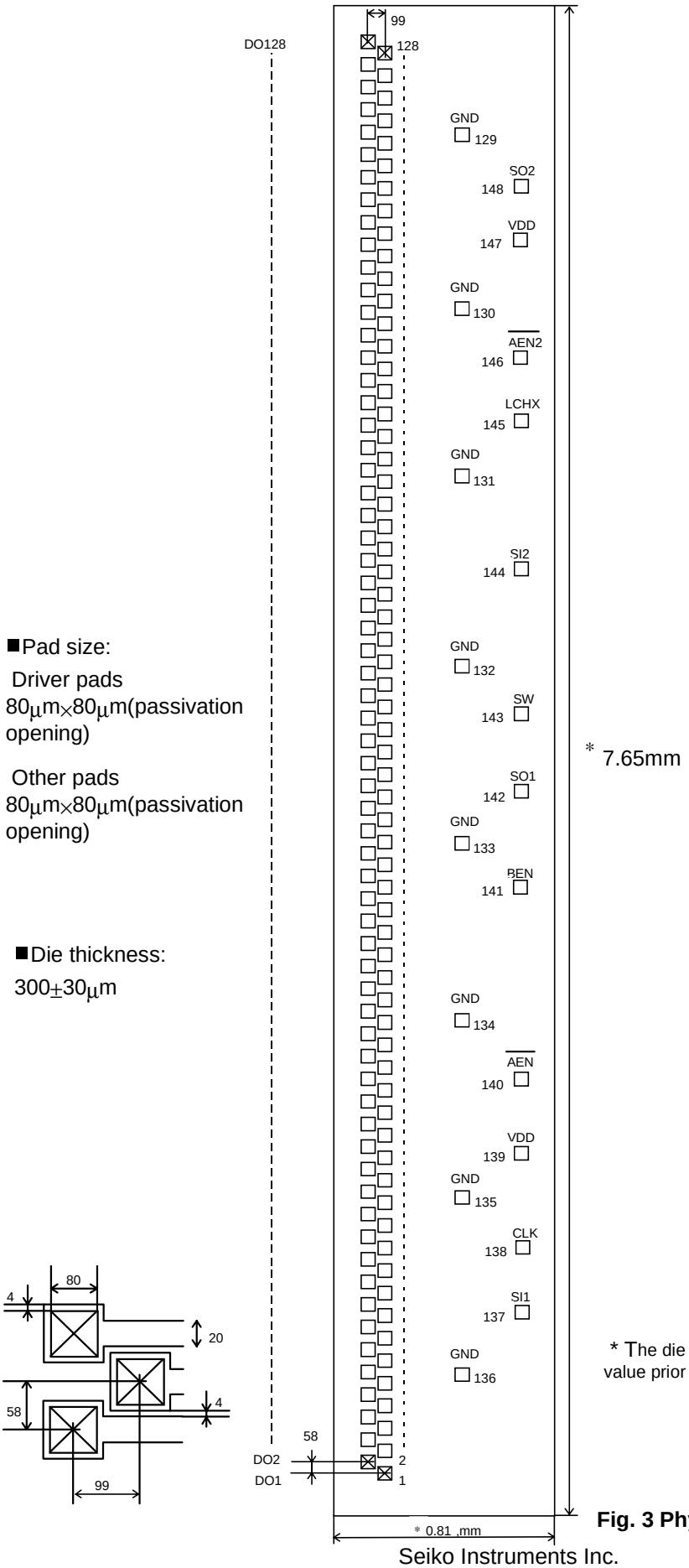
■Pad size:

Driver pads
80μm×80μm(passivation opening)

Other pads
80μm×80μm(passivation opening)

■Die thickness:

300±30μm



* The die size used here is the value prior to dicing.

Fig. 3 Physical Dimensions

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