SP9685

ULTRA FAST COMPARATOR

The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and -5.2V rails. It is pin and voltage compatible with AD9685.

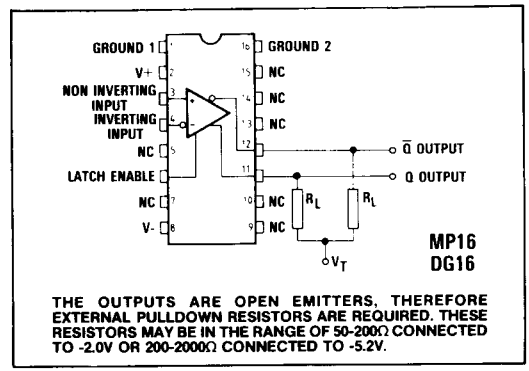

Fig.1 DIL pin connections (top view) and function diagram

FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- Supply +5V, -5.2V (±0.25V)
- 50 ohm Line Driving Capability
- Excellent Common Mode Rejection
- Operating Temperature Range :
  SP9685 — -30°C to +85°C
  SP9685AC — -55°C to +125°C
- Pin Compatible with AD9685
- Pin Compatible with AM685 — But Faster

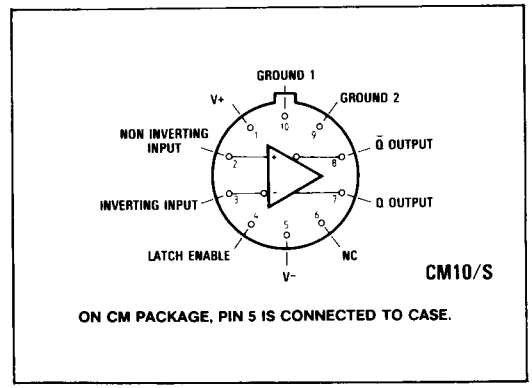

Fig.2 Metal package (CM10/S) pin connections (top veiw)

APPLICATIONS

- Ultra High Speed A/D Converter
- Ultra High Speed Line Receivers
- Peak Detectors
- Threshold Detectors

ORDERING INFORMATION

SP9685CM (Industrial - Cylindrical Metal package)
SP9685DG (Industrial - Ceramic DIL package)
SP9685BB DG (Plessey High Reliability Ceramic DIL package)
SP9685MP (Industrial - Miniature Plastic package)
SP9685AC DG (Military - Ceramic DIL package)

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

ABSOLUTE MAXIMUM RATINGS

Postive supply voltage	6V
Negative supply voltage	-6V
Output current	30mA
Input voltage	±3V
Differential input voltage	3.5V
Power dissipation	350mW

Storage temperature range	-55° C to +150° C
Operating junction temperature	<175° C
Lead temperature (soldering 60 sec)	300° C
Vibration	196m/s²
Shock	14700m/s² peak 0.5ms duration

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} 5.00V: V_{EE} = -5.2V: R_L 50Ω: V_T = 2.0V (see Fig.1)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	-5		+5	mV	Rs< 100Ω 25°C
	-7		+7	mV	Rs< 100Ω
Input bias current			20	μA	25°C
			30	μA	
Input offset current			5	μA	25°C
			8	μA	
Supply current I_{EE}			34	mA	25°C
			36	mA	
Supply current I_{CC}			23	mA	25°C
			24	mA	25°C
Total power dissipation	210		350	mW	25°C Note 3
Common mode range	-2.5		+2.5	V	
Output logic levels					
Output high	-0.96		-0.81	V	25°C
	-1.045		-0.875	V	T_{amb} = Min.
	-0.89		-0.70	V	T_{amb} = Max.
Output low	-1.85		-1.65	V	25°C
	-1.89		-1.65	V	T_{amb} = Min.
	-1.83		-1.575	V	T_{amb} = Max.
Min. latch set up time			1	ns	Notes 1, 2, 3 25°C
			2	ns	
Input to output delay			3	ns	Note 1, 3 (Q and $\overline{Q}$) 25°C
			4	ns	
Latch to output delay			3	ns	Notes 1, 2, 3 (Q and $\overline{Q}$) 25°C
			4.5	ns	
Minimum latch pulse width			3	ns	Note 3 25°C
Minimum hold time			1	ns	Note 3 25°C
Max. input capacitance		3		pF	Note 3 25°C
Input resistance	60		kΩ		Note 3 25°C
Common mode rejection ratio	70			dB	Note 3 25°C
Supply voltage rejection ratio	50			dB	Note 3 25°C

NOTES
1 -100mV pulse with -10mV overdrive
2 Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.
3 Guaranteed but not tested

Thermal characteristics

CM10	θ_{JA}	220°C/W
	θ_{JC}	65°C/W
DG16	θ_{JA}	120°C/W
	θ_{JC}	40°C/W
LC20	θ_{JA}	73°C/W
	θ_{JC}	22°C/W

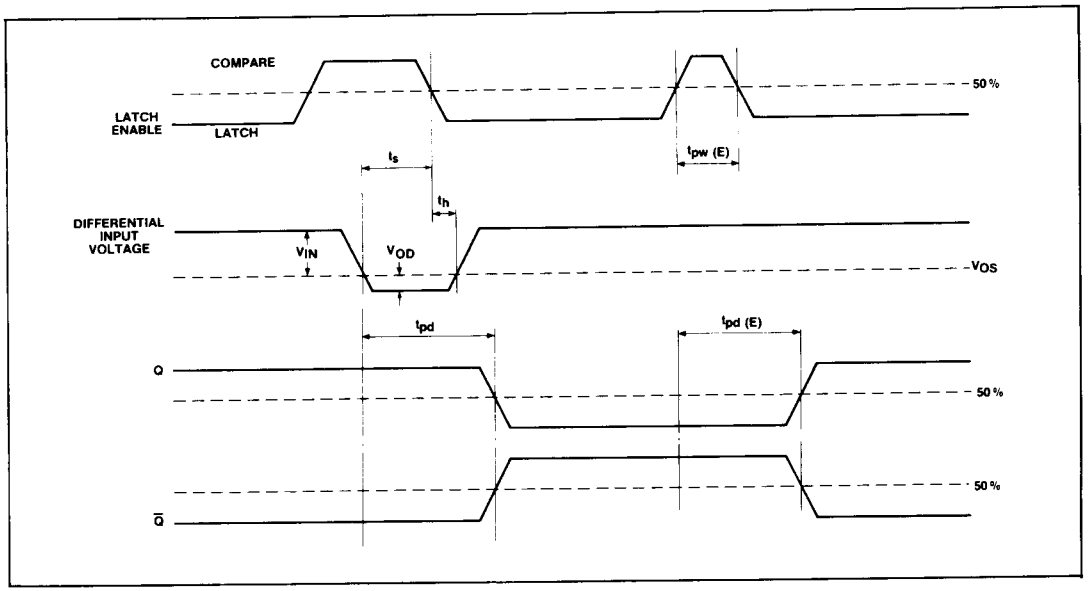

Fig.3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Measurement of propagation and latch delays

A simple test circuit is shown in Fig.4. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

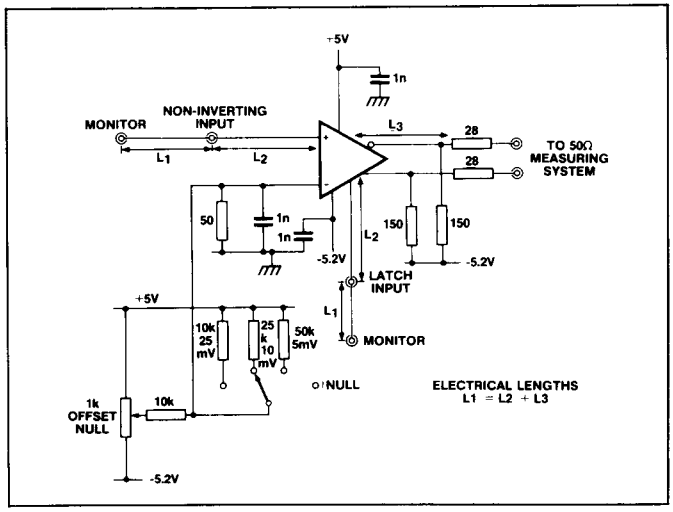

Fig.4 SP9685 test circuit

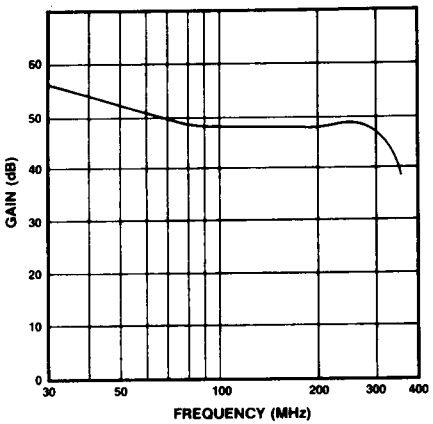

Fig.5 Open loop gain as a function of frequency

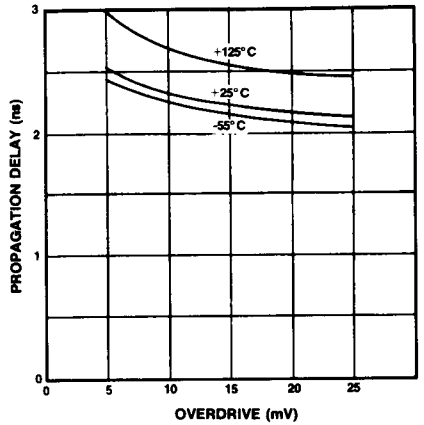

Fig.6 Propagation delay, latch to output as a function of overdrive

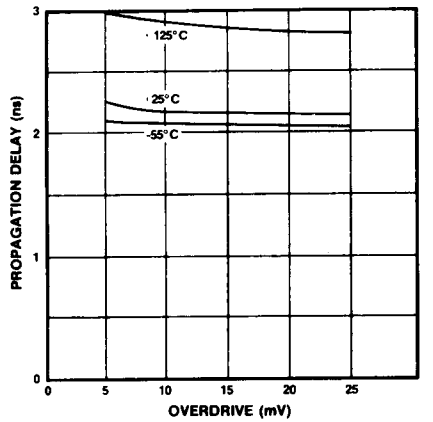

Fig.7 Propagation delay, input to output as a function of overdrive

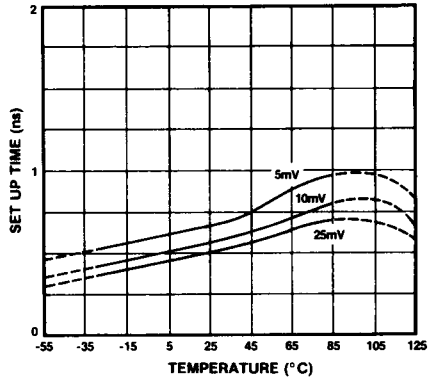

Fig.8 Set-up time as a function of temperature

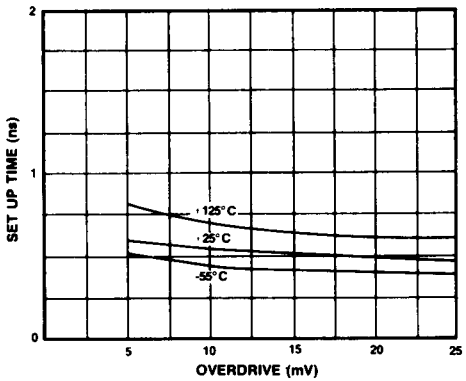

Fig.9 Set-up time as a function of input overdrive

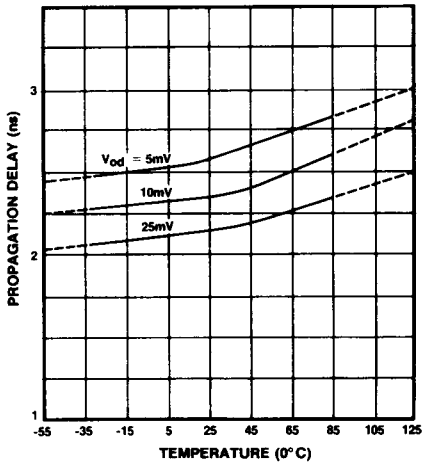

Fig.10 Propagation delay, input to output as a function of temperature

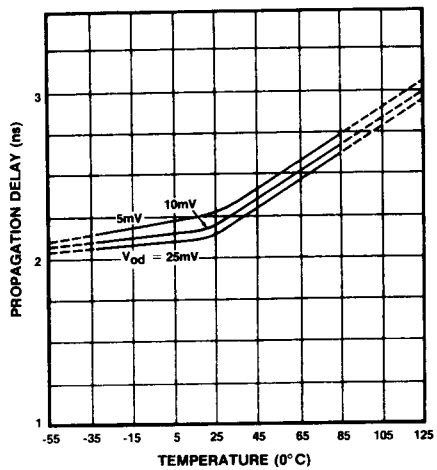

Fig.11 Propagation delay, latch to output as a function of temperature

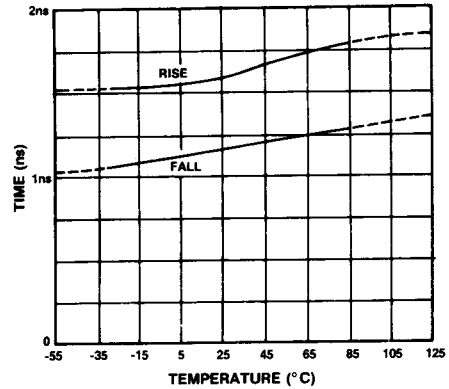

Fig.12 Output rise and fall times as a function of temperature

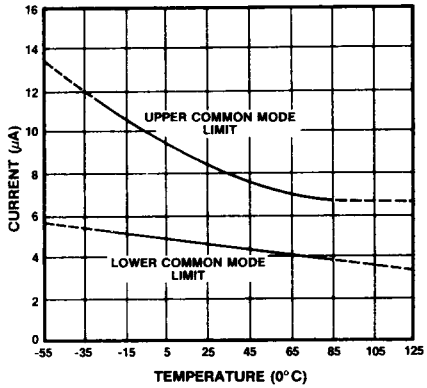

Fig.13 Input bias currents as a function of temperature

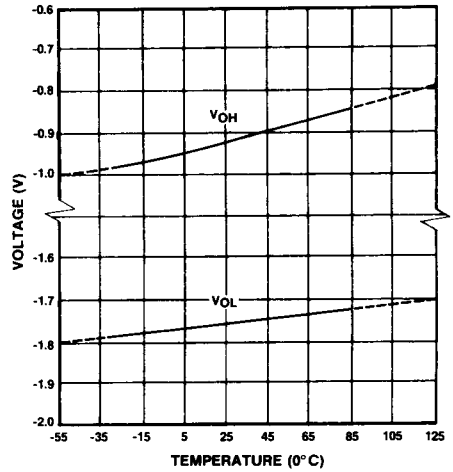

Fig.14 Output levels as a function of temperature

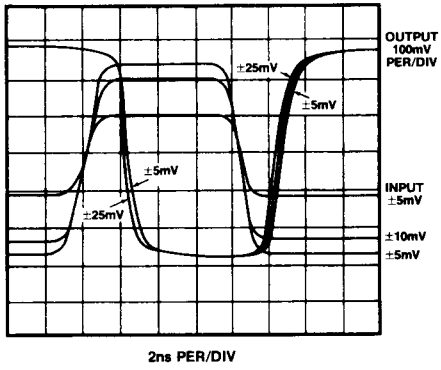

Fig.15 Response to various input signal levels