PBA 310 03/1
Dual Subscriber Interface Circuit (DSIC)

Description

The Ericsson module, DSIC (Dual Subscriber Interface Circuit) PBA 310 03/1, provides a low cost complete line interface between two separate analogue subscriber lines and a PCM highway.
PBA 310 03/1 is a member of the DSIC family, manufactured on an epoxy glass carrier, built up around two Ericsson FlexiSLIC™ circuits and an Ericsson dual CODEC/filter.
The DSIC family, a generic component with a fixed Single In Line pin-out, is easily accommodated for markets with various requirements.
The DSIC members provide Battery-, Ring relay-, Supervision-, Coding-, and market specific Hybrid- functions for two channels with only a minimum of external components.

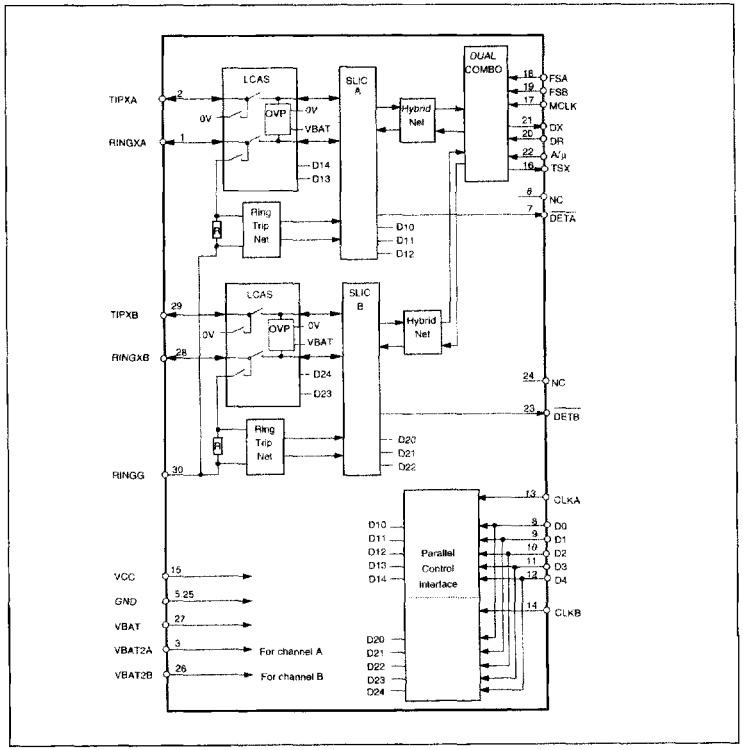

Figure 1. Block diagram.

Key Features

- In accordance with ITU-T, Q552.
- *Optimised for short line applications.*
- SIL (Single in Line) low profile module.
- Generic component with a fixed pin-out.
- On-hook transmission.
- Polarity reversal.
- Full longitudinal current capability during on-hook state.
- High and low battery feed with automatic switching (V_{BAT} and V_{BAT2}).
- Simple parallel control interface, 5 bit.
- Pin selectable A-law or μ-law companding.
- *Integrated ring relays.*
- Ring Trip net included.

Key Data

- 600Ω nominal impedance (Z_N)
- 600Ω balance impedance (Z_B)
- L_i = 0 dBr, L_o = -7 dBr.
- Constant current feed 23.5mA.
- Only +5V required in addition to battery voltages.
- 190 mW total power dissipation, both channels active on hook @ V_{BAT} = -48V.
- 43V open loop voltage @ -48V battery feed.

Suggested Applications

- ADSL CPE
- HFC CPE
- WLL Line Cards
- Terminal Adapters
- CTI

(Refer to the last page regarding abbreviations)

Typical Dimensions

Length	3.0"	76.2 mm
Height (from PCB)	0.95"	24.0 mm
Pin spacing	0.1"	2.54 mm
Stand-off	0.03	0.8 mm
Building width:		
Primary side	0.12"	3.1 mm
Secondary side	0.09"	2.3 mm

The pins are intended for through-hole mounting with 1.1±0.1 mm hole diameter.

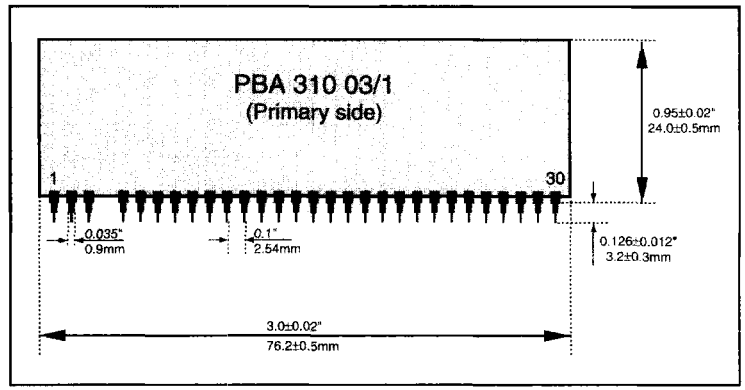

Figure 2. DSIC package, 30-pin SIL (Single In Line).

Pin Description

Pin	Symbol	Description
1	RINGXA	Channel A - RING lead from the subscriber line (two-wire)
2	TIPXA	Channel A -TIP lead from the subscriber line (two-wire)
3	VBAT2A	Second battery voltage for channel A – between GND and V_{BAT}
4		Omitted pin
5	GND	Ground - connected to pin 25 on the printed board
6	NC	
7	DET A	Loop/Ring detector output from channel A – active low
8	D0	*Digital control input 0 for both channels. (SLIC control input C1)*
9	D1	Digital control input 1 for both channels. (SLIC control input C2)
10	D2	Digital control input 2 for both channels. (SLIC control input C3)
11	D3	Digital control input 3 for both channels. (LCAS control input TSD)
12	D4	Digital control input 4 for both channels. (LCAS control input INPUT)
13	CLKA	Latch clock A - State of digital control inputs are latched to channel A
14	CLKB	Latch clock B - State of digital control inputs are latched to channel B
15	VCC	+5V power supply
16	TSX	Output indicating time slot transmission – low during transmission
17	MCLK	Master clock for PCM interface
18	FSA	Frame sync input for channel A
19	FSB	Frame sync input for channel B
20	DR	PCM receive data input for both channels
21	DX	PCM transmit data output for both channels
22	A/μ	Companding scheme selection - Logic '1' selects μ-law
23	DET B	Loop/Ring detector output from channel B – active low
24	NC	
25	GND	Ground - connected to pin 5 on the printed board
26	VBAT2B	Second battery voltage for channel B – between GND and V_{BAT}
27	VBAT	Battery supply voltage for both channels
28	RINGXB	Channel B - RING lead from the subscriber line (two-wire)
29	TIPXB	Channel B -TIP lead from the subscriber line (two-wire)
30	RINGG	Input from ringing generator for both channels

Operating States

The control signals consist of the data inputs D0-D4 and the clock inputs CLKA and CLKB

D0-D4 are common for both channels
CLKA is used to load D0-D4 for channel A
CLKB is used to load D0-D4 for channel B

The data is clocked on the positive edge of CLKA and CLKB.

The data inputs are used in the following way:

D0 Controls the C1 input on the SLIC circuits
D1 Controls the C2 input on the SLIC circuits
D2 Controls the C3 input on the SLIC circuits
D3 Controls the TSD (Thermal Shut Down) input on the LCAS circuits
D4 Controls the INPUT (Switch control) input on the LCAS circuits

Usage of the D0-D4 inputs is indicated in the table below.

D4	D3	D2	D1	D0	State/Definition
		0	0	0	**Open circuit.** SLIC circuit will be powered down as well as the TIPX and RINGX line drive amplifiers. High impedance is presented to the line.
		0	0	1	**Ringing state.** Ring trip detector indicating off hook with a logic low level at detector output.
		0	1	0	**Active state.** *Loop detector indicating off hook with logic low level at detector output.*
		0	1	1	**Not applicable.**
		1	0	0	**Not applicable.**
		1	0	1	**Not applicable.**
		1	1	0	**Active reverse.** Loop detector indicating off hook with logic low level at detector output.
		1	1	1	**Not applicable.**
0	1				**Idle / Talk state.** Line switches are closed and ring switches are open.
1	1				**Power ringing state**. *Ring switches are closed and line switches are open.*
1	0				**Hold state**. Ring return switch open and ringing access switch waiting for zero current open. This state should be kept for half the ring signal period.
0	0				**All off.** Zero current has occurred and ringing access switch has opened.

Table 2. Logical State and definition for the DSIC

Comments: Due to the zero current switching of the ringing signal there can be a delay from application of the D3, D4 input signals to the steady states that are described in the table above. This delay can be up to half the period time of the ringing signal (0.5T). To prevent loading of the ringing generator through the overvoltage protectors, the hold state should be kept as described in the table.

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Unit
Temperature					
Storage temperature		T_{stg}	-40	+110	°C
Operating temperature		T_{amb}	0	+70	°C
Power Supply					
V_{CC} with respect to GND		V_{CC}	-0.3	+6.5	V
V_{BAT} with respect to GND		V_{BAT}	-70	+0.4	V
V_{BAT2} with respect to GND		V_{BAT2}	V_{BAT}	+0.4	V
Ring Feed Resistors					
Ring Current RINGG to RINGX	Continuous	I_{RGRX}	-45	+45	mA_{RMS}
Ring Current RINGG to RINGX	200ms	I_{RGRXPP}	-100	+100	mA_{RMS}
TIPX and RINGX Terminals					
Voltage with respect to GND	Continuous	V_{TA}, V_{RA}	V_{BAT}	GND	V
Digital Inputs/Outputs					
Input Voltage (FSA, FSB, MCLK, DR, A/μ, CLKA, CLKB, D0-D4, TSX)		V_{IN}	-0.4	V_{CC}	V
Output Voltage (DX, DETA, DETB)	V_{OUT}		-0.4	V_{CC}	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Temperature					
Ambient temperature, Operating	T_{amb}	0		+70	°C
Ambient temperature, Test	T_{amb}		+23		°C
Power Supply					
Positive Supply Voltage with respect to Ground (GND)	V_{CC}	+4.75	+5.00	+5.25	V
Battery Voltage with respect to Ground (GND)	V_{BAT}	-56	-48	-32	V
Second Battery Voltage with respect to Ground (GND)	V_{BAT2}	-32		-24	V

Electrical Characteristics

Unless otherwise noted, the specification applies for T_{amb} = 0 to +70°C, $R_{F1} = R_{F2} = 50\Omega$ (refer to fig. 11), V_{CC} = 5V, V_{BAT} = -48V, V_{BAT2} = -24V, $R_L = 500\Omega$, $Z_N = 600\Omega$

Parameter	Ref. fig	Condition	Symbol	Min	Typ	Max	Unit
Power Dissipation		MCLK=2.048MHz					
Open circuit/Open circuit		Both ch. in Open Circuit State, CODEC in Power Down	P_{OO}		20	40	mW
Active/Active		Both ch. Active, CODEC Active $R_L = \infty$	P_{AA}		190	250	mW
Active/Active		Both ch. Active, CODEC Active $R_L = 500\Omega$	P_{AA}		680	750	mW
Power Supply Current							
V_{CC}		Both ch. Active			21.5	24	mA
V_{BAT}		Both ch. Active, $R_L < 550\Omega$ or $R_L = \infty$. Note 1.			2	4	mA
V_{BAT2}		Both ch. Active, (on-hook) $R_L = \infty$			0		mA
V_{BAT2}		Both ch. Active, (off-hook) $R_L < 550\Omega$			47	52	mA
V_{BAT} to V_{BAT2} Auto switch							
Loop Resistance			R_l	550	620		Ω
Power Supply Rejection Ratio (PSRR)							
V_{CC} to Analogue Interface	5	f =50 - 4000 Hz, Vn=100mV_{RMS}		25			dB
V_{BAT} to Analogue Interface	5	f =50 - 4000 Hz, Vn=100mV_{RMS}		25			dB
V_{BAT2} to Analogue Interface	5	f =50 - 4000 Hz, Vn=100mV_{RMS}		25			dB

Parameter	Ref. fig	Condition	Symbol	Min	Typ	Max	Unit
Digital Interface (TTL Levels)							
Input Low Voltage		D0-D4, CLKA, CLKB, FSA, FSB, MCLK, DR, A/μ	V_{IL}			0.8	V
Input High Voltage		D0-D4, CLKA, CLKB, FSA, FSB, MCLK, DR, A/μ	V_{IH}	2.0			V
Input Leakage Current		All inputs	I_{IL}, I_{IH}	-10		+10	μA
Input Capacitance		FSA, FSB, MCLK, DR, A/μ	C_I			5	pF
Input Capacitance		CLKA, CLKB	C_I			10	pF
Input Capacitance		D0-D4	C_I			20	pF
Output Low Voltage		DX, TSX I_O = 3.2 mA	V_{OL}			0.4	V
Output High Voltage		DX, -I_O = 3.2 mA	V_{OH}	2.4			V
Output Current		DX In Tri-state Mode and TSX	I_O	-10		+10	mA
Output Low Voltage		DETA, DETB, I_{OL} = 0.5 mA	V_{OL}			0.5	V
Internal pull-up resistor		DETA, DETB			5		kΩ
Battery Feed Characteristics							
Loop Current		R_L=500Ω		+21.0	+23.5	+26.0	mA
Loop Current Reversed		R_L=500Ω		-21.0	-23.5	-26.0	mA
Loop Voltage		Open Loop, V_{BAT} = -48V			+43		V
Loop Voltage Reversed		Open Loop, V_{BAT} = -48V			-43		V
Loop Current Detector							
Loop Resistance for Off-Hook Detection			R_L			1	kΩ
Loop Resistance for On-Hook Detection			R_I	10			kΩ
Off-Hook Detection Delay Time		R_L=1kΩ	t_{LD}			5	ms
Ring Trip Detector							
Off-Hook Detection Delay Time during Ringing		R_L=600Ω, Vbias=-24V	t_{RD}		<100	150	ms
Relative levels		Note 2, 3					
Transmit (A-D) &	6	Level = -10 dBm0	L_I	-0.5	0.0	+0.5	dBr
Receive (D-A)	7	Level = -10 dBm0	L_O	-7.5	-7.0	-6.5	dBr
Gain Tracking		Relative to 0 dBm0					
Transmit (A-D) &	6	-55dBm0 to -50dBm0		-1.6		+1.6	dB
Receive (D-A)	7	-50dBm0 to -40dBm0		-0.6		+0.6	dB
		-40dBm0 to +3dBm0		-0.3		+0.3	dB
Impedance unbalance		Note 4, 300 - 3400 Hz					
LCL	8	R_L = 500Ω		50	68		dB
	8	Open-loop		50	63		dB
Longitudinal current limit							
Current for each wire		Active state	I_{LOT}, I_{LOR}	10			mA_{RMS}
Return loss		Note 5, Z_N = 600Ω					
	9	300 Hz		18			dB
		500 - 2000 Hz		22			dB
		3400 Hz		18			dB
Terminal balance return loss		Note 5, Z_B = 600Ω					
TBRL	10	300 Hz		18			dB
		500 - 2500 Hz		22			dB
		3400 Hz		18			dB
Gain distortion with frequency		Gain relative to 1014 Hz					
Transmit (A-D) &	6	300 - 400 Hz		-1.00		+0.30	dB
Receive (D-A)	7	400 - 600 Hz		-0.75		+0.30	dB
		600 - 2400 Hz		-0.35		+0.30	dB
		2400 - 3000 Hz		-0.55		+0.30	dB
		3000 - 3400 Hz		-1.50		+0.30	dB

Parameter	Ref. fig	Condition	Symbol	Min	Typ	Max	Unit
Signal to Total Distortion		Sine wave: 1014Hz, Psoph. weighted					
Transmit (A-D) &	6	-45 dBm0		20			dB
Receive (D-A)	7	-40 dBm0		25			dB
		-30 dBm0		33			dB
		-20 to 0 dBm0		35			dB
Cross Talk		1014 Hz selective					
Transmit (A-D) FEXT						-70	dB
Receive (D-A) FEXT						-73	dB
Idle Channel Noise							
Transmit (A-D)	6					-65	dBm0p
Receive (D-A)	7					-70	dBm0p
Discrimination against out-of-band signals							
Transmit (A-D), In-band signal	6	Level = -25 dBm0, f = 4.6 - 72 kHz				-50	dBm0
Spurious out-of-band signals							
Receive (D-A), Out-of-band signal, 4.6 - 72kHz	7	Level = 0 dBm0, f = 300 - 3400 Hz				-25	dBm0
Intermodulation		2nd or 3rd order 4-tone: 857, 862, 1373 and 1388 Hz					
Transmit (A-D), In-band signal	6					-41	dBm0
Receive (D-A), In-band signal	7					-41	dBm0

Notes

1. For R_L higher than 550Ω, the total current supplied by V_{BAT} would be 56 mA.
2. By definition the relative level at the digital path = 0 dBr, (dBm value = dBm0 value + dBr value).
3. 0 dBm (1 mW) at the 2-wire interface (Z_N = 600Ω) corresponds to 775 mV at 1014 Hz.
4. For R_{F1} and R_{F2} with at least 2%matching, LCL will be 46 dB or better.
5. Rising log scale from 300 Hz to 500Hz and failing log scale from 2500 Hz to 3400 Hz.

Timing specification for Codec

Unless otherwise noted, the specification applies for T_{amb} = 0 to +70 °C, V_{CC} = 5V, MCLK = 2.048 MHz, V_{IH} = 2.0V, V_{IL} = 0.8V, V_{OL} = 0.4V and V_{OH} = 2.4V

Parameter	Ref. fig	Symbol	Min	Typ	Max	Unit
Frequency of Master Clock, MCLK	3	$1/T_{PM}$		2.048		MHz
Width of Master Clock High	3	t_{WMH}	195			ns
Width of Master Clock Low	3	t_{WML}	195			ns
Rise time of Master Clock	3	t_{RM}			40	ns
Fall time of Master Clock	3	t_{FM}			40	ns
Delay time to valid Data from FS or MCLK, which ever comes later, and Delay time from FS to Data Output disabled	4	t_{DZF}	20		165	ns
Delay time from MCLK Low to Data Output disabled	3	t_{DZC}	50		165	ns
Set-up time from DR Valid to MCLK Low	3	t_{SDM}	40			ns
Hold time from MCLK Low to DR Invalid	4	t_{HDM}	50			ns
Hold time from MCLK Low to Frame Sync	4	t_{HMF}	10			ns
Set-up time from Frame Sync to MCLK Low	4	t_{SFM}	70		T_{PM} -70	ns
Hold time from 3rd period of MCLK Low to Frame Sync	4	t_{HMFI}	90			ns
Delay time from MCLK High to Data Valid	3	t_{DMD}	0		170	ns
Set-up time from FS to MCLK Low	3	t_{SF}	80		T_{PM} -80	ns
Hold time from MCLK Low to FS Low	3	t_{HF}	100			ns
Delay time TSX Low	3	t_{XDP}	0		140	ns
Hold time for MCLK High to Frame Sync	3	t_{HOLD}	0			ns

Timing specification for parallel Control Interface

V_{CC} = 5V, V_{IH} = 2.0V, V_{IL} = 0.8V

Parameter	Ref. fig	Symbol	Min	Typ	Max	Unit
Clock pulse width HIGH or LOW		t_w	20			ns
Set-up time for D0-D4 to clock pulse		t_{su}	25			ns
Hold time for clock pulse to D0-D4		t_h	5			ns

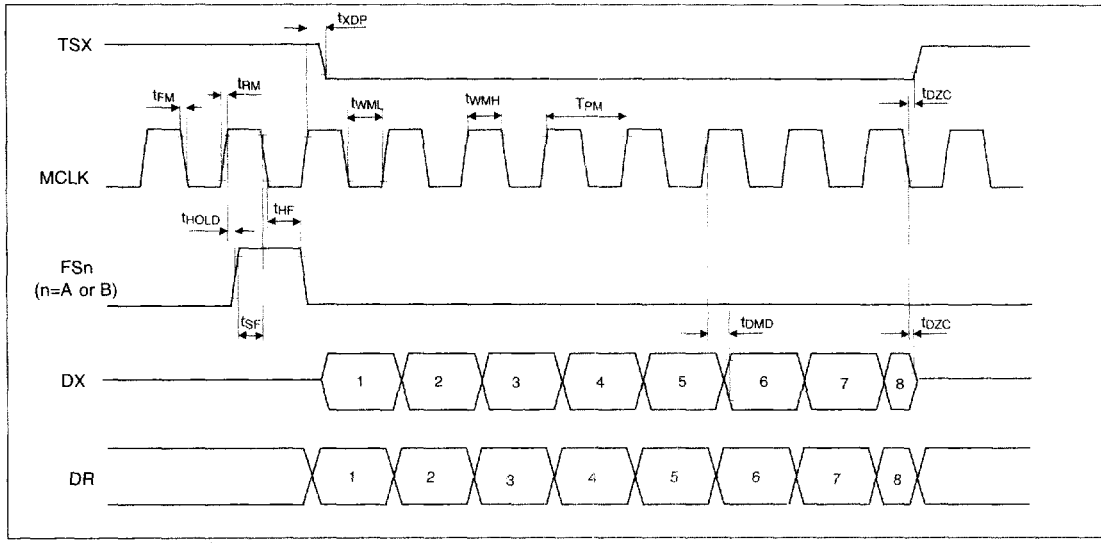

Figure 3. Short Frame Sync Timing Diagram

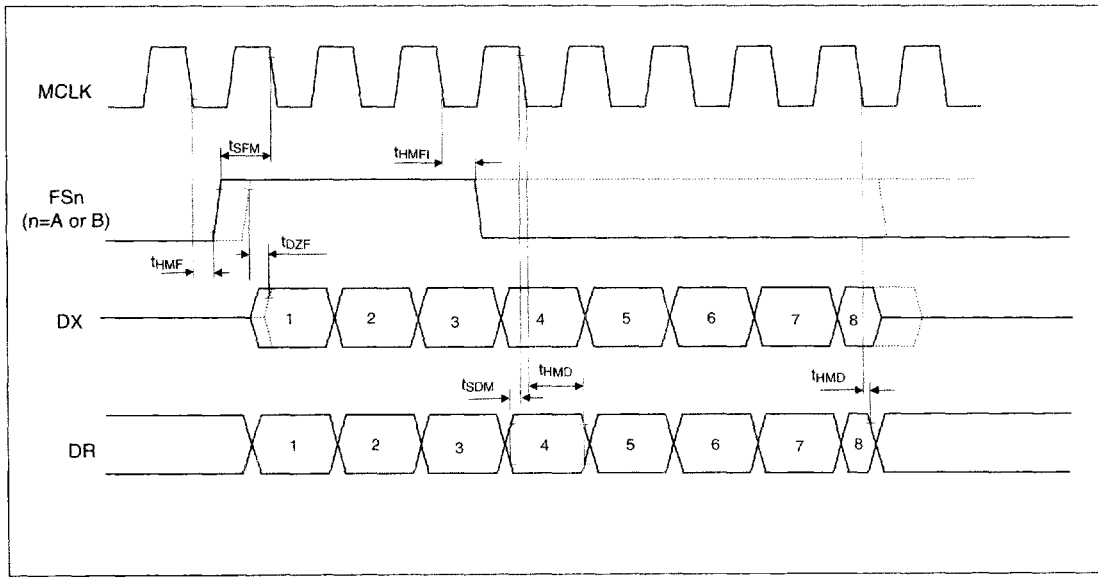

Figure 4. Long Frame Sync Timing Diagram

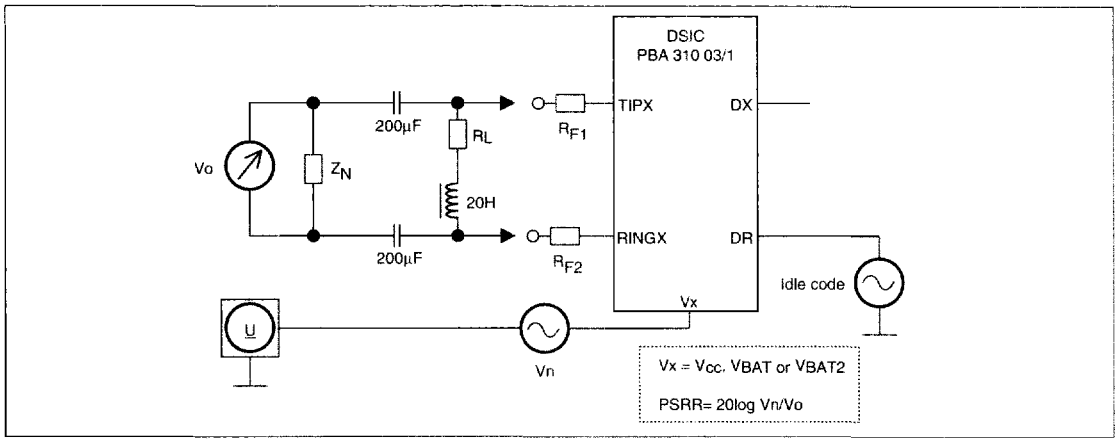

Figure 5. PSRR test circuit.

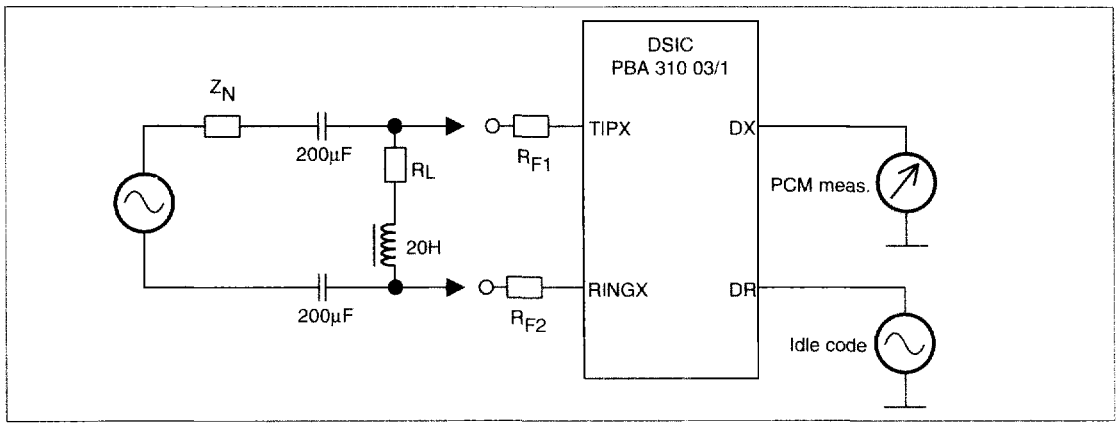

Figure 6. Transmit (A-D) test circuit.

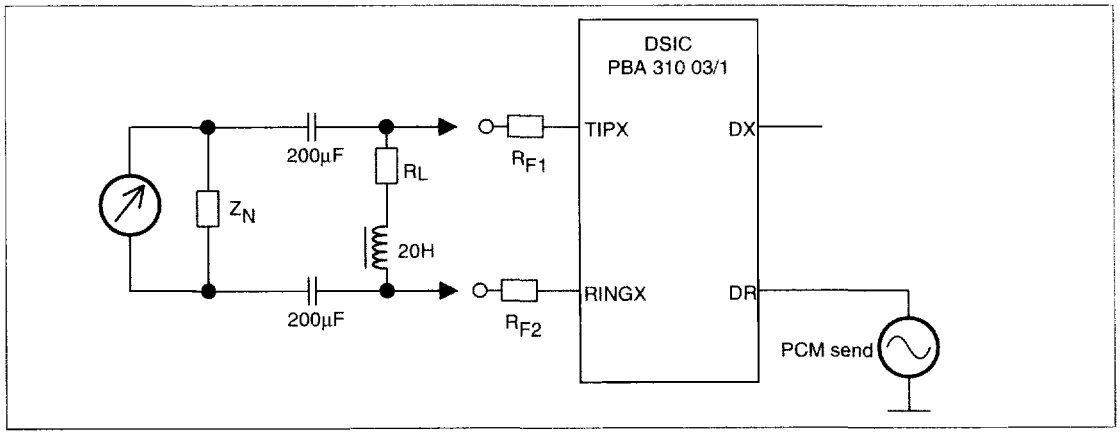

Figure 7. Receive (D-A) test circuit.

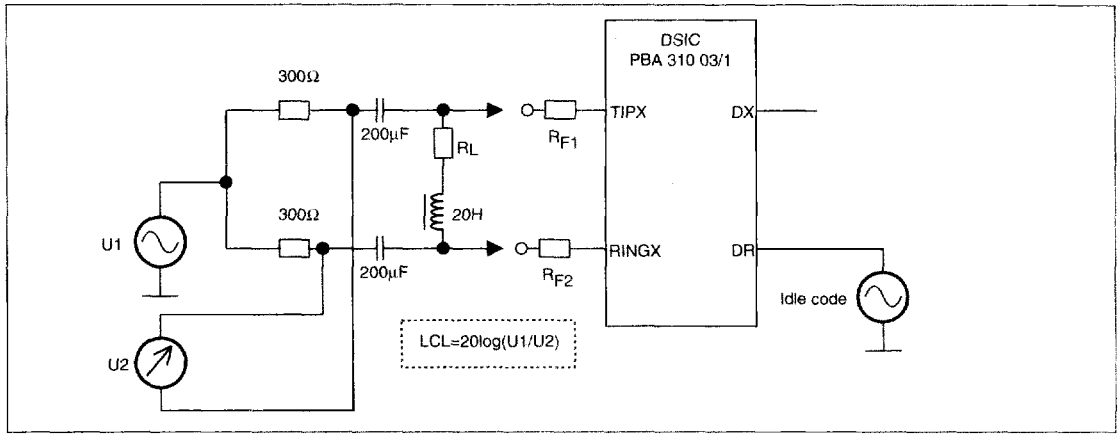

Figure 8. Longitudinal conversion loss test circuit.

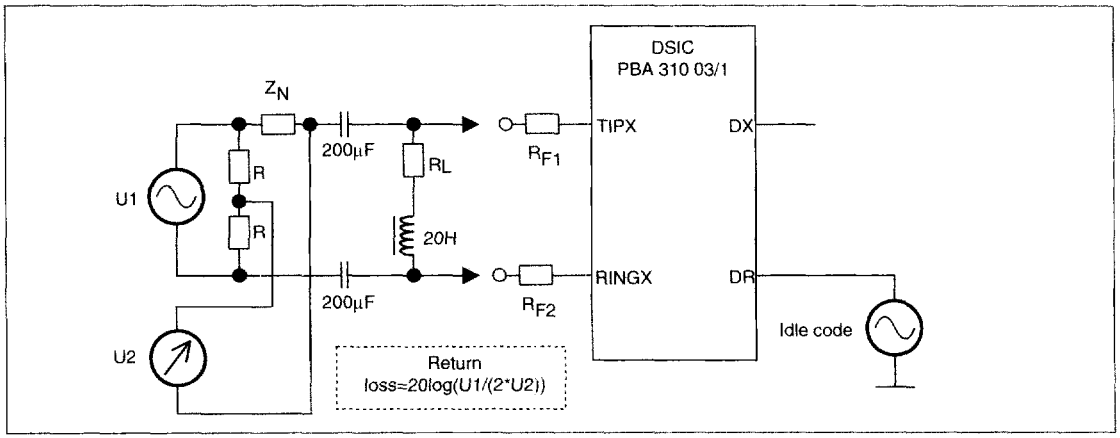

Figure 9. Return loss test circuit.

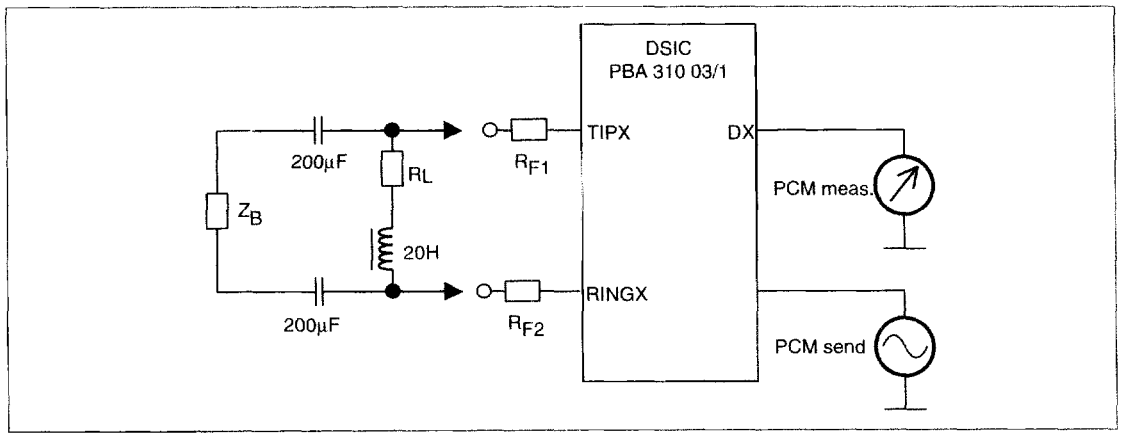

Figure 10. Terminal balance return loss test circuit.

Applications

The PBA 310 03/1 is a Dual Subscriber Interface Circuit. Only a small number of additional external components are required to implement two POTS (Plain Old Telephone Service) interfaces.

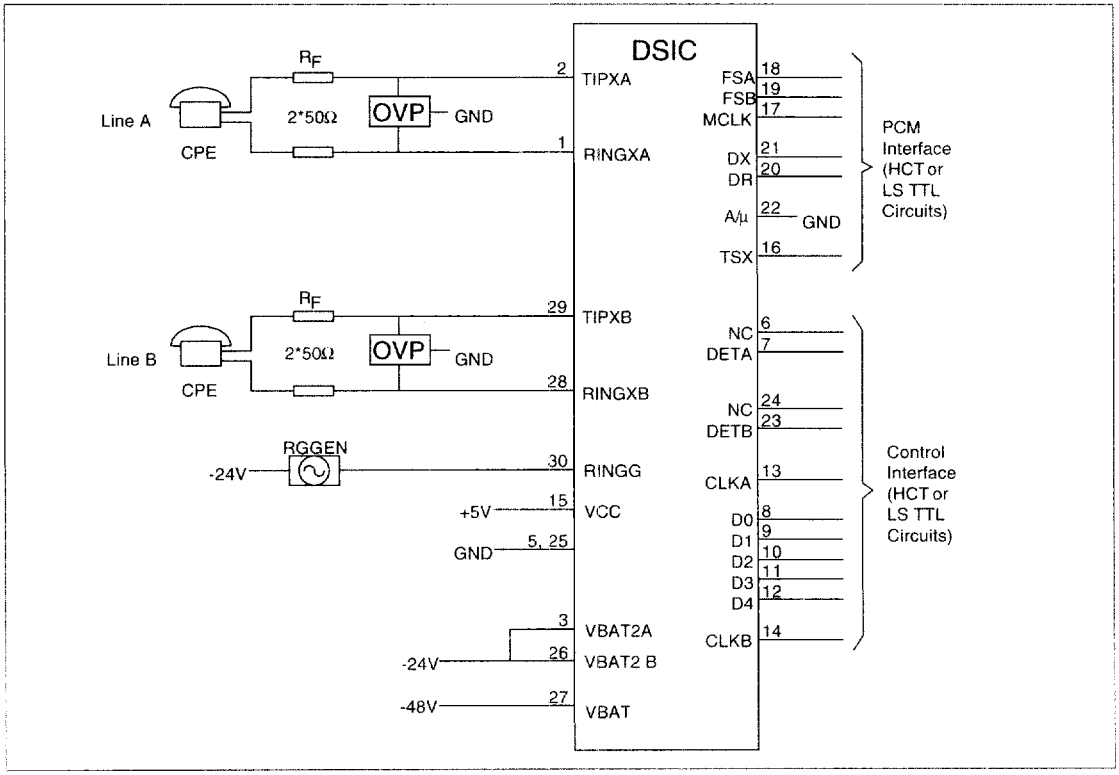

Figure 11. Typical application for the DSIC.

Denotation	Type of component
R_F	Resistor 2*50Ω with PTC protection PBR 520 03/1 or 2*50Ω with thermal fuse PBR 530 01/1
OVP	Suggested Over-Voltage Protection TISP L758LF3D, Power Innovation
CPE	Customer Premises Equipment (Telephone, Modem, Fax, etc)
RGGEN	Ring generator – refer to application notes

Application Information

Dual Codec/Filter

The A/D and D/A conversions and PCM-coding are realised by a CMOS single supply CODEC filter that is common for the two channels. A-law and μ-law PCM-coding is chosen by the A/μ-law pin (22). There are two standard ways for frame synchronisation (Long/Short frame synchronisation) both are available.

Power-on reset
Power-on reset is implemented. During the typical 150ms initialisation sequence, any input on FSA and FSB will not be taken into account.

Master clock
The master clock MCLK is common for both channels and is used in synchronous operation: the master clock and the bit clock are the same, and the master clock is used both in transmit and in receive direction. During operation, MCLK must be continuously present.

Long/short frame sychronisation selection
Long or short frame synchronisation timing modes are defined by the first frame synchronisation FSn (n=A or B) pulse after power up. This applies to power supply related power up as well as power up after auto power down. Long frame synchronisation timing is selected if first FS is three or more MCLK cycles. Otherwise short frame synchronisation timing is selected.

Short frame synchronisation operation
FSA/FSB must be one MCLK clock cycle with timing specified in figure 3. With FSn (n=A or B) high during a falling edge of MCLK, the next rising edge of MCLK latches the sign bit at the DR input and enables the DX tri-state output which will output the sign bit. The following seven rising MCLK edges latch the remaining seven bits at the DR input and output the remaining seven bits at the DX output. The next falling edge disables the DX tri-state output. The TSX open drain output is low when the DX output is enabled.

Long frame synchronisation operation
FSA/FSB must be three MCLK cycles or more with the timing specified in figure 4. The rising edge of FSn (n=A or B) or the rising edge of MCLK, whichever comes later, will latch the sign bit at the DR input and enable the DX tri-state output which will output the sign bit. The following rising edges of MCLK latch the remaining bits at the DR input and output the seven remaining bits at the DX output. The DX tri-state output is disabled by the falling edge following the eighth rising edge, or by FSn going low, whichever comes later. The TSX open drain output is low when the DX output is enabled.

Time slot assignment
Both FSA and FSB must be derived from MCLK and both should have a periodicity of 256 MCLK cycles. The internal time slot 0 is determined by the slot defined by FSA or FSB whichever comes first after power-on or auto power-down mode. FS of the other channel must be delayed from the first by a multiple of 8 MCLK cycles. The FS order must not be changed during normal operation. The change of the FS sequence is possible after an auto power-down mode as described below.

Auto power-down mode.
The dual codec enters power-down mode when the FSA or FSB defining internal time slot 0, is absent during 500ms (i.e. 4 time frames). The codec does not enter power-down mode after power-on reset if the frame sync is absent but must first be powed-up with a frame sync pulse. Power-down is not guaranteed if MCLK is lost unless the device was already in power down mode due to the absence of frame synchronisation.

SLIC Circuits

Two FlexiSLIC™ PBL 386 21/1 onboard the module performs the 4 to 2 and 2 to 4 wire conversion.

Battery feed
A constant current, typically 23.5mA, is fed to the line. When the line resistance is high and/or battery voltage is low the device automatically switches to resistive feeding, typically 90Ω with an apparent battery of $|V_{BAT}| - 5V$.

Analogue temperature guard
The dc line current will be reduced when the SLIC chip temperature reaches approximately 145°C and increases it again automatically when the temperature drops. Therefore transmission is not lost under high temperature conditions
The detector output, DET, is forced to a logic low level when the temperature guard is active.

SLIC control inputs
The control signals D0, D1 and D2 will put the SLIC in four different states:

- Open Circuit state
- Ringing state
- Active state
- Active reverse state

Refer to section Control inputs.

Ring Relay (LCAS)

Two Solid State Relays perform the switching between Idle/Talk state and Power ringing state for each channel.

Switching
There are two different ways of switching:
Break-before-make: Ringing access switch is opened before the Line switch is closed
Make-before-break: Line switch is closed before the Ringing access switch is opened

Recommended is the Break-before-make transition sequence since if Make-before-break is used the Ring signal can be switched to the SCR protection circuit in the LCAS and a false Ring Trip can occur.

Temperature guard
At a chip temperature of 110°C minimum, the thermal shutdown mechanism will be activated and force the device to an all OFF state. All switches will then be open.

Loss of battery voltage
The LCAS automatically enters the all OFF state and remains in this state until the battery voltage is restored.

Protection
Integrated in the LCAS is a diode bridge / SCR clamping circuit and current limited switches. With a secondary external OVP protection together with the suggested R_{F1} and R_{F2} on the loop side, maximum protection can be accomplished for the module.

Control Signals
The control signals D3 and D4 will put the LCAS in four different states:

- Idle/Talk state
- Power ringing state
- Hold state
- All off state

The two control signals should follow a set sequences. Refer to section Ring switching.

Parallel Control Interface

Two registers are used for controlling the active circuits. The applied input signals D0-D4 for channel A and B will be passed on the positive edge of CLKA or CLKB. Reset is performed at power up and therefore the outputs from the registers are all low at power up.

Design Considerations

Over Voltage Protection

The DSIC should be protected against surge voltages, power cross and induction conditions. In figure 11, the line feed resistors (R_F) together with the voltage clamping devices (OVP) form the secondary protection.

PBR 520 03/1 with PTC acts as a resettable fuse function for non-destructive power contact. PBR 530 01/1 with thermal fuse acts as a safe fuse function for destructive power contact. However, PBR 530 01/1 will enhance impedance unbalance (LCL) performance for the line card. The choice of R_F will be depending on market requirements regarding fuse functionality and LCL.

TISP L758LF3D provides asymmetrical protection for RINGX terminal and symmetrical for the TIPX terminal and is suitable for biased ringing applications using solid state relay (LCAS).
See table 3.

Terminal pair	Stand-off Voltage V_{DRM}	Break-over Voltage V_{BO}	Holding current I_H
TIPX to GND	+/-100V	+/- 130V	+100mA
RINGX to GND	+100V, -180V	+130, -230V	-150mA

Table 3. OVP device parameters.

The OVP-device ground connector should be as close as possible to the DSIC ground pins.

In active state using the suggested components for secondary protection, full protection according to Table1/K.20 and K.21 with Uc(max) = 1.5kV, in ITU-T recommendation for Over Voltage protection will be reached. Full protection during ringing state is dependent on choice of ring generator and must therefore be considered for each application.

A reverse current on the VBAT pin for the ring relay (LCAS) occurs when the internal thyristor is in a zener state before triggering e.g. during high impedance negative voltages. The battery should therefore be able to sink current during over-voltages otherwise V_{BAT} can drop significantly. If the battery can not sink current then a transorb (zener functionality for transient protection) should be connected between V_{BAT} and GND. The value of the transorb must be higher than the battery voltage.

Ringing

Ring Trip Detection
The ring trip function has been designed for typical off-hook detection delay (t_{RD}<100ms) under the following conditions:

	Min	Typ	Max
Ring Voltage	$65V_{RMS}$	$75V_{RMS}$	$85V_{RMS}$
Ring Frequency	20Hz		50Hz

Table 4. Ring generator voltages and frequencies.

Parameter	Min	Max	Additional parameter
Ring signal on cycle	200 ms	1500 ms	SW adjustable in steps of 5ms
Ring signal on cycle	200 ms	9000 ms	SW adjustable in steps of 5ms
Ringing duty cycle		50 %	SW adjustable. Ring on is not longer than ring off

Table 5. Suggested cadence implementation.

- Unbalanced ringing superimposed on a negative DC bias. Typically –24V.
- Maximum ring load 5 USREN
- RL=600Ω

See table 4.

Discrete as well as integrated ring generator solutions are suitable.

Cadence
Cadence of the ring signal is usually implemented by switching the states (switches) of the LCAS. When injecting the Ring signal, it is advisable to do it in a zero-voltage crossing mode, thereby reducing impulse noise in the system.

Ring access switch will not be opened before current zero crossing and this must be taken into account when programming the controller and the performance and sequence of the switching.

There are many different cadences used in different countries. Most country requirements can be met by implementing, in the controller SW, the cadence as in the table 5.

Ring switching
Recommended sequence for going from Idle/Talk state (D4,D3) = (0.1) to Power ringing state (D4,D3) = (1.1) and back is;

(0.1)=>(1.1)=>(1.0)=>(0.0)=>(0.1)
wait 0.5T

This sequence will secure a break before make status for the LCAS switches, which is recommended.

Loop Monitoring Functions

The Loop Current and Ring Trip detectors status is reported through a common output, DET. Selection of detector is made by setting D0 to low/high. With D0 low, DET output is the loop detector and by D0 high it is the Ring Trip detector.

Loop current detector

The Loop current detector indicates by the DET output at a logical low that the telephone is off-hook and dc current is flowing in the loop. Dial tone should then be presented to the subscriber.

Ring Trip detector

The Ring trip detector indicates by the DET output at a logical low that the telephone is off-hook and dc current is flowing in the loop. This should cause the system to quickly respond, by going into the Idle/Talk state for the relay function through the recommended sequence.

Control Inputs

DATA Clock

CLKA and CLKB will clock the control-input signals to channel A and channel B on the positive edge of the clock signals.

SLIC control signals

For controlling the SLIC's there are three TTL compatible digital control inputs, D0, D1 and D2. They are used to put the SLIC's in four different states;

1. **Open circuit.** SLIC circuit will be powered down as well as the TIPX and RINGX line drive amplifiers. High impedance is presented to the line.
2. **Ringing state.** Ring trip detector indicating off hook with a logic low level at detector (DET) output. The SLIC does not have a standby state and will remain in active state.
3. **Active state.** Loop detector indicating off-hook with logic low level at detector output. TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks the loop current. Vf signal transmission is normal.
4. **Active reverse.** Loop detector indicating off hook with logic low level at detector output. TIPX and RINGX polarity is reversed from the active state. Vf signal transmission is normal.

On power-up the internal control signals to the SLIC's will all be logical low. Both channels will be in Open circuit state.

LCAS control signals

For controlling the two LCAS there are two TTL compatible digital control inputs D3 and D4. They are used to put the LCAS in four different states;

1. **Idle / Talk state.** Line switches are closed and Ring switches are open. The LCAS must be in this state during transmission. This state is also used as an idle state waiting for the Subscriber going off-hook.
2. **Power ringing state.** Ring switches are closed and Line switches are open.
3. **Hold state.** Ring return switch open and Ringing access switch waiting for zero current to open. This state should be kept for 0.5T of ring signal period (T).
4. **All off.** Zero current has occurred and Ringing access switch has opened.

On power-up the internal control signals for the two LCAS will all be logical low. Both channels will be in All off state.

Battery supplies

V_{BAT} should be more negative than –48V to secure an open-loop voltage as high as 43V, which in some countries are needed for CPE:s to recognise the line as up and running.

A second lower battery, V_{BAT2}, must be connected to the device in order to reduce short loop power dissipation and thereby gain the benefits of low power dissipation for the whole system.

For a single battery system using only V_{BAT}, it is advisable to implement a thermal management resistor between the pin VBAT and the two pins VBAT2A and VBAT2B, thereby reducing power dissipation on the module. The optimal resistor value depends on typical and maximum line length.

Line length

Normal line cable length up to 200 meter, 26 gauge ø = 0.40mm, cable is feasible. This is however depending on the country specific telephone sets. The total line length (cable and telephone resistance) should not exceed R_L = 550Ω, to ensure operation using V_{BAT2} = -24V as source for the line current. However transmission will not suffer, but a higher power dissipation will occur by the switching to V_{BAT} as source for the line current.

Battery switching

Automatically without external control the device will silently switch between the two battery supply voltages. The silent battery switching occur typically when the line voltage passes the value $|V_{BAT2}| - 7.1V$.

It is possible to optimise the power dissipation by choosing the V_{BAT} and V_{BAT2} voltages depending on the typical and maximum line length and open loop voltage requirements. Please contact Ericsson Components for assistance.

Power-up Sequence

When power is applied simultaneously, there are no particular requirements for the power-up sequence.
If the DSIC is powered up in a set sequence then GND must be applied first.

Printed Circuit Board Layout

TIPX and RINGX

A minimum distance of 1mm/kV clearance is advisable for TIPX and RINGX tracks on the PCB. This minimum distance to other tracks, Uc(max) = 1.5kV give a distance of at least 1.5mm, should be kept throughout the board. Larger distances are needed if uncoated surfaces are close.

Grounding

GND should be distributed with very low impedance as a ground plane or a grid in order to sink the over-voltage current with low voltage drops between the connectors of the component. All free space of the layout should be used to improve the ground distribution. Connect module pins (5) and (25) to the ground plane.

Abbreviations

SLIC	Subscriber Line Interface Circuit
LCAS	Line Card Access Switch
ADSL	Asymmetric Digital Subscriber Line
CPE	Customer Premises Equipment
HFC	Hybrid Fibre Coax
WLL	Wireless Local Loop
CTI	Computer Telephony Integration
POTS	*Plain Old* Telephone Service
SCR	Silicon Controlled Rectifier
OVP	Over Voltage Protection
FEXT	Far End cross talk
PCB	Printed Circuit Board
Vf	Voice frequency
5 USREN	Five US Ringer Equivalent Numbers (1386Ω + 40μF)

Ordering Information

Package	**Part no.**
30 pin SIL	PBA 310 03/1

Data Sheet Order number:
1522-PBA 310 03/1 Uen Rev: B

ERICSSON

Ericsson Components AB
S-164 81 Kista-Stockholm, Sweden
Telephone: (08) 757 50 00