2004
4K (512 x 8) NON-VOLATILE RANDOM ACCESS MEMORY

- **5 Volt Only Operation**
- **Fast Static RAM Read/Write Cycles**
  2004-2, 200ns Max.
  2004, 250ns Max.
  2004-3, 300ns Max.
- **Single Line STORE & RECALL**
- **10ms Self-Timed STORE Cycles for 2004-2 and 2004 (20ms for 2004-3)**
- **Automatic Recall on Power Up**
- **Write Protect Circuit to Preserve Data On Power-Up and Power-Down**
- **Lower Power Standby Mode**
- **10-Year Data Retention for each STORE**
- **Minimum 10,000 Non-Volatile STORE Cycle Endurance**
- **Unlimited Endurance for Read, Write, and RECALL Cycles**
- **HMOS*-E FLOTOX Cell Design**
- **Conforms to JEDEC Byte-Wide Universal Site**

The Intel 2004 Non-Volatile Random Access Memory (NVRAM) is a 4K device with 512 × 8 architecture. It provides the real-time read/write functions of a static RAM together with the reliable non-volatile storage capability of an E²PROM array to preserve its memory contents when power is removed.

Internally, the 2004 NVRAM consists of a high speed static RAM array backed up, bit-for-bit, by an E²PROM array for non-volatile storage. The transfer of memory data between the static RAM and the E²PROM array occurs in parallel for fast storage and recall as well as minimal system support.

Two functions are provided to transfer data between the volatile RAM and its non-volatile E²PROM counterpart. The STORE function transfers RAM data into the E²PROM while the RECALL function fetches E²PROM data and places it in the RAM array. Both functions are controlled by a single $\overline{NE}$ signal which can easily be activated with traditional circuitry in memory mapped space, through an I/O port, or from the output of a power-fail detector.

The RAM operating characteristics of the 2004 NVRAM provides high speed microprocessor performance with unlimited endurance. In the non-volatile storage mode, data retention is specified at over 10 years for each STORE operation. Over 10,000 STORE operations can be performed reliably.

The 2004 NVRAM is furnished in a 28-pin byte wide package with its address, data and control lines configured according to the standard JEDEC universal 28-pin site.

*HMOS is patent process of Intel Corporation.

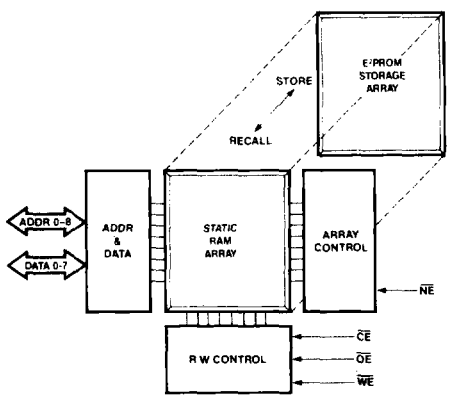

Figure 1. 2004 Functional Diagram

2004 PIN NAMES

A_0-A_8	ADDRESSES
I/O	DATA INPUT/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE (READ)
$\overline{NE}$	NON-VOLATILE ENABLE (STORE/RECALL CONTROL)
$\overline{WE}$	WRITE ENABLE
N.C.	NO CONNECT

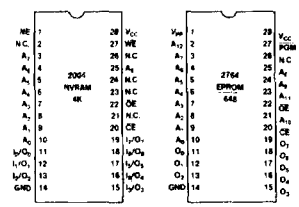

Figure 2. 2004 Pin Configuration

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NVRAM APPLICATIONS

The non-volatile RAM is designed for operation in systems where important variable data needs to be retained during periods when power is not applied to the system. It combines the flexibility of a static RAM with the reliable non-volatility of E²PROM.

The NVRAM provides a more flexible alternative than the E²PROM. E²PROMs are best suited for non-volatile storage of program code or system parameters which are occasionally altered. The NVRAM is designed for fast non-volatile storage of multiple data bytes which are in transit in the system or are being altered at microprocessor speeds.

Both NVRAMs and E²PROMs provide important, but separate, functions in the same system. An example is in communication equipment. The NVRAM is used for buffer storage for data being received or transmitted over a communications link. If power fails, a single microprocessor instruction causes the NVRAM to store all the buffered data. The E²PROM array in this system is used to store the microprocessor program code as well as look-up tables for the various operating parameters. The E²PROM program code can be updated via the communications link, and the operating parameters can be modified either remotely over the link or directly from the keyboard.

Non-volatile RAMs offer a silicon alternative to memory designs using battery-back CMOS RAM. The simple operation, single chip solution, and superior reliability of the NVRAM is a preferable alternative to the chemical battery.

The 2004 non-volatile RAM features 2-line control. By requiring a chip enable ($\overline{CE} = 0$) whenever a device function is to be activated (determined by $\overline{OE}$, $\overline{WE}$, and $\overline{NE}$), data bus contention is eliminated, system noise is reduced, and system design is simplified.

SYSTEM CONSIDERATIONS

Figure 3 illustrates a typical hardware system's block diagram. A power fail detection circuit is used to notify the system CPU of the loss of AC power via an interrupt line. The microprocessor decodes the interrupt, enters a servicing routine which writes important system data into the NVRAM, then performs a STORE initiation cycle. The STORE operation is completed in 10ms during which the power supply has held V_{CC} at 5V. As power is finally lost in the system, an on-chip V_{CC} STORE protection circuit prevents any subsequent unwanted STORE operations from being started due to system power-down noise. Data is retained in the non-volatile storage array in the NVRAM.

Figure 4 shows how to generate the $\overline{NE}$ signal with an I/O port bit for an array of 2004s.

It is a good design practice to decouple the power supply pin on any memory device. Therefore, it is recommended that a 0.1μf ceramic capacitor be used on every device between V_{CC} and GND.

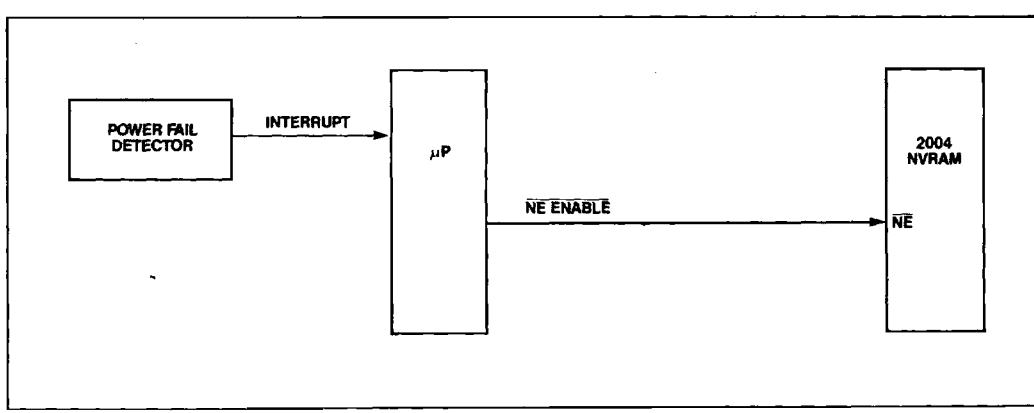


Figure 3. NVRAM System Block Diagram

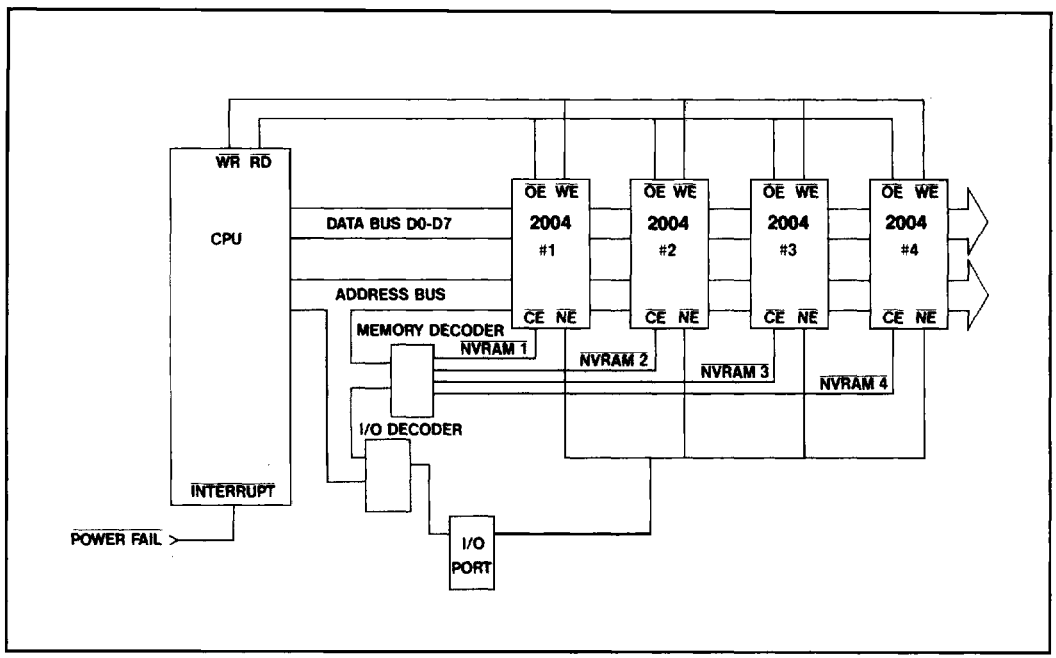


Figure 4. 2004 Array: Generating $\overline{NE}$ by I/O Output Port Bit

OPERATIONAL OVERVIEW

The non-volatile RAM uses standard control lines in accordance with established microprocessor interfaces and pinout standards. An additional control pin, non-volatile enable ($\overline{NE}$), is used to control the STORE and RECALL functions to the non-volatile storage array. For RAM access cycles the $\overline{NE}$ input is held high on the NVRAM. Addressing of each of the individual 512 RAM array bytes is accomplished using address lines 0 through 8 (A0-A8) and enabling the chip ($\overline{CE}$). Data is then transferred a byte (8 bits) at a time to and from the RAM array in the NVRAM. Data is written by lowering Write Enable ($\overline{WE}$) and holding Output Enable ($\overline{OE}$) at a TTL high level. Data is read by lowering the $\overline{OE}$ input while holding the $\overline{WE}$ input high. These functions are generally accomplished using a hardware design as shown in Figure 5.

The non-volatile functions of the NVRAM are implemented by putting a TTL low on the $\overline{NE}$ pin. A RECALL operation is initiated by bringing $\overline{OE}$ low while $\overline{NE}$ = 0. This causes the data from the NVRAM's internal non-volatile storage array to be transferred to the static RAM array, from which it can be externally accessed. The RECALL function can be activated by the CPU at any time, as often as desired without affecting the integrity of the data in the non-volatile storage array. The RECALL function is also automatically performed when the NVRAM is powered up.

A STORE operation is started by bringing $\overline{WE}$ low while holding $\overline{NE}$ low. This causes the data in the static RAM array to be transferred to the non-volatile storage array. The STORE function is typically used to save data during power failure periods and is executed

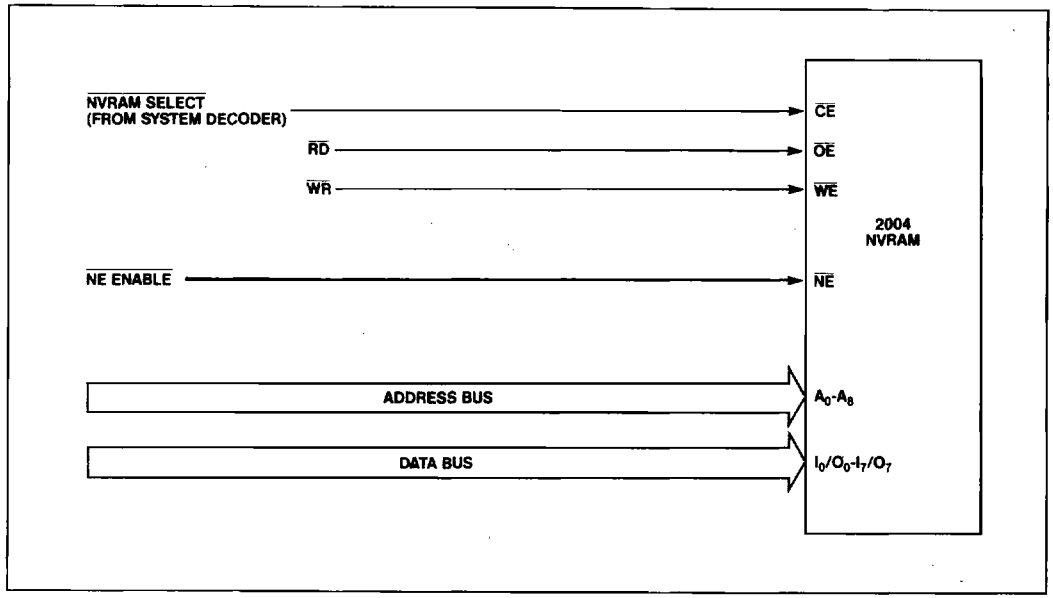


Figure 5. NVRAM System Interface

when a power fail signal is received by the system from the power supply. Since the STORE cycle takes 10ms for reliable storage, the NVRAM's Vcc supply must be maintained for this duration.

All operations of the NVRAM are gated by the chip enable ($\overline{CE}$) input. When $\overline{CE}$ is held at a TTL high level, the NVRAM is in the standby mode and consumes almost 50% less power. In this mode the data outputs are in a high impedance state. A summary of operational modes is listed in Table 1.

INADVERTENT STORE PROTECTION DURING POWER FAIL

When system power is falling the TTL devices which generate the $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ signals will no longer be stable. There is a possibility that the noise on these lines could initiate a STORE operation as V_{CC} is falling. An on-chip circuit is needed to prevent an inadvertent STORE operation. The 2004 has an on-chip inadvertent write protection circuit. When V_{CC} is between 4.0 and 4.4V the device's write mode is disabled: The lockout voltage on all products will fall in this range. Individual units will lockout at one specific voltage.

STORE AND RECALL CONSIDERATIONS

Data retention for data that has been written into the 2004's non-volatile array by a STORE operation is greater than 10 years. The STORE endurance is a minimum of 10^4 cycles, that is, at least 10,000 STORE operations can be reliably performed.

Table 1. 2004 Operational Modes Vcc = 5V

	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{NE}$	Outputs
Standby	V_{IH}	X	X	X	Hi–Z
READ	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Out
WRITE	V_{IL}	X	V_{IL}	V_{IH}	Data In
RECALL–Power Up	X	X	X	V_{IH}	Hi–Z
RECALL–Standard	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Hi–Z
STORE	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Hi–Z

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +100C
All Input or Output Voltages with
Respect to Ground ..... +6V to -0.3V

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

Operating Conditions: $T_A = 0°C$ to $70°C$
VCC = 5 VDC ± 5%

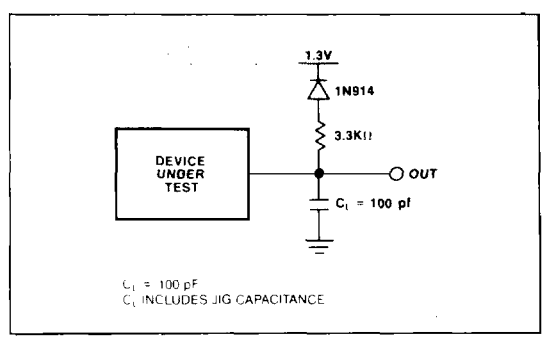
Symbol	Parameter	Min	Max	Units	Conditions
I_{LI}	Input leakage current		10	μA	VCC = max, VIN = GND to VCC
I_{LO}	Output leakage current		10	μA	VCC = max, $\overline{CE}$ = VIH, VOUT = GND to VCC
I_{CC1}	VCC current (Standby)		55	mA	VCC = max, $\overline{CE}$ = VIH
I_{CC2}	VCC current (Active)		100	mA	VCC = max, Mode = READ or WRITE
I_{CC3}	VCC current (STORE)		100	mA	VCC = max, Mode = STORE
I_{CC4}	VCC current (RECALL)		100	mA	VCC = max, Mode = RECALL
V_{IL}	Input low voltage	-0.1[1]	0.8	V	
V_{IH}	Input high voltage	2.0	VCC + 1	V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 2.1ma
V_{OH}	Output high voltage	2.4		V	I_{OH} = -400μa
V_{RCL}	V_{cc} level at which automatic RECALL begins during Power-Up	4.0	4.4	V	

Note 1. -1.0V spikes less than 20ns in duration are allowed

A.C. TEST CONDITIONS

Input pulse levels: 0.45V and 2.4V
Input rise and fall times: 20 nsec (10% and 90% levels)
Output timing reference levels: 0.8V and 2.0V

A.C. TESTING LOAD CIRCUIT



A.C. CHARACTERISTICS

READ CYCLE

Symbol	Parameter	2004-2		2004		2004-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{ACC}	Address Access Time		200		250		300	ns
t_{CE}	Chip Select Access		200		250		300	ns
t_{OE}	$\overline{OE}$ Access Time		70		100		150	ns
t_{CLZ}	$\overline{CE}$ Selection to Active Output	10		10		10		ns
t_{CHZ}	$\overline{CE}$ Deselection to Output Not Driven		60		60		130	ns
t_{OLZ}	$\overline{OE}$ Selection to Active Output	10		10		10		ns
t_{OHZ}	$\overline{OE}$ Deselection to Output Not Driven		60		60		130	ns
t_{PU}	$\overline{CE}$ Selection to Power Up Time[1]	10		10		10		ns
t_{PD}	$\overline{CE}$ Deselection to Power Down Time[1]		90		120		160	ns
t_{OH}	Output Held from Addresses, $\overline{CE}$, or $\overline{OE}$, (whichever occurs first)	0		0		0		ns

WRITE CYCLE

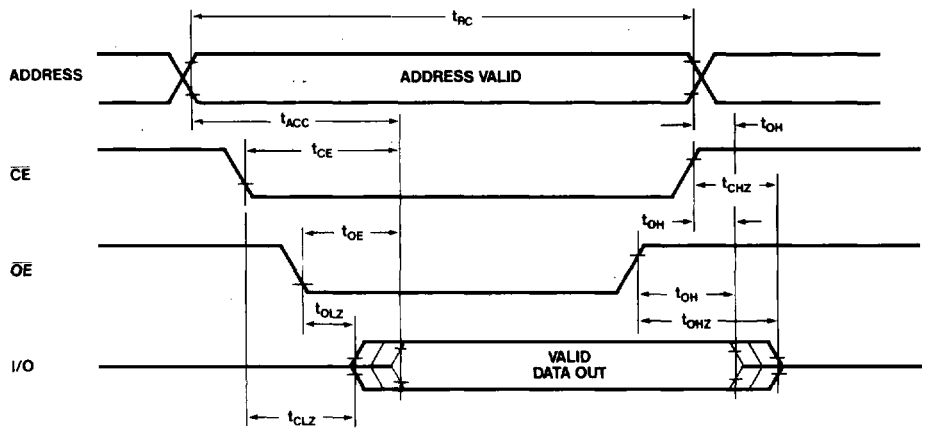
Symbol	Parameter	2004-2		2004		2004-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	200		250		300		ns
t_{CW}	Chip Selection to End of Write	200		250		300		ns
t_{AW}	Address Valid to End of Write	200		250		300		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	120		150		200		ns
t_{DW}	Data Valid to End of Write	120		150		200		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WLZ}	$\overline{WE}$ Disabled to Active Output	10		10		10		ns
t_{WHZ}	$\overline{WE}$ Enabled to Output Not Driven		60		90		130	ns
t_{WR}	Write Recovery Time	0		0		0		ns

Note 1. This refers to the powering up and down of the device's internal circuitry.

WAVEFORMS

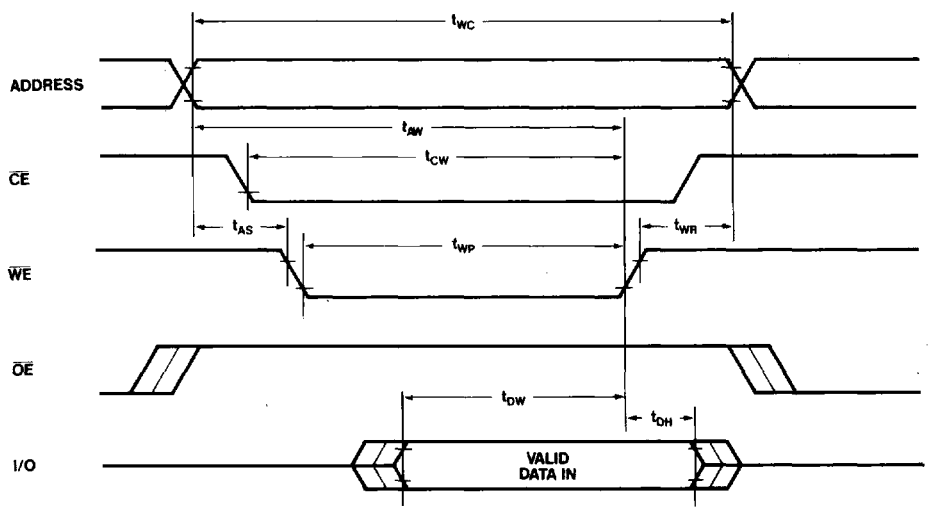
READ

CONDITIONS: $\overline{NE} = V_{IH}$, $\overline{WE} = V_{IH}$



WRITE

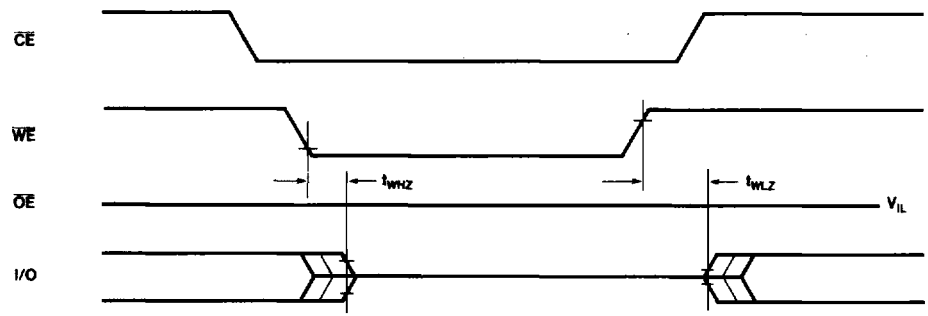
FOR SYSTEMS WITH 2-LINE CONTROL (INTEL MICROPROCESSORS)
CONDITION: $\overline{NE} = V_{IH}$



WAVEFORMS

WRITE

WITH SINGLE LINE CONTROL
CONDITION: $\overline{NE} = V_{IH}$ (OUTPUT ENABLE AND DISABLE TIMES SHOWN ONLY)

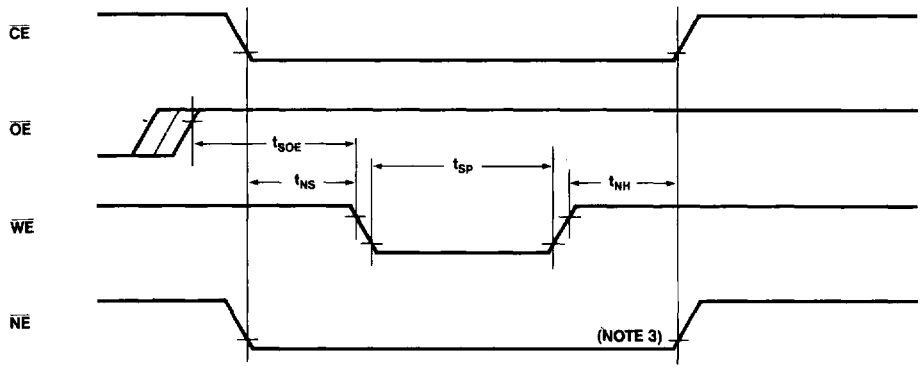


STORE Operation[1, 2]

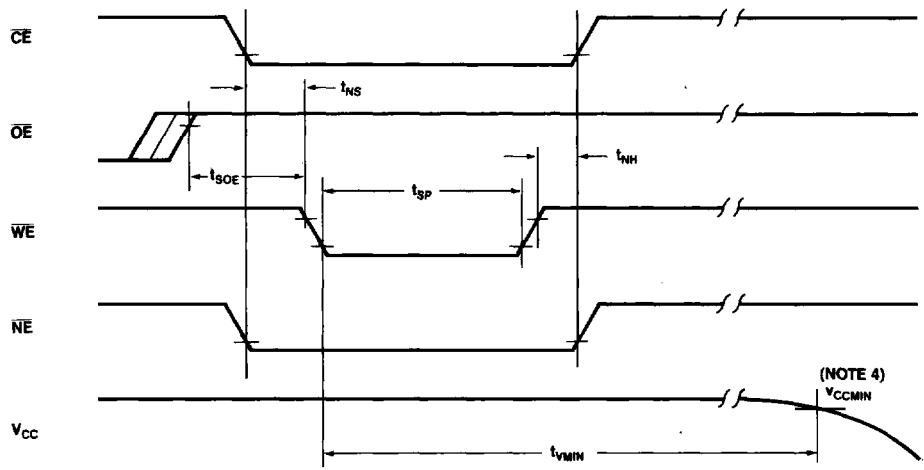
Symbol	Parameter	2004-2		2004		2004-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SOE}	$\overline{OE}$ Disable to STORE Function	200		200		200		ns
t_{SP}	STORE Pulse Width	120		150		200		ns
t_{STR}	STORE Cycle Time		10		10		20	ms
t_{VMIN}	Vcc Above Vccmin after STORE Operation Initiated	10		10		20		ms
t_{NS}	Setup Time to $\overline{WE}$ for STORE Initiation Cycle	0		0		0		ns
t_{NH}	Hold Time after $\overline{WE}$ for STORE Initiation Cycle	0		0		0		ns

WAVEFORMS (continued)

STORE INITIATION CYCLE UNDER NORMAL CONDITIONS



STORE INITIATION CYCLE DURING POWER FAIL



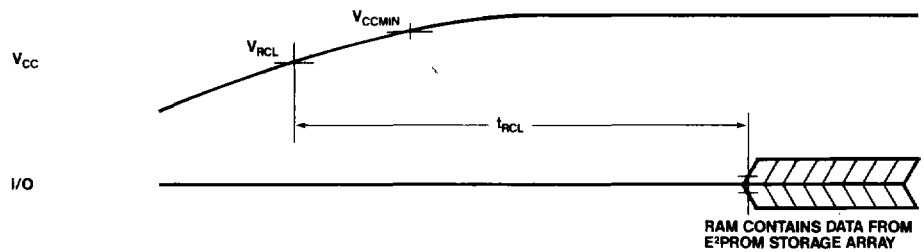
NOTES:

1. During a STORE initiation cycle, addresses and I/O inputs = DON'T CARE.
2. For a STORE cycle, $\overline{WE}$ must not go low before $\overline{NE}$. Otherwise, a RAM write cycle will result.
3. A lockout feature on the $\overline{NE}$ input prevents subsequent STORE cycles from occurring until $\overline{NE}$ is brought back high. The $\overline{NE}$ input should therefore be brought back high after a non power-fail STORE operation is initiated to allow normal read/write access after completion of the STORE operation.
4. Vccmin = 4.75V for 5% Vcc spec
5. Once a STORE operation has begun, all inputs are ignored and the outputs are in a high impedance state.

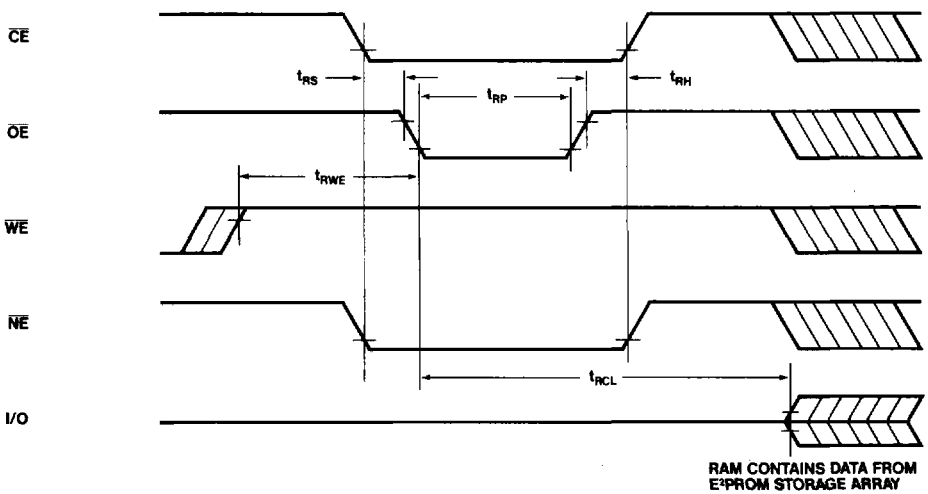
RECALL Operation[1]

Symbol	Parameter	2004-2		2004		2004-3		Units
		Min	Max	Min	Max	Min	Max	
t_{RWE}	$\overline{WE}$ Disable to RECALL Command	200		200		200		ns
t_{RP}	RECALL Pulse Width	120		150		200		ns
t_{RCL}	RECALL Cycle Time		10		10		10	μs
t_{RS}	Setup Time to RECALL Command	0		0		0		ns
t_{RH}	Hold Time after RECALL Command	0		0		0		ns

AUTOMATIC RECALL DURING POWER UP[2]



RECALL INITIATION CYCLE UNDER NORMAL CONDITIONS (NOTE 3)



NOTES:

1. During a RECALL Initiation Cycle, the address and data inputs = DON'T CARE.
2. During Automatic Power-Up RECALL, $\overline{CE} = \overline{WE} = \overline{OE} = \overline{NE}$ = DON'T CARE.
3. Once a RECALL operation has begun, all inputs are ignored and the outputs are in a high impedance state.
4. Vccmin = 4.75V for 5% Vcc spec