FUJITSU
MICROELECTRONICS, INC.

MB8264A
MB8264A

MB8266A-10
MB8266A-12
MB8266A-15

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

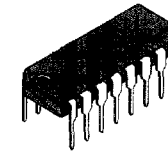
DESCRIPTION

The Fujitsu MB8266A is a fully decoded dynamic NMOS random access memory organized as 65,536 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

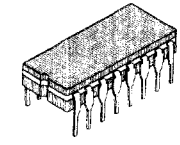
The MB8266A offers new functional enhancements that make it more versatile than previous dynamic RAMS. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is compatible with upward expansion to 256K dynamic RAMS, since pin 1 is left as a "no connect". The MB8266A also features Nibble Mode, which allows high speed serial access to up to four bits of data. Multiplexed row and column address inputs permit the MB8266A to be housed in a Jedec standard 16-pin DIP and 18-pad LCC.

The MB8266A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including sense amplifiers.

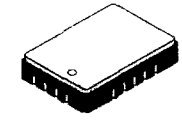
Clock timing requirements are non-critical and the power supply tolerance is very wide. All inputs and output are TTL compatible.



PLASTIC PACKAGE
DIP-16P-M03



CERDIP PACKAGE
DIP-16C-C04

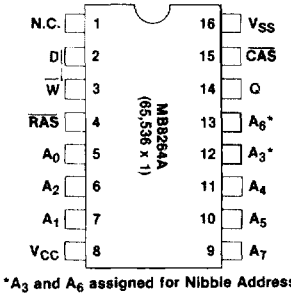


CERAMIC LCC
LCC-18C-F02

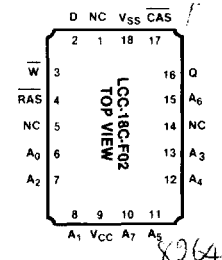
FEATURES

- **65,536 x 1-bit organization**
- **Row Access Time/Cycle Time**
  MB8266A-10 100 ns Max./200 ns Min.
  MB8266A-12 120 ns Max./230 ns Min.
  MB8266A-15 150 ns Max./260 ns Min.
- **Nibble Access Time/Cycle Time**
  MB8266A-10 25 ns Max./60 ns Min.
  MB8266A-12 30 ns Max./70 ns Min.
  MB8266A-15 40 ns Max./90 ns Min.
- **Low Maximum Power Dissipation**
  MB8266A-10 275 mW (Active)
  MB8266A-12 248 mW (Active)
  MB8266A-15 220 mW (Active)
  All devices 25 mW (Standby) Max.
- **Single +5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Nibble mode capability for faster access**
- **$\overline{CAS}$ before $\overline{RAS}$ on chip refresh**
- **$\overline{RAS}$ only refresh**
- **Hidden $\overline{CAS}$ before $\overline{RAS}$ on chip refresh**
- **2ms/128 cycle refresh**
- **Read-Modify-Write capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows two-dimensional chip select**
- **On-chip Address and Data-in latches**
- **On-chip substrate bias generator**
- **t_{AR}, t_{WCR}, t_{DHR} eliminated**

PIN ASSIGNMENTS

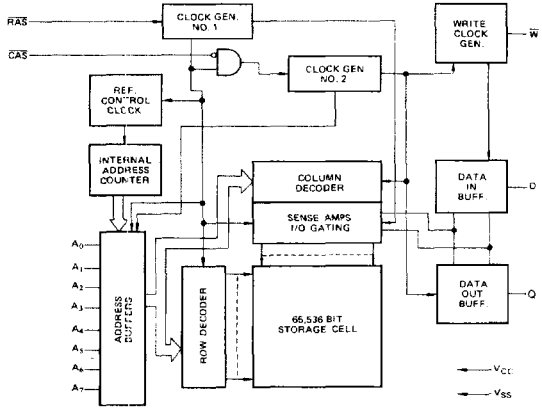


*A_3 and A_6 assigned for Nibble Address



8264ALCC

MB8266A BLOCK DIAGRAM



Note: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data in, $\overline{W}$ = Write Enable, Q = Data Out.

ABSOLUTE MAXIMUM RATING (See Note)

R7

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short circuit output current		I_{OS}	50	mA

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

R4

Parameter	Symbol	Value			Unit	Ambient Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

R3

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_7, D	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	—	8	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

R9

Parameter	Symbol	MB8266A-10		MB8266A-12		MB8266A-15		Unit
		Min	Max	Min	Max	Min	Max	
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	I_{CC1}	—	50	—	45	—	40	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$/$\overline{CAS}$ = V_{IH})	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	I_{CC3}	—	38	—	35	—	31	mA
NIBBLE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min)	I_{CC4}	—	21	—	21	—	21	mA
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$-before-RAS)	I_{CC5}	—	42	—	38	—	34	mA
INPUT LEAKAGE CURRENT any input ($0 \le V_{IN} \le 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT HIGH VOLTAGE (I_{OH} = −5 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
OUTPUT LOW VOLTAGE (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V

Note: I_{CC} is dependent on output loading cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS (Recommended operating conditons unless otherwise noted.)

R46

Parameter	Notes	Symbol		MB8266A-10		MB8266A-12		MB8266A-15		Unit
		Alternate	*Standard	Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	230	—	265	—	280	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn Off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{CAS}$ Precharge Time		t_{CP}	TCEHCEL	50	—	50	—	55	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	4 7	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	30	—	30	—	30	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Write Command Set Up Time		t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	35	—	40	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	35	—	40	—	45	—	ns
Data In Set Up Time		t_{DS}	TDVREL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	8	t_{CWD}	TCELWL	40	—	50	—	60	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay	8	t_{RWD}	TRELWL	90	—	110	—	120	—	ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)		t_{FCH}	TRELCEX	20	—	25	—	30	—	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
Nibble Mode Read/Write Cycle Time		t_{NC}	TCEHCEH	60	—	70	—	90	—	ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	TCEHCEH	75	—	90	—	120	—	ns
Nibble Mode Access Time		t_{NCAC}	TCELQV	—	25	—	30	—	40	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	TCELCEH	25	—	30	—	40	—	ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	TCEHCEL	25	—	30	—	40	—	ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	TCELREH	25	—	30	—	40	—	ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	TCELREH	35	—	40	—	45	—	ns
Nibble Mode Write Command to $\overline{CAS}$ Lead Time		t_{NCWL}	TWLCEH	20	—	25	—	35	—	ns
Nibble Mode Write Command Set Up Time		t_{NWCS}	TWLCEL	0	—	0	—	0	—	ns
Nibble Mode $\overline{CAS}$ to $\overline{W}$ Delay		t_{NCWD}	TCELWL	15	—	20	—	30	—	ns
Refresh Counter Test Cycle Time	10	t_{RTC}	TRELREL	300	—	350	—	405	—	ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	10	t_{TRAS}	TRELREH	200	—	240	—	295	—	ns

See Notes on following page.

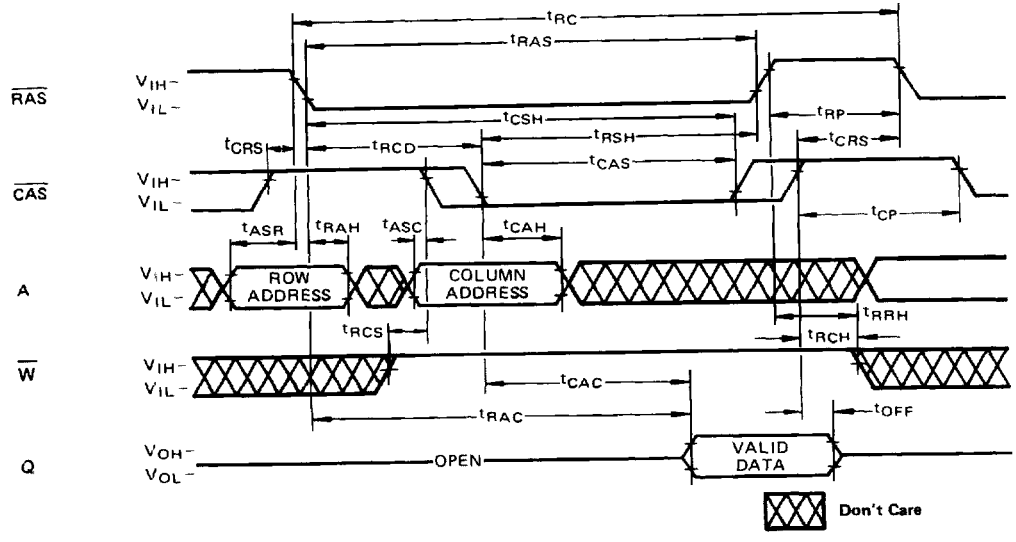
***These symbols are described in IEEE STD 662-1980: IEEE Standard Terminology for Semiconductor Memory.**

Notes:

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. (If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.)
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max) the specified maximum value of t_{RAC} (max) can be met. If $t_{RCD} > t_{RCD}$ (max) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5ns) + t_{ASC} (min).
8. t_{WCS}, t_{CWD} and t_{RWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Refresh counter test cycle only.

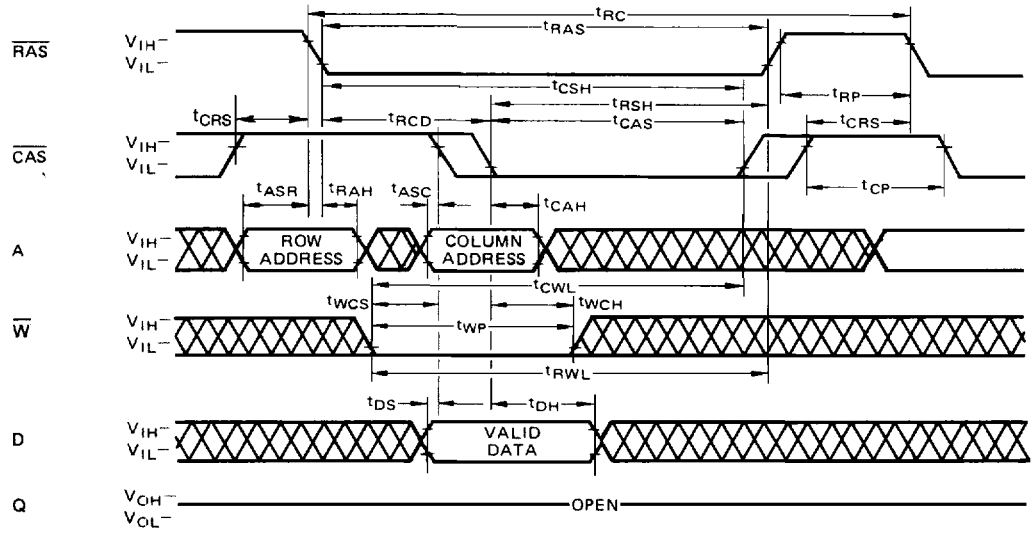
TIMING DIAGRAMS

READ CYCLE

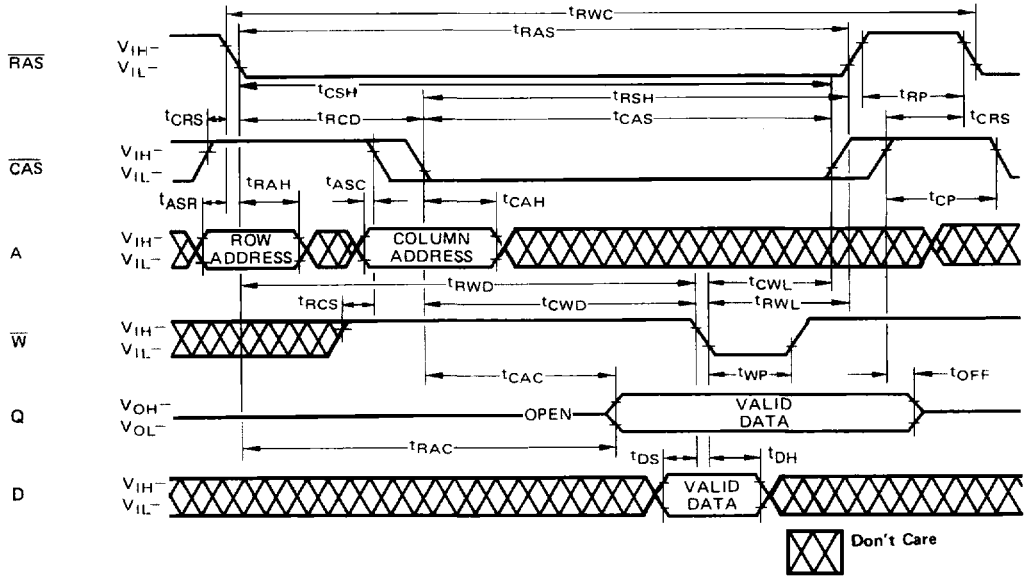


TIMING DIAGRAMS (Continued)

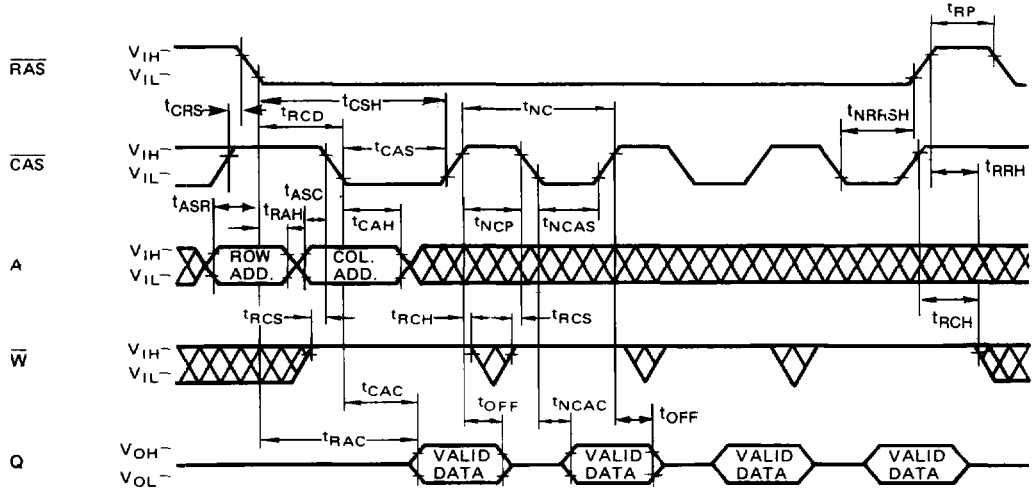
WRITE CYCLE (EARLY WRITE)



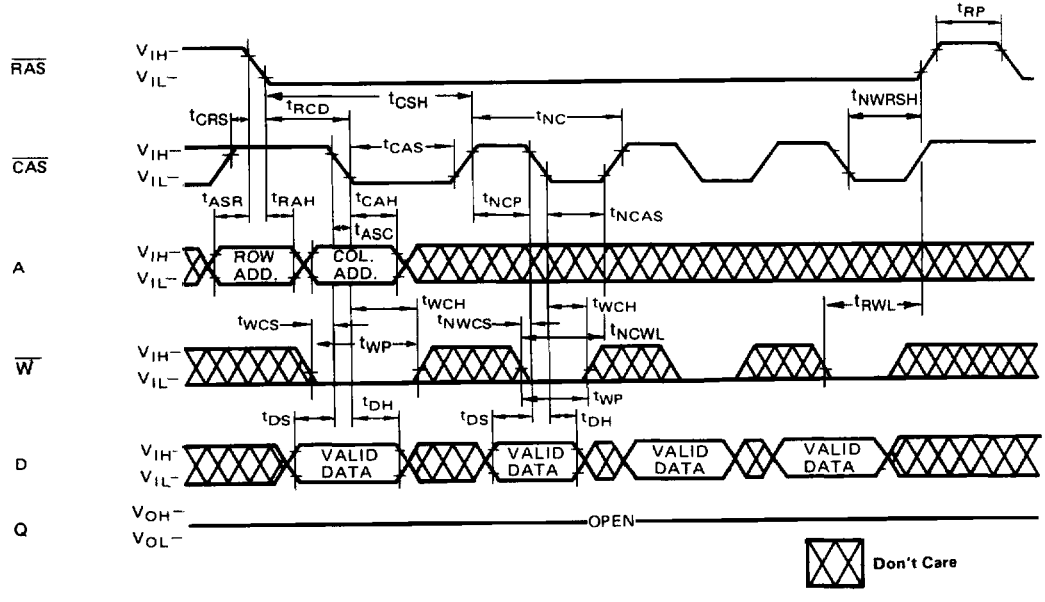
READ-WRITE/READ-MODIFY-WRITE CYCLE



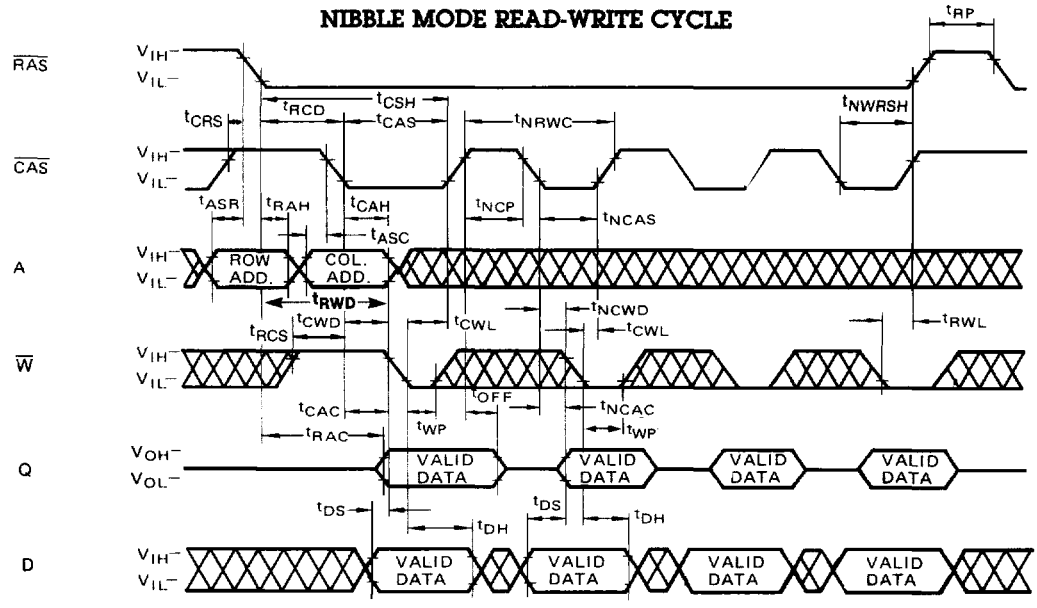
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE

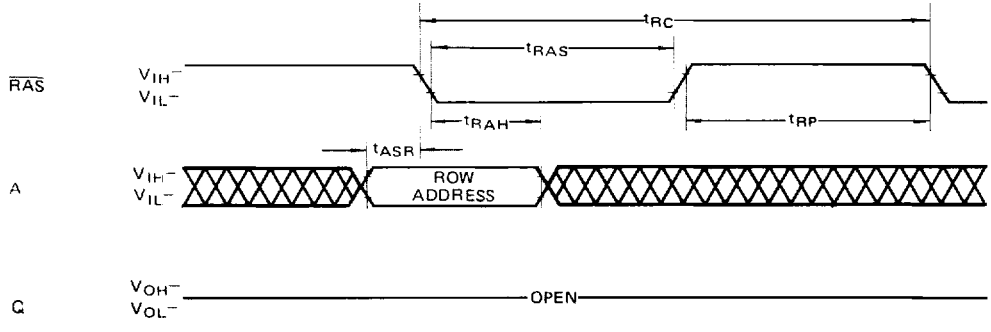


NIBBLE MODE READ-WRITE CYCLE



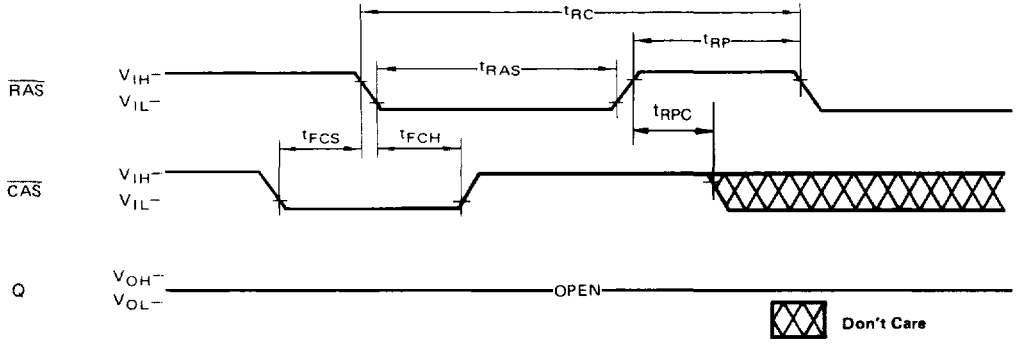
"RAS-ONLY" REFRESH CYCLE

Note: CAS = V_{IH}, W, D = Don't Care



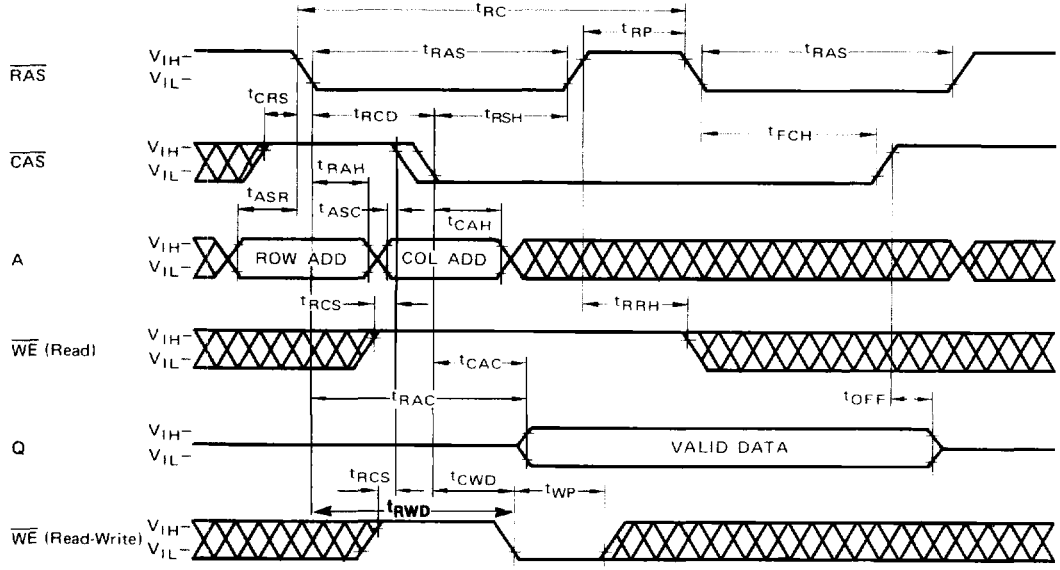
"CAS-BEFORE-RAS" REFRESH CYCLE

Note: A, W, D = Don't Care

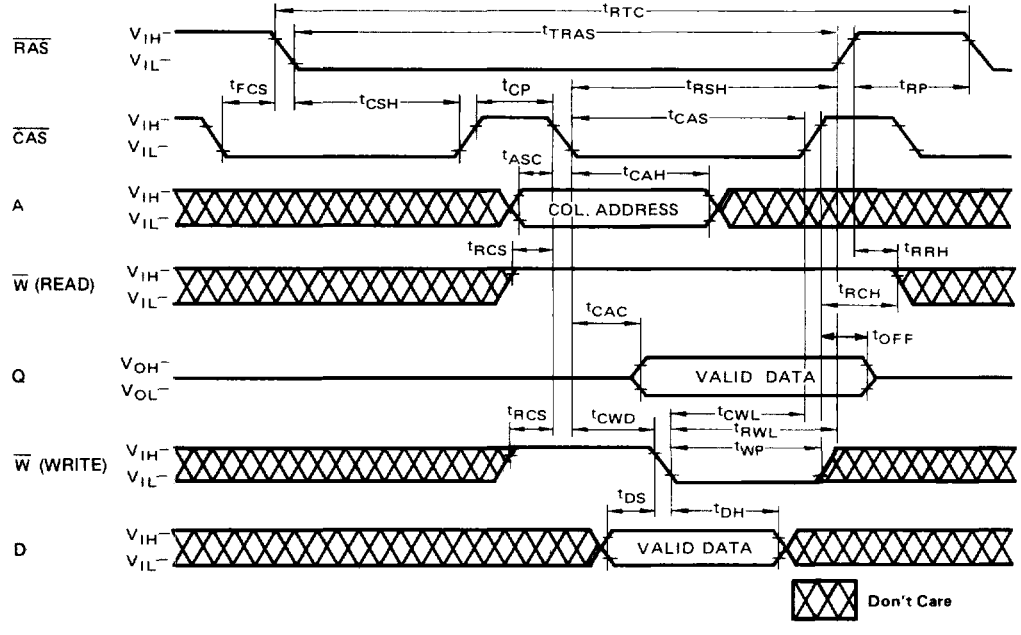


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8266A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high (1) on $\overline{W}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8266A during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data In (D) register. In a write cycle, if $\overline{W}$ is brought low (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ must be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0 ~ A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and 6 column addresses. The 2 column address bits (A_3, A_6) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes A_6 and A_3 to be incremented internally while all the other address bits are held constant thereby making the next nibble bit available for access. (See Table 1).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, read, write, and read-modify-write operations may be performed in any desired combination.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB8266A offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

A Hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB8266A, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh address as in a normal $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled. A memory cell can be addressed with 8 row address bits and 8 column address bits defined as follows:

- *A ROW ADDRESS—Bits A_0 through A_6 are defined by the refresh counter. The other bit A_7 is set "low" internally.
- *A COLUMN ADDRESS—All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

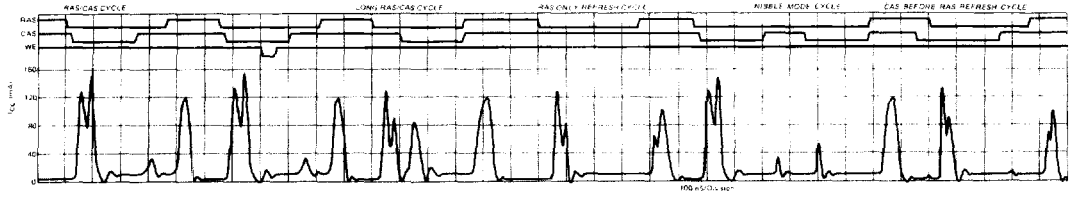
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

(1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
(2) Write a test pattern of "low"s into the memory cells at a single column address and 128 row addresses.
(3) Using a read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new "high" in the same cycle. This cycle is repeated 128 times, and "high"s are written into the 128 memory cells.
(4) Read the "high"s written at the last operation (Step (3)).
(5) Compliment the test pattern and repeat steps (2), (3) and (4).

NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

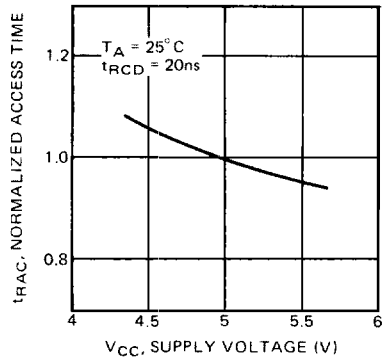
Sequence	Nibble Bit	Row Address	Column Address			
				A_3	A_6	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	10101010	101010	1	0	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	10101010	101010	1	1	generated internally
toggle $\overline{CAS}$ (nibble mode)	3	10101010	101010	0	0	
toggle $\overline{CAS}$ (nibble mode)	4	10101010	101010	0	1	
toggle $\overline{CAS}$ (nibble mode)	1	10101010	101010	1	0	sequence repeats

CURRENT WAVEFORM (V_{CC} = 5.5V, TA = 25°C)

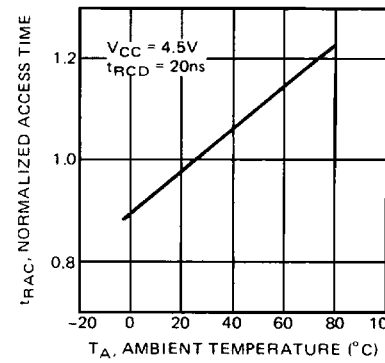


TYPICAL CHARACTERISTICS CURVES

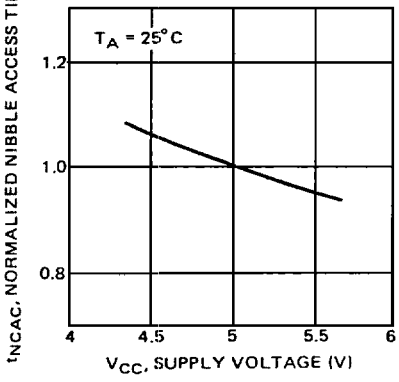
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



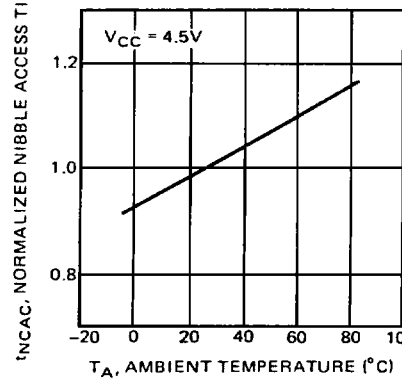
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



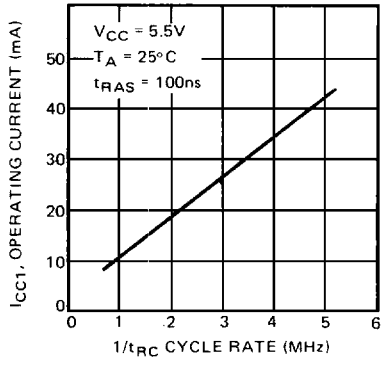
NORMALIZED NIBBLE ACCESS TIME vs SUPPLY VOLTAGE



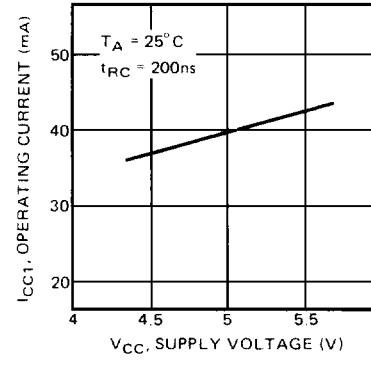
NORMALIZED NIBBLE ACCESS TIME vs AMBIENT TEMPERATURE



OPERATING CURRENT vs CYCLE RATE

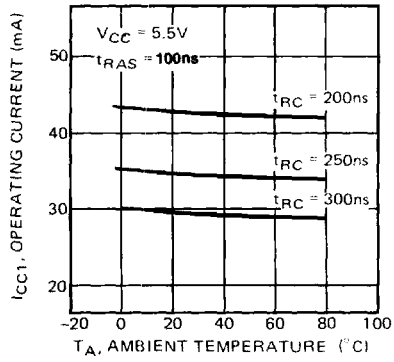


OPERATING CURRENT vs SUPPLY VOLTAGE

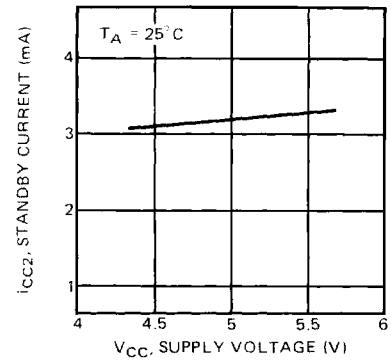


TYPICAL CHARACTERISTICS CURVES (Continued)

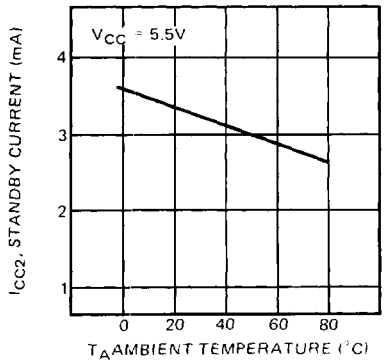
OPERATING CURRENT vs AMBIENT TEMPERATURE



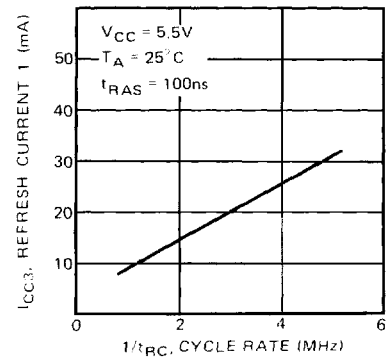
STANDBY CURRENT vs SUPPLY VOLTAGE



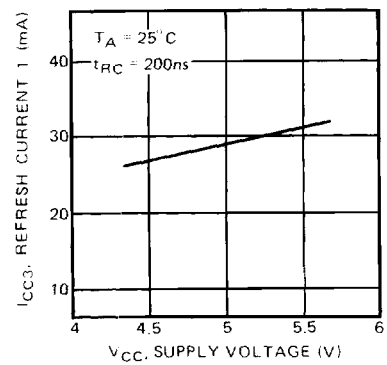
STANDBY CURRENT vs AMBIENT TEMPERATURE



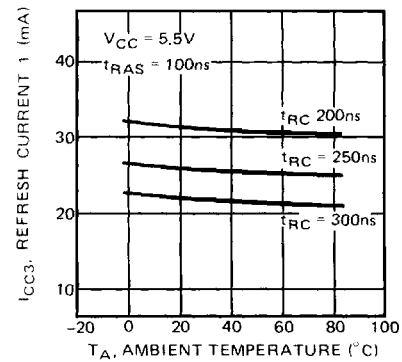
REFRESH CURRENT 1 vs CYCLE RATE



REFRESH CURRENT 1 vs SUPPLY VOLTAGE

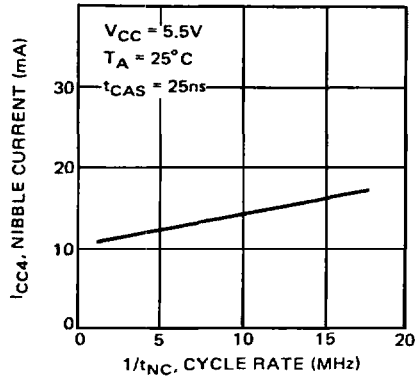


REFRESH CURRENT 1 vs AMBIENT TEMPERATURE

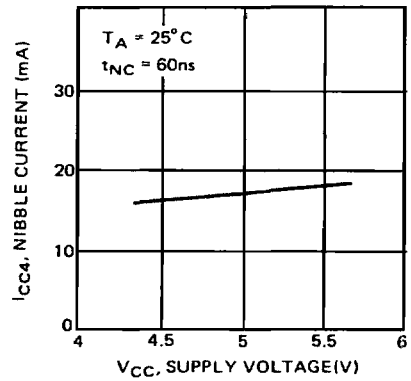


TYPICAL CHARACTERISTICS CURVES (Continued)

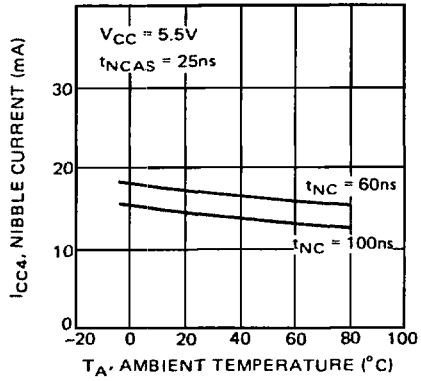
NIBBLE CURRENT vs CYCLE RATE



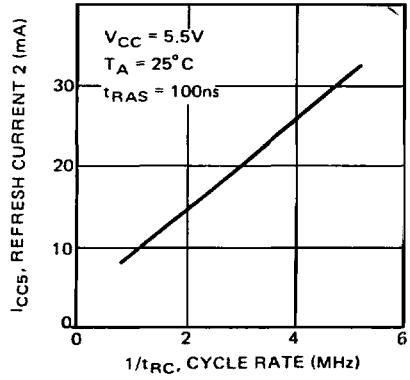
NIBBLE CURRENT vs SUPPLY CURRENT



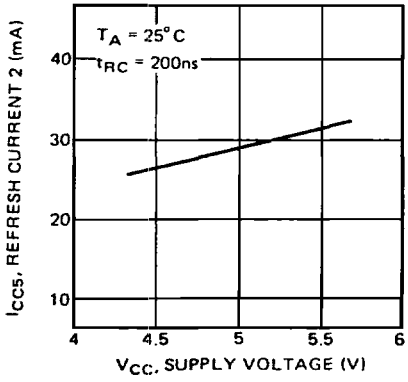
NIBBLE CURRENT vs AMBIENT TEMPERATURE



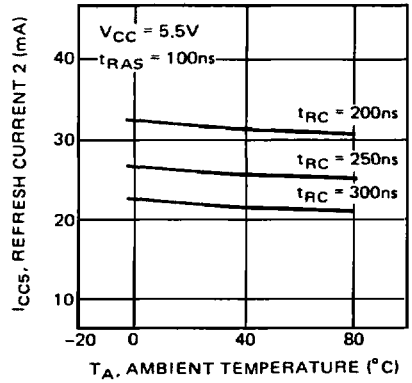
REFRESH CURRENT 2 vs CYCLE RATE



REFRESH CURRENT 2 vs SUPPLY VOLTAGE

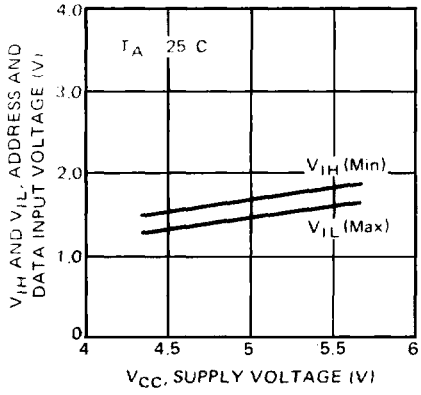


REFRESH CURRENT 2 vs AMBIENT TEMPERATURE

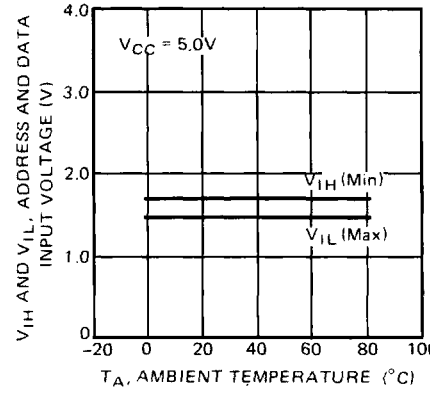


TYPICAL CHARACTERISTICS CURVES (Continued)

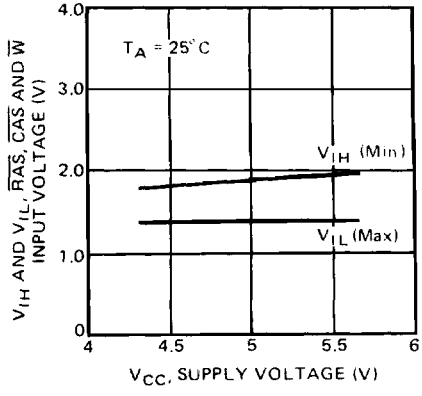
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



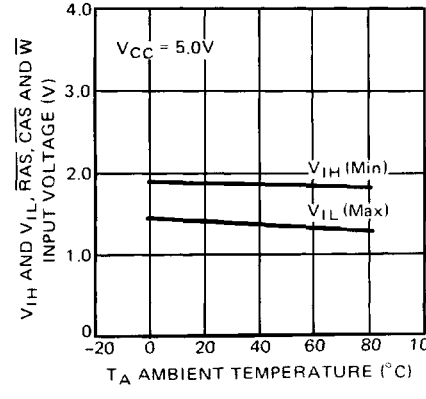
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

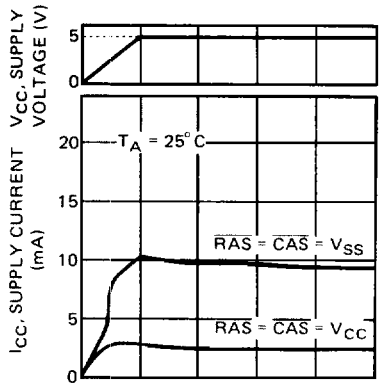


$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

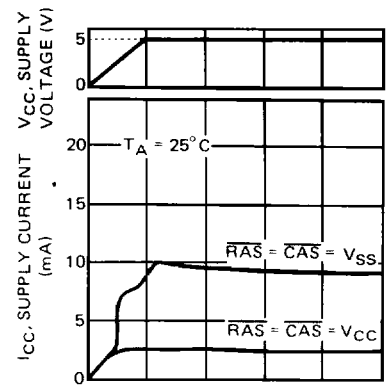


TYPICAL CHARACTERISTICS CURVES (Continued)

CURRENT WAVEFORM DURING POWER UP

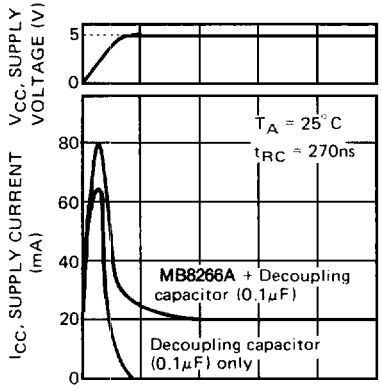


10μs/Division

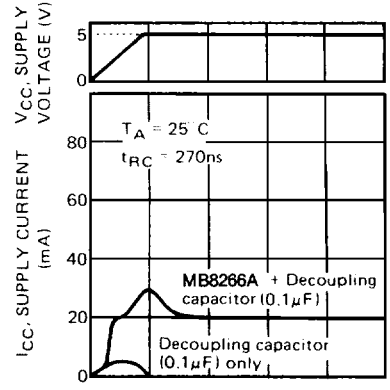


100μs/Division

CURRENT WAVEFORM DURING POWER UP (ON MEMORY BOARD)

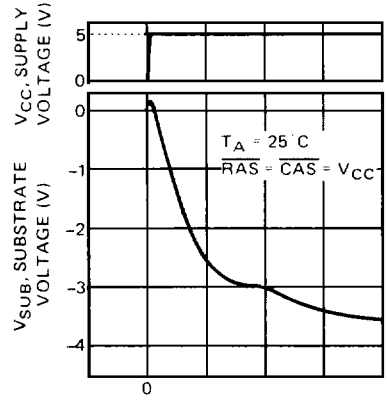


20μs/Division



100μs/Division

SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE (DURING POWER UP)



50μs/Division