SLG84503

Management Clock

Features

- Supports Intel CK-MNG+ specifications
- One CPU/SRC selectable differential clock pair
- Individual tristate control and power down functions
- High PPM accuracy
- Spread Spectrum support for EMI reduction
- 3.3 Volt Power Supply
- 40-pin QFN Package

Output Summary

- 1 - differential 96MHz clock output @ 0.7V
- 1 - differential CPU clock output @ 0.7V
- 2 - single-ended 25MHz clock outputs @ 3.3V
- 6 - single-ended 50MHz clock output @ 3.3V
- 2 - single-ended 125MHz clock output @ 3.3V
- 1 - single-ended 32.768KHz output
- 1 - single-ended 33.3MHz output
- 25MHz crystal input

The SLG84503 clock synthesizer is a single-chip clock solution intended to be a low-cost high performance platform clocking solution. The SLG84503 synthesizes and distributes a multitude of clock outputs at various frequencies, timings and drive levels using a single 25MHz crystal. The SLG84503 serves as the base clocking component for CPU, Video, RMII and other miscellaneous clocks.

CPU Frequency Table

CPU FS2	CPU FS1	CPU FS0	CPUCLK MHz
Byte0 Bit2	Byte0 Bit1	Byte0 Bit0	
0	0	0	266.67
0	0	1	133.33
0	1	0	200.00
0	1	1	166.67
1	0	0	333.33
1	**0**	**1**	**100.00**
1	1	0	400.00
1	1	1	Reserved

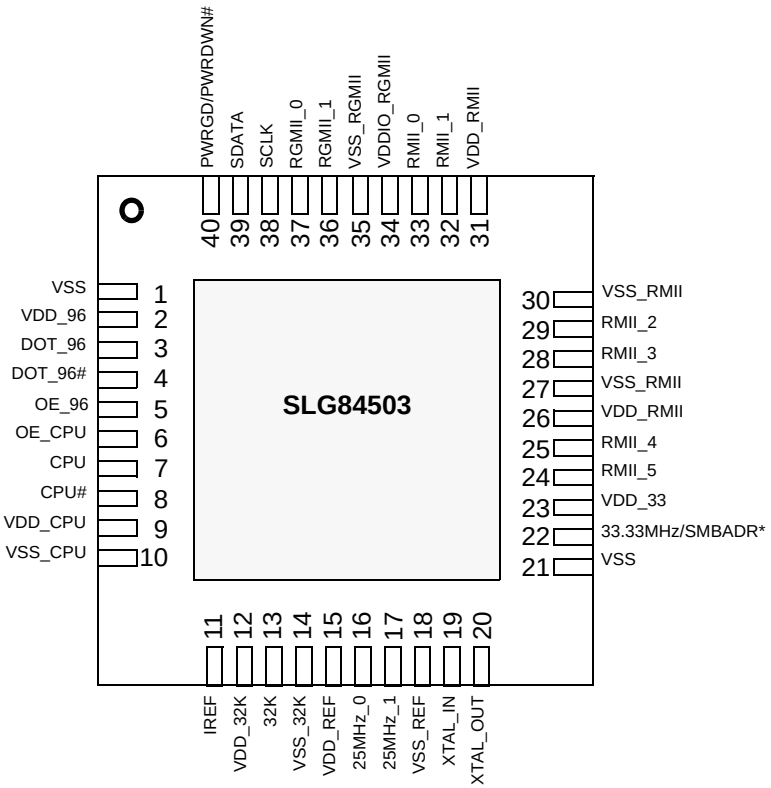
Note: CPU frequency power up defualt = 100MHz

SMBus Address Selection

SMBADR	
*SMBADR = 0	SMBADR = 1
D_0/D_1	C_0/C_1

* Default Value

Pin Configuration



Note: * Internal Pull-Down Resistor - Default

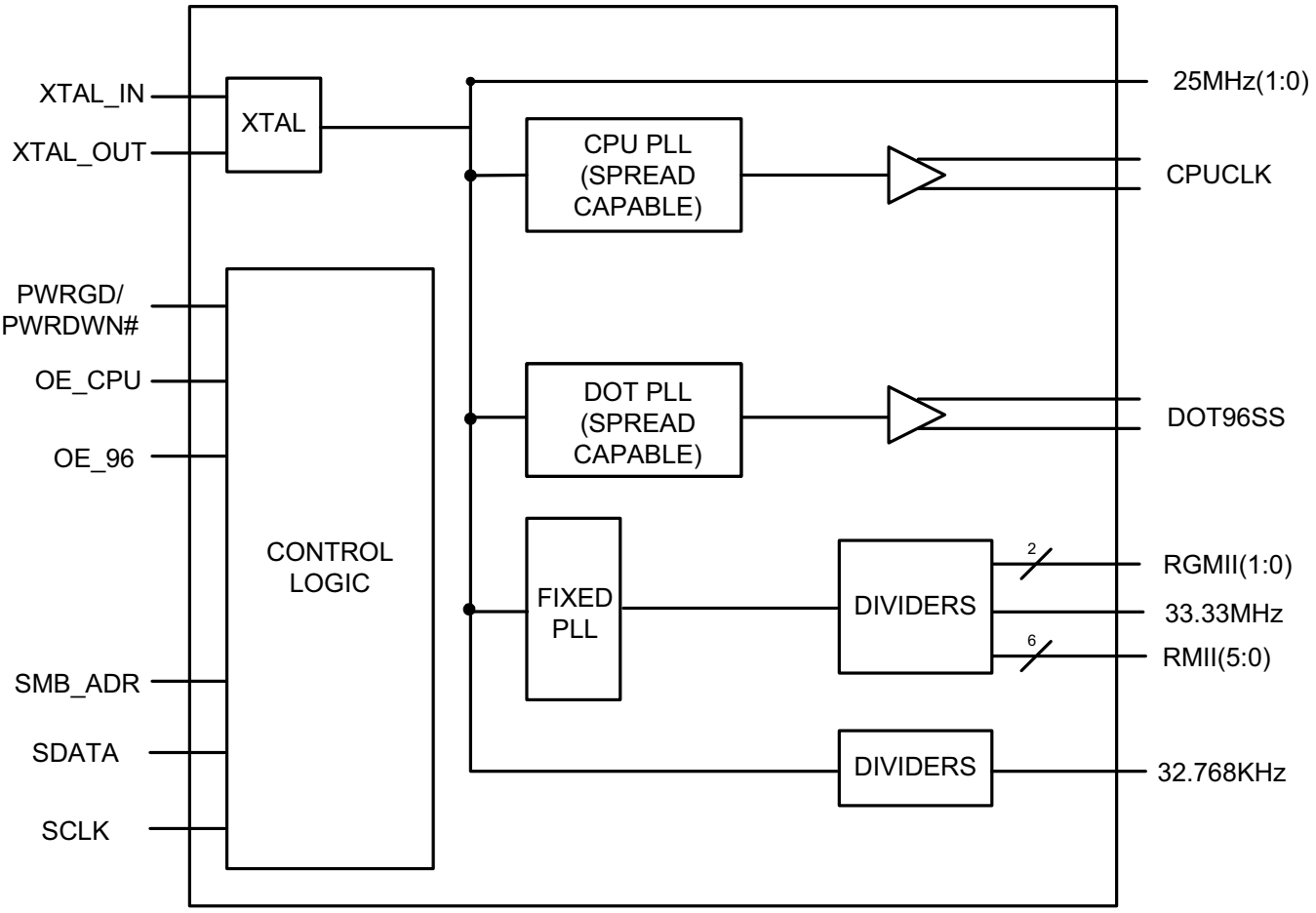
Pin Description

Pin #	Name	Type	Description
1	VSS	GND	Ground for outputs.
2	VDD_96	PWR	3.3V power supply for outputs
3	DOT_96	O, DIF	96MHz differential clock outputs
4	DOT_96#	O, DIF	96MHz differential clock outputs
5	OE_96	I	Active high input for enabling 96MHz outputs. 1 = enable outputs, 0 = tri-state outputs
6	OE_CPU	I	Active high input for enabling CPU outputs. 1 = enable outputs, 0 = tri-state outputs
7	CPU	O, DIF	CPU differential clock outputs
8	CPU#	O, DIF	CPU differential clock outputs
9	VDD_CPU	PWR	3.3V power supply for outputs
10	VSS_CPU	GND	Ground for outputs.
11	IREF	I	A precision resistor is attached to this pin, which is connected to the internal current reference.
12	VDD_32K	PWR	3.3V power supply for outputs
13	32K	O, SE	32.768kHz clock output
14	VSS_32K	GND	Ground for outputs.
15	VDD_REF	PWR	3.3V power supply for outputs
16	25MHz_0	O, SE	25MHz clock output
17	25MHz_1	O, SE	25MHz clock output
18	VSS_REF	GND	Ground for outputs.
19	XTAL_IN	I	25MHz crystal input
20	XTAL_OUT	O, SE	25MHz crystal output
21	VSS	GND	Ground for outputs.
22	33.33MHz/SMBADR	I/O	33.33MHz clock output/SMBus address select bit
23	VDD_33	PWR	3.3V power supply for outputs
24	RMII_5	O, SE	50MHz RMII clocks
25	RMII_4	O, SE	50MHz RMII clocks
26	VDD_RMII	PWR	3.3V power supply for outputs
27	VSS_RMII	GND	Ground for outputs.
28	RMII_3	O, SE	50MHz RMII clocks
29	RMII_2	O, SE	50MHz RMII clocks
30	VSS_RMII	GND	Ground for outputs.
31	VDD_RMII	PWR	3.3V power supply for outputs
32	RMII_1	O, SE	50MHz RMII clocks
33	RMII_0	O, SE	50MHz RMII clocks
34	VDDIO_RGMII	PWR	Power supply for 125MHz RGMII output.

Pin Description (continued)

Pin #	Name	Type	Description
35	VSS_RGMII	GND	Ground for outputs.
36	RGMII_1	O, SE	125MHz SE Output
37	RGMII_0	O, SE	125MHz SE Output
38	SCLK	I	Serial Interface bus clock input.
39	SDATA	I/O	Serial Interface bus data input and output.
40	PWRGD/PWRDWN#	I	3.3V LVTTL input. It acts as a level sensitive strobe.

Block Diagram



PD# (Power Down) Clarification

The PWRGD/PWRDWN# pin is a dual function pin. During initial power-up, the pin functions as PWRGD. Once PWRGD/PWRDWN# has been sampled low by the device, the pin assumes PWRDWN# functionality. The PWRDWN# pin is an asynchronous active low input used to shut off ALL clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. When PWRDWN# is asserted low, all clocks are driven to a low value and held prior to turning off the VCOs and the crystal oscillator.

Table 1. PD# Functionality

PD#	CPU	CPU#	DOT_96	DOT_96#	50MHz	33.3MHz	25MHz	32.768kHz
1	Normal	Normal	Normal	Normal	50MHz	33.3MHz	25MHz	32.768kHz
0	Iref*2 or Float	Float	Iref*2 or Float	Float	Low	Iref*2 or Float	Low	Low

PWRDWN# - Assertion

When PWRDWN# is sampled low by two consecutive rising edges of CPU, all single-ended outputs will be held low on their next high to low transition and differential clocks will be held high or tristated (depending on the state of the control register drive mode bit) on the next “Diff clock#” high to low transition.

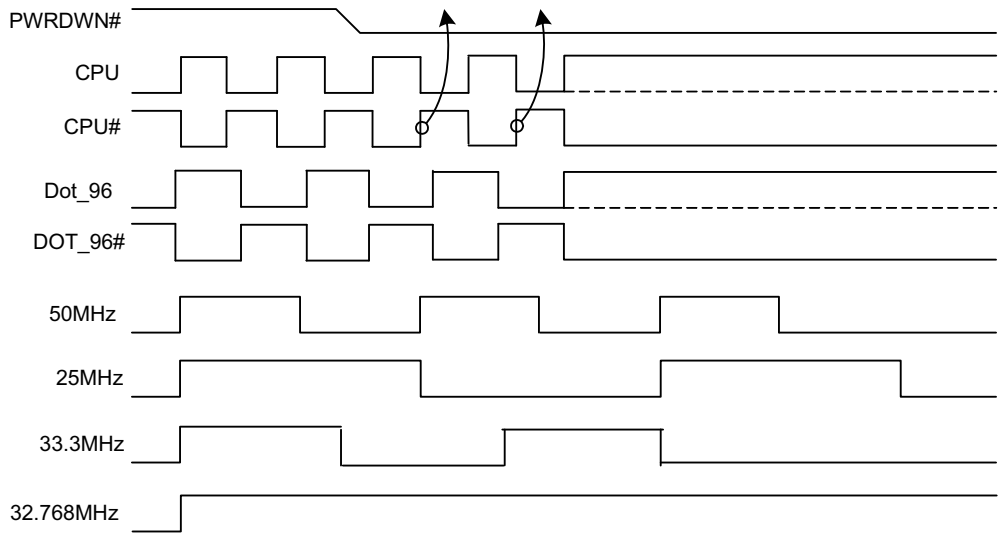


Figure 1. Power Down Assertion

PWRDWN# De-assertion

The power-up latency is less than 2.5ms. This is the time from the de-assertion of the PWRDWN# pin or the ramping of the power supply until the time that stable clocks are output from the clock device. All differential outputs stopped in a tristate condition resulting from power down will be driven high in less than 300us of PWRDWN# de-assertion to voltage greater than 200mV. After the clock chip’s internal PLL is powered up and locked, all outputs are to be enabled within a few clock cycles of each other. Below is an example showing the relationship of clocks coming up. Unfortunately, we cannot show all possible combinations, designers need to insure that from the first active clock output to the last takes no more than two full clock cycles.

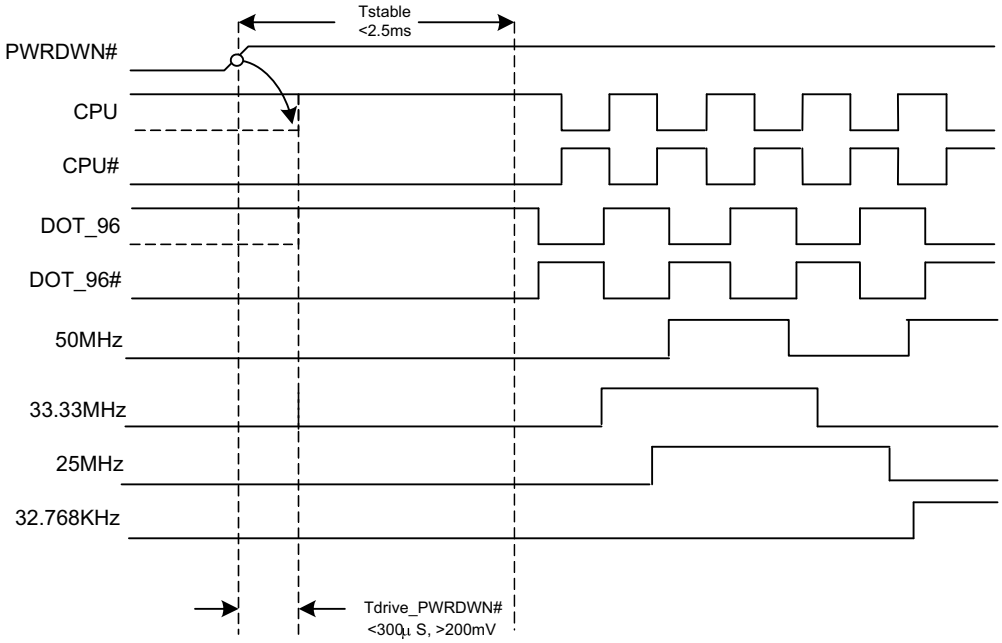


Figure 2. Power Down De-assertion

Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 2*. The slave receiver address is related to SMBADR.

Table 2. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit'00000000' stands for block operation	11:18	Command Code - 8 Bit'00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	-	Reserved	X
6	-	Reserved	X
5	-	Reserved	X
4	RW	DOT_96 Spread Spectrum Enable 0 = Disabled 1 = Enabled	0
3	RW	Differential Clock Spread Spectrum Enable 0 = Disabled 1 = Enabled	0
2	RW	Frequency Select Bit FS2 0 = Disabled 1 = Enabled	1
1	RW	Frequency Select Bit FS1 0 = Disabled 1 = Enabled	0
0	RW	Frequency Select Bit FS0 0 = Disabled 1 = Enabled	1

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	RMII5 (50MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
6	RW	RMII4 (50MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
5	RW	RMII3 (50MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
4	RW	RMII2 (50MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
3	RW	RMII1 (50MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
2	RW	RMII0 (50MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1

Control Register 1 (continued)

Bit	Type	Description/Function	Power up condition
1	RW	RGMII1 (125MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
0	RW	RGMII0 (125MHz) Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1

Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	CPU Drive Mode 0 = Driven 1 = Hi-Z	0
6	RW	DOT_96 Drive Mode 0 = Driven 1 = Hi-Z	0
5	RW	33.33MHz Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
4	RW	25MHz_1 Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
3	RW	25MHz_0 Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
2	RW	32.768KHz Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
1	RW	CPU Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1
0	RW	DOT_96 Output Enable 0 = Disabled 1 = Enabled (Disabled = Low)	1

Control Register 3

Bit	Type	Description/Function	Power up condition
7	-	Reserved	X
6	-	Reserved	X
5	-	Reserved	X
4	-	Reserved	X

Control Register 3 (continued)

Bit	Type	Description/Function	Power up condition
3	RW	DOT_96 FS3	0
2	RW	DOT_96 FS2	0
1	RW	DOT_96 FS1	0
0	RW	DOT_96 FS0	0

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	RMII5 Strength Control 0 = 1x Strength 1 = 2x Strength	0
6	RW	RMII4 Strength Control 0 = 1x Strength 1 = 2x Strength	0
5	RW	RMII3 Strength Control 0 = 1x Strength 1 = 2x Strength	0
4	RW	RMII2 Strength Control 0 = 1x Strength 1 = 2x Strength	0
3	RW	RMII1 Strength Control 0 = 1x Strength 1 = 2x Strength	0
2	RW	RMII0 Strength Control 0 = 1x Strength 1 = 2x Strength	0
1	RW	RGMII1 Strength Control 0 = 1x Strength 1 = 2x Strength	0
0	RW	RGMII0 Strength Control 0 = 1x Strength 1 = 2x Strength	0

Control Register 5

Bit	Type	Description/Function	Power up condition
7	-	Reserved	X
6	-	Reserved	X
5	RW	33.33MHz Strength Control 0 = 1x Strength 1 = 2x Strength	1
4	RW	25MHz_1Strength Control 0 = 1x Strength 1 = 2x Strength	1
3	RW	25MHz_0 Strength Control 0 = 1x Strength 1 = 2x Strength	1

Control Register 5 (continued)

Bit	Type	Description/Function	Power up condition
2	RW	32.768KHz Strength Control 0 = 1x Strength 1 = 2x Strength	1
1	-	Reserved	X
0	-	Reserved	X

Control Register 6

Bit	Type	Description/Function	Power up condition
7	R	Revision Code bit 3	0
6	R	Revision Code bit 2	0
5	R	Revision Code bit 1	0
4	R	Revision Code bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	Device ID 7	0
6	R	Device ID 6	0
5	R	Device ID 5	1
4	R	Device ID 4	0
3	R	Device ID 3	0
2	R	Device ID 2	0
1	R	Device ID 1	1
0	R	Device ID 0	0

Control Register 8

Bit	Type	Description/Function	Power up condition
7	RW	Byte Count bit 7	0
6	RW	Byte Count bit 6	0
5	RW	Byte Count bit 5	0
4	RW	Byte Count bit 4	0
3	RW	Byte Count bit 3	1
2	RW	Byte Count bit 2	0
1	RW	Byte Count bit 1	0
0	RW	Byte Count bit 0	1

Crystal Recommendations

The SLG84503 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG84503 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 3. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Overtone	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
25.00000MHz	AT	Parallel	20pF	0.1mW	Fundamental	35ppm	15ppm	5ppm

Absolute Maximum Ratings

Storage Temperature:–65°C to + 150°C

Supply Voltage (VDDA):-0.5 to 4.6V

Supply Voltage (VDD):-0.5 to 4.6V

3.3V Input Voltage:-0.5 to 4.6V

Operating Temperature (Ambient):0°C to +70°C

ESD Protection (Min):2000V

Lead Frame Material (for Green package): Sn/Bi

Reflow Temperature (for Green package): 260°C (10sec)

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDA	3.3V Core Supply Voltage	3.3V±5%	3.135		3.465	V
VDD	3.3V I/O Supply Voltage	3.3V±5%	3.135		3.465	V
VDDIO_RGMII	3.3V I/O Supply Voltage	3.3V±5%	3.135	3.3	3.465	V
V_{ih}	3.3V Input High Voltage	VDD	2.0		VDD+0.3	V
V_{il}	3.3V Input Low Voltage		VSS-0.3		0.8	V
V_{oh}	3.3V Output High Voltage	I_{oh} = -1mA	2.4			V
V_ol	3.3V Output Low Voltage	I_{ol} = 1mA			0.4	V
I_{il}	Input Leakage Current	0 < V_{in} < VDD	-5		+5	uA
C_{in}	Input Pin Capacitance		2.5		6	pF
C_{xtal}	Xtal Pin Capacitance		3		5	pF
C_{out}	Output Pin Capacitance		2.5		6	pF
L_{pin}	Pin Inductance				7	nH
$I_{dd\_PD\_DR}$	Powerdown Current	VDD = 3.465V All static inputs = VDD or VSS All differential pairs driven			70	mA
$I_{dd\_ON\_TRI}$	Powerdown Current	VDD = 3.465V All static inputs = VDD or VSS All differential pairs tristated			12	mA

Differential 0.7V Timing Characteristics

CPU Timing Characteristics (SSC Disabled)

Symbol	Description	Min.	Max.	Unit	Notes
$L_{accurracy}$	Long term accuracy	-	100	ppm	
T_{period}	Average Period	7.4993	7.5008	ns	
T_{abs}	Absolute Min/Max Host CLK period	7.4143	7.6235	ns	
T_{rise}	Rise Time	175	700	ps	
T_{fall}	Fall Time	175	700	ps	
T_{rise}	Rise Time variation	-	125	ps	
T_{fall}	Fall Time variation	-	125	ps	
Rise/Fall Matching	Rise/Fall Matching	-	20	%	
V_{High}	Voltage High	660	850	mV	
V_{Low}	Voltage Low	-150	-	mV	
$V_{cross(abs)}$	Absolute Crossing Point Voltages	250	550	mV	
$V_{cross(rel)}$	Relative Crossing Point Voltages	Calc	Calc	-	
Total V_{cross}	Total Variation of Vcross Over All Edges	-	140	mV	
Edge_rate	Edge Rate	0.5	2.0	V/ns	
$T_{jcyc-cyc}$	Cycle to Cycle Jitter	-	85	ps	
Duty Cycle	Duty Cycle	35	65	%	
V_{ovs}	Maximum Voltage (Overshoot)	-	VH+0.3V	V	
V_{uds}	Maximum Voltage (Undershoot)	-0.3	-	V	
V_{rb}	Ringback Voltage	N/A	0.2	V	

Differential 0.7V Timing Characteristics

CPU Timing Characteristics (SSC Enabled)

Symbol	Description	Min.	Max.	Unit	Notes
$L_{accurracy}$	Long term accuracy	-	100	ppm	
T_{period}	CLK period	7.4993	7.5385	ns	
T_{abs}	Absolute Min/Max Host CLK period	7.4143	7.6235	ns	
T_{rise}	Rise Time	175	700	ps	
T_{fall}	Fall Time	175	700	ps	
T_{rise}	Rise Time variation	-	125	ps	
T_{fall}	Fall Time variation	-	125	ps	
Rise/Fall Matching	Rise/Fall Matching	-	20	%	
V_{High}	Voltage High	660	850	mV	
V_{Low}	Voltage Low	-150	-	mV	
$V_{cross(abs)}$	Absolute Crossing Point Voltages	250	550	mV	
$V_{cross(rel)}$	Relative Crossing Point Voltages	Calc	Calc	-	
Total V_{cross}	Total Variation of Vcross Over All Edges	-	140	mV	
Edge_rate	Edge Rate	0.5	2.0	V/ns	
$T_{jcyc-cyc}$	Cycle to Cycle Jitter	-	85	ps	
Duty Cycle	Duty Cycle	45	55	%	
V_{ovs}	Maximum Voltage (Overshoot)	-	VH+0.3V	V	
V_{uds}	Maximum Voltage (Undershoot)	-0.3	-	V	
V_{rb}	Ringback Voltage	N/A	0.2	V	

DOT Timing Characteristics (SSC Disabled)

Symbol	Description	Min.	Max.	Unit	Notes
$L_{accurracy}$	Long term accuracy	-	300	ppm	
T_{period}	CLK period	10.4135	10.4196	ns	
T_{abs}	Absolute Min/Max Host CLK period	10.1635	10.7222	ns	
T_{rise}	Rise Time	175	700	ps	
T_{fall}	Fall Time	175	700	ps	
T_{rise}	Rise Time variation	-	125	ps	
T_{fall}	Fall Time variation	-	125	ps	
Rise/Fall Matching	Rise/Fall Matching	-	20	%	
V_{High}	Voltage High	660	850	mV	
V_{Low}	Voltage Low	-150	-	mV	
$V_{cross(abs)}$	Absolute Crossing Point Voltages	250	550	mV	
$V_{cross(rel)}$	Relative Crossing Point Voltages	Calc	Calc	-	
Total V_{cross}	Total Variation of Vcross Over All Edges	-	140	mV	
Edge_rate	Edge Rate	0.5	2.0	V/ns	
$T_{jcyc-cyc}$	Cycle to Cycle Jitter	-	250	ps	

DOT Timing Characteristics (SSC Disabled)

Symbol	Description	Min.	Max.	Unit	Notes
Duty Cycle	Duty Cycle	45	55	%	
V_{ovs}	Maximum Voltage (Overshoot)	-	VH+0.3V	V	
V_{uds}	Maximum Voltage (Undershoot)	-0.3	-	V	
V_{rb}	Ringback Voltage	N/A	0.2	V	

AC Electrical Characteristics

RMII 50MHz Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Notes
$L_{accurracy}$	Long term accuracy	-	50	ppm	2, 4
T_{period}	CLK period	19.99900	20.00100	ns	2, 3
T_{rise}	Rise Time	1.0	3.0	ns	
T_{fall}	Fall Time	1.0	3.0	ns	
$T_{jcyc-cyc}$	Cycle to Cycle Jitter	-	250	ps	2
Duty Cycle	Duty Cycle	35	65	%	

RGMII 125MHz Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{skewT}	Data to Clock output Skew (at transmitter)	-500	0	500	ps	
T_{skewR}	Data to Clock input Skew (at receiver)	1	-	2.6	ns	1
T_{cyc}	Clock cycle Duration	7.2	8	8.8	ns	2
$Duty_G$	Duty Cycle for Gigabit	45	50	55	%	3
$Duty_T$	Duty Cycle for 10/100T	40	50	60	%	3
$T_{jcyc-cyc}$	Cycle to Cycle Jitter	-	-	250	ps	2
T_R/T_F	Rise/Fall Time (20-80%)	-	-	0.75	ns	

33.33MHz Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
$L_{accurracy}$	Long term accuracy	-	300	ppm	2, 4
T_{period}	CLK period	29.99100	30.00900	ns	2,3
T_{rise}	Rise Time	0.5	2.0	ns	
T_{fall}	Fall Time	0.5	2.0	ns	
$T_{jcyc-cyc}$	Cycle to cycle jitter	-	350	ps	2
Duty Cycle	Duty Cycle	45	55	%	

25MHz Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
$L_{accurracy}$	Long term accuracy	-	50	ppm	2, 4
T_{rise}	CLK period	39.99800	40.00200	ns	2, 3
T_{fall}	CLK high time	0.5	2.0	ns	
T_{low}	CLK low time	0.5	2.0	ns	
$T_{jcyc-cyc}$	Cycle to cycle jitter	-	500	ps	2
Duty Cycle	Duty Cycle	45	55	%	

32.768 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
$L_{accurracy}$	Long term accuracy	-	300	ppm	2, 4
T_{period}	CLK period	30.50685	30.52515	us	2,3
T_{rise}	CLK high time	0.5	2.0	ns	
T_{fall}	CLK low time	0.5	2.0	ns	
$T_{jcyc-cyc}$	Cycle to cycle jitter	-	500	ps	2
Duty Cycle	Duty Cycle	45	55	%	

[1] Edge rate measured from 0.8V to 2.0V

[2] Duty cycle, Period and Jitter are measured with respect to 1.5V

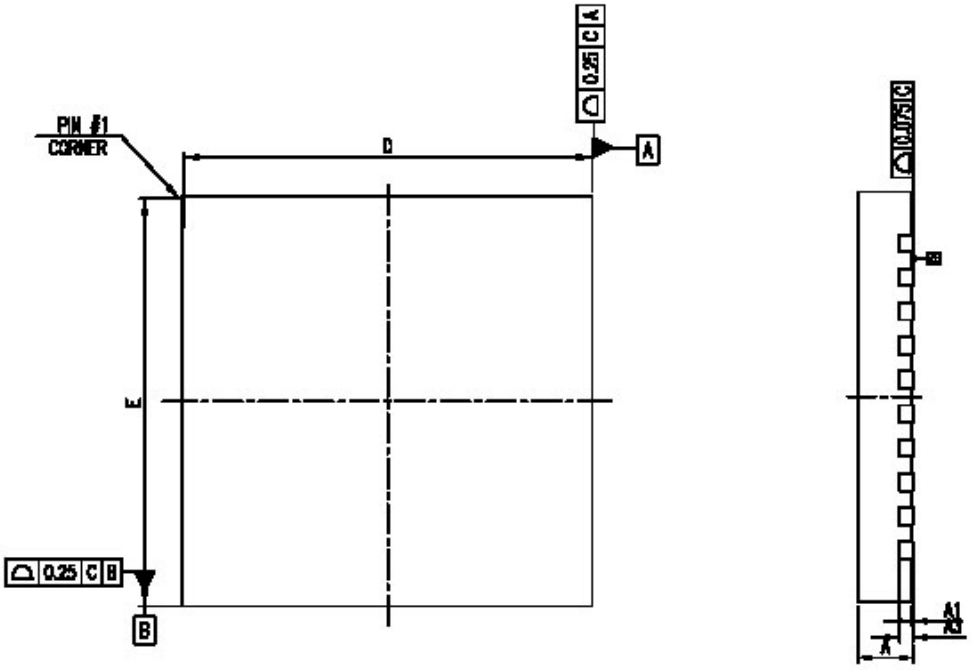
[3] The average period over any 1us period of time

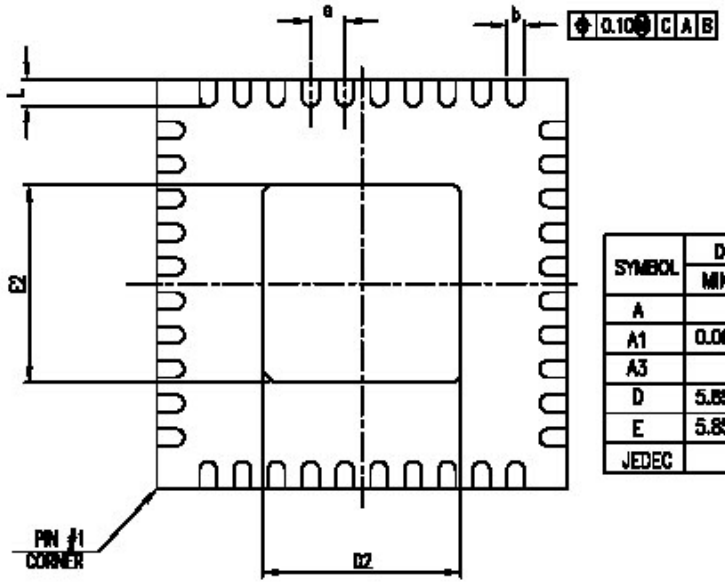
[4] Using frequency counter with the measurement interval equal or greater than 0.15s, the target frequencies are 50MHz, 33.333MHz, 25MHz, 32,768kHz

Ordering Information

Part Number	Package Type	Temperature Range
SLG84503V	40-LEAD QFN	Commercial, 0° to 70°C
SLG84503VTR	40-LEAD QFN - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions - 40 Lead QFN Package





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A		0.80	0.84		0.031	0.033
A1	0.00	0.02	0.04	0.00	0.0008	0.0015
A3	0.20 REF.			0.008 REF.		
D	5.85	6.00	6.15	0.230	0.236	0.242
E	5.85	6.00	6.15	0.230	0.236	0.242
JEDEC	MO-220					

N	b			D2			E2			e	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
40L	0.20	0.25	0.30	2.85	2.90	2.95	2.85	2.90	2.95	0.500 BSC	0.35	0.40	0.45	MO-220VAJD-5