IXF1010 10-Port 100/1000 Mbps Ethernet Media Access Controller

Preliminary Datasheet

IXF1010 is a 10-port 100/1000 Mbps Ethernet Media Access Controller (MAC) that supports IEEE 802.3 100 and 1000 Mbps applications. The device supports a System Packet Interface Level 4 Phase 2 (SPI4-2) system interface to the network processor or ASIC, and implements the Reduced Gigabit Media Independent Interface (RGMII), as defined in Version 1.2a of the Hewlett-Packard specification, for PHY connectivity. The RGMII reduces the interface pin count from GMII to allow for higher port densities.

Applications

In general, the IXF1010 is appropriate for high-end switching applications where MAC functions are not integrated into the switch/network processor.

- High-End Ethernet Switches
- Multi-Service Ethernet Switches
- High-End Ethernet LAN/WAN Routers

Product Features

- Supports 10 independent 100/1000 full-duplex Ethernet MAC ports
- System Packet Interface Level 4 Phase 2 (SPI4-2)
  - Capable of data transfers up to 12.8 Gbps
  - Supports dynamic phase alignment
- RGMII interface for PHY Ethernet connectivity
- 32-bit CPU interface
- RMON statistics
- JTAG and boundary scan capable
- Compliance with IEEE 802.3 MII Management Interface (MDIO)
- Compliance with IEEE 802.3x Standard for flow control
- Jumbo frame support for 10 KB packets
- .18 µ CMOS process technology
- Internal 17.0 KB receive FIFO and 4.5 KB transmit FIFO per channel
- Independent enable/disable of any port
- Detection short or overly large packets
- Error counters for dropped and errored packets
- CRC calculation and error detection
- Programmable option to:
  - Filter packets with errors
  - Filter, broadcast, multicast, and unicast address packets
  - Automatically pad transmitted packets less than the minimum frame size
- 552-Ceramic Ball Grid Array (CBGA)
- 1.8 V and 2.5 V operation
- Power consumption: 480 mW per-port typical

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Contents

Document #: 249839
Revision #: 001
Rev. Date: April 29, 2002

Figures

Tables

Document #: 249839
Revision #: 001
Rev. Date: April 29, 2002

1.0 General Description

IXF1010 is a 10-port 100/1000 Mbps Ethernet Media Access Controller (MAC). The 10 Gigabit interface to the network processor is supported through a System Packet Interface Level 4 Phase 2 (SPI4-2), while the PHY interface is RGMII (Reduced Gigabit Media Independent Interface). Figure 1 represents the IXF1010 block diagram and Figure 2 illustrates the IXF1010 system block diagram.

Figure 1. IXF1010 Block Diagram

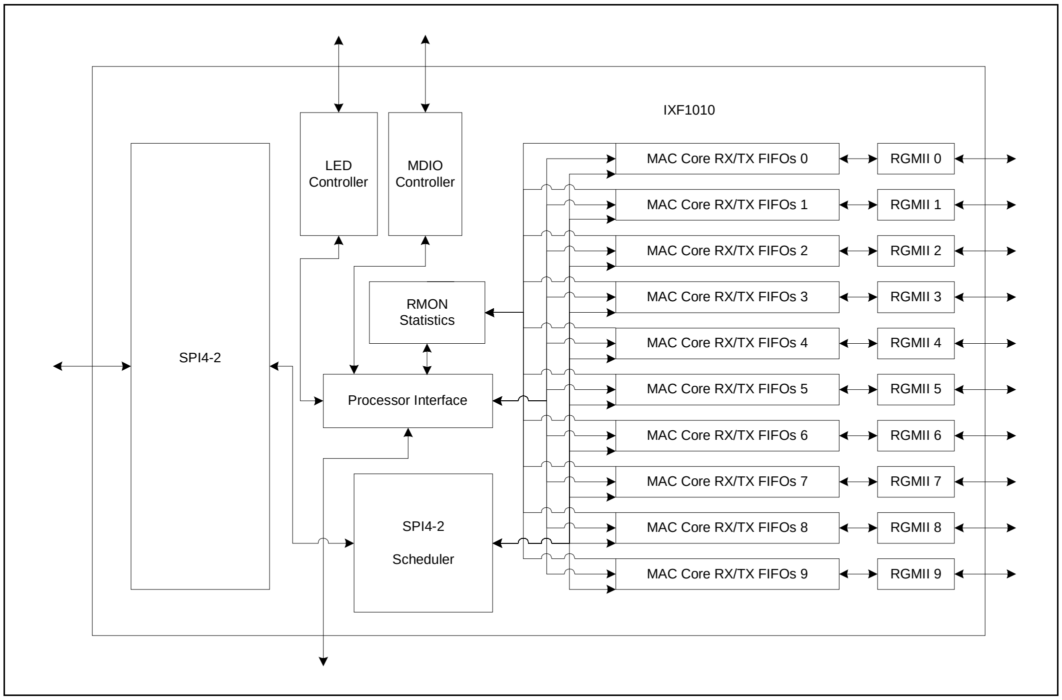


Figure 2. IXF1010 System Block Diagram

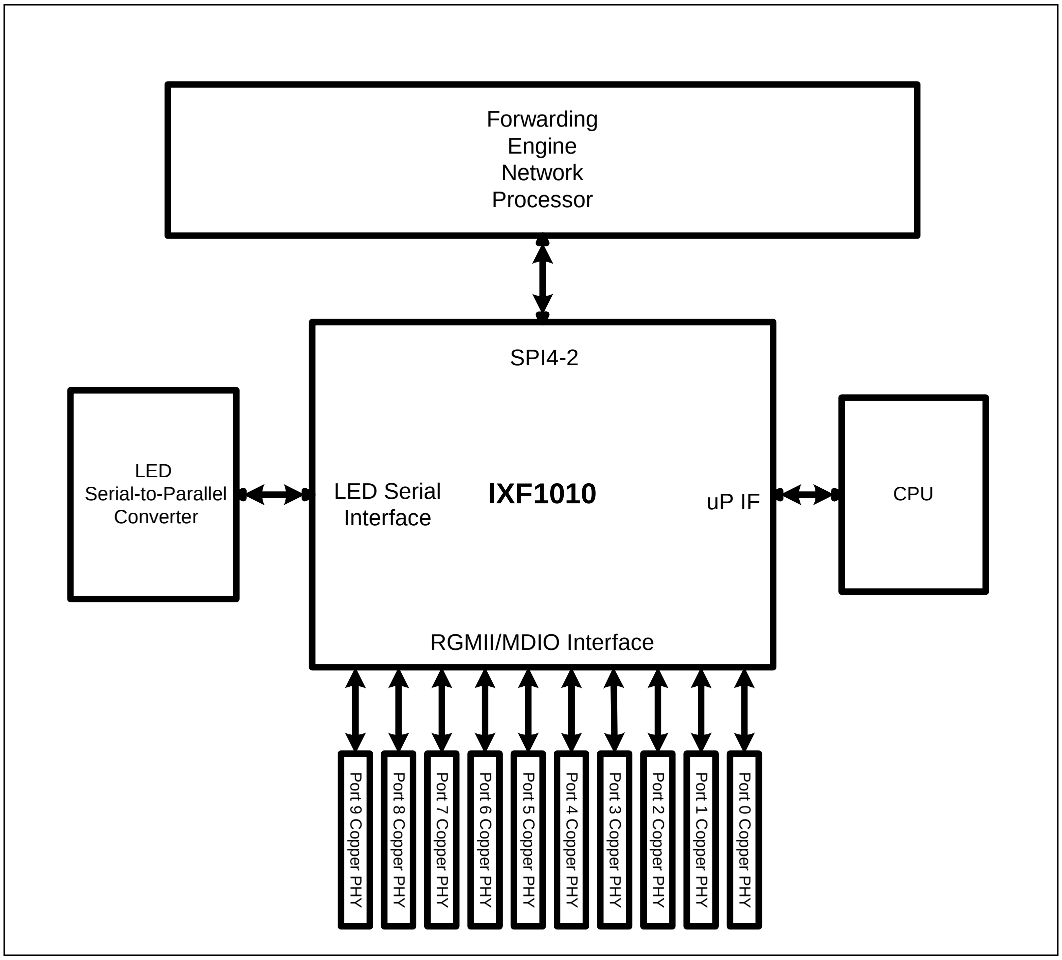


Figure 3 provides the physical layout of the balls, labeled with their ball number (matrix layout) and signal name.

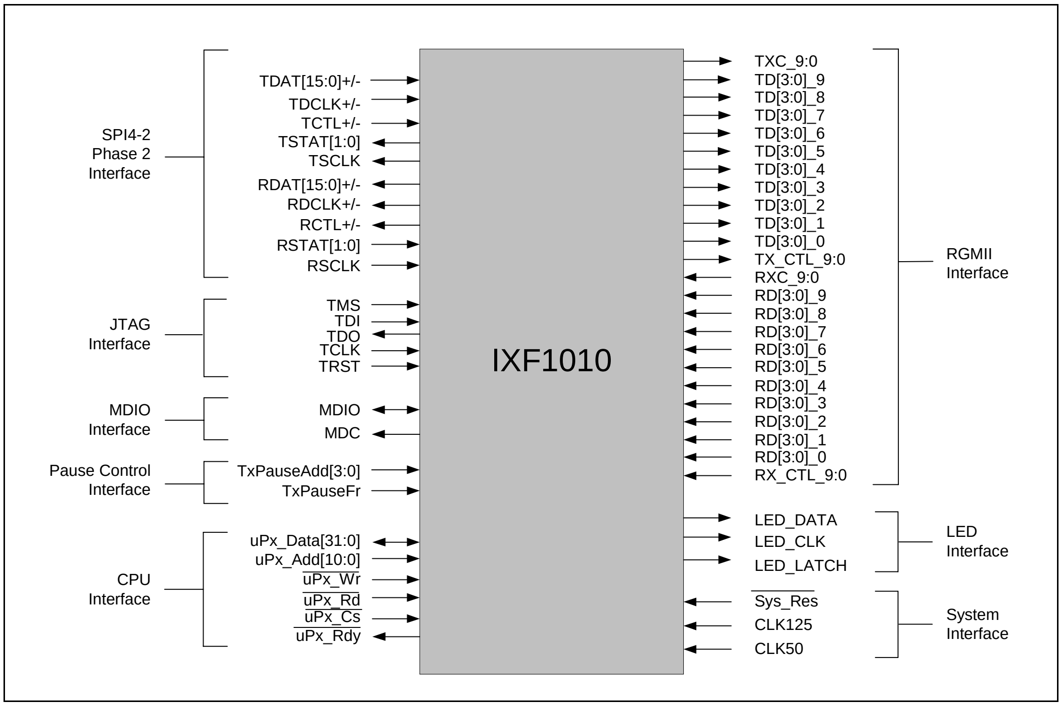
Figure 3. IXF1010 552-Ceramic Ball Grid Array (CBGA) Assignments (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	No Pad	No Ball	No Ball	uPx_Data1	N/C	N/C	uPx_Data3	uPx_Data7	uPx_Data9	uPx_Data8	uPx_Data 11	uPx_Data 19	RDAT12+	RDAT12-	uPx_Data 20	uPx_Data 25	uPx_Data 27	uPx_W	LED_CLK	LED_DATA	uPx_Data 29	No Ball	No Ball	No Ball	A
B	No Ball	No Ball	uPx_Data0	VDD2	TDAT2+	GND	TDAT9+	VDD2	uPx_Data2	GND	N/C	VDD2	VDD2	N/C	GND	uPx_Data 22	VDD2	uPx_Data 28	GND	RDAT1+	VDD2	uPx_Data 30	No Ball	No Ball	B
C	No Ball	uPX_Add 10	uPx_Add7	GND	TDAT2-	TDAT7-	TDAT7+	TDAT9-	TDAT14+	N/C	TSCLK	uPx_Data4	uPx_Data6	uPx_Data 17	N/C	RDAT8+	uPx_Data 26	RDCLK+	RDCLK-	RDAT1-	CLK50	uPx_Rdy	uPx_Data 31	No Ball	C
D	AVDD	VDD2	TDCLK+	GND	GND	VDD	uPx_Data 15	GND	TDAT14-	VDD	VDD	GND	GND	uPX_Data 16	VDD	RDAT8-	GND	RDAT9+	VDD	VDD	GND	GND	VDD2	GND	D
E	GND	uPx_Add5	uPx_Add4	TDCLK-	TSTAT0	TSTAT1	TDAT11-	TDAT11+	TDAT10+	uPx_Data 13	uPx_Data5	uPx_Data 10	RDAT13+	RDAT13-	uPx_Data 23	RDAT6+	RDAT6-	RDAT9-	RDAT0+	RDAT0-	VDD	N/C	N/C	AVDD	E
F	uPx_Add9	GND	uPx_Add2	VDD	uPx_Add8	GND	TDAT4+	VDD2	TDAT10-	GND	uPx_Data 14	VDD2	VDD2	uPx_Data 18	GND	RDAT14+	VDD2	RDAT2+	GND	uPx_Cs	VDD	N/C	GND	N/C	F
G	uPx_Add6	TxPause Add1	TxPause Add0	uPx_Add1	TDAT5+	TDAT4-	N/C	N/C	TDAT3+	VDD2	TDAT15+	uPx_Data 12	uPx_Data 21	uPx_Data 24	N/C	RDAT14-	RDAT10+	RDAT10-	RDAT2-	N/C	RDAT3+	N/C	N/C	N/C	G
H	uP_Add3	VDD2	TDAT1+	GND	TDAT5-	VDD2	TDAT12+	GND	TDAT3-	VDD	TDAT15-	GND	GND	uPx_Rd	VDD	RCTL+	GND	RCTL-	VDD2	RDAT3-	GND	MDC	VDD2	N/C	H
J	uPx_Add0	TxPause Add2	TDAT1-	VDD	TDAT0-	TDAT0+	TxPauseFr	TDAT12-	TDAT13+	GND	VDD	VDD2	VDD2	VDD	GND	RDAT11+	RSCLK	RDAT4+	RDAT4-	RSTAT1	RXC_0	MDIO	GND	N/C	J
K	TxPause Add3	GND	VDD	VDD	VDD	GND	N/C	VDD	GND	TDAT13-	GND	RDAT15+	RDAT15-	GND	RDAT11-	GND	VDD	LED_ LATCH	GND	RD2_0	VDD	RD0_0	GND	RD1_0	K
L	TX_CTL_9	TD1_9	RX_CTL_9	RD0_9	TDAT8+	RD1_6	TDAT6-	TDAT6+	VDD	GND	VDD	GND	GND	VDD	GND	VDD	RDAT5+	RDAT5-	N/C	RSTAT0	TD2_0	TD3_0	TD0_0	RX_CTL_0	L
M	TD2_9	VDD2	RD1_9	GND	TDAT8-	VDD2	N/C	GND	VDD2	TCTL+	GND	VDD2	VDD2	GND	RDAT7+	VDD2	GND	RD3_0	VDD2	TX_CTL_3	GND	RD0_1	VDD2	TD1_0	M
N	TXC_9	VDD2	N/C	GND	TXC_8	VDD2	N/C	GND	VDD2	TCTL-	GND	VDD2	VDD2	GND	RDAT7-	VDD2	GND	TRST	VDD2	TD2_1	GND	N/C	VDD2	TX_CTL_0	N
P	RD2_9	TD3_9	N/C	TD0_9	N/C	N/C	N/C	TD1_8	VDD	GND	VDD	GND	GND	VDD	GND	VDD	TD0_1	N/C	N/C	N/C	RXC_3	N/C	RD3_1	RD1_1	P
R	RXC_9	GND	RD3_9	VDD	TD2_8	GND	TX_CTL_8	VDD	GND	RXC_6	GND	TD3_3	TD2_3	GND	TD1_3	GND	VDD	N/C	GND	TXC_1	VDD	TXC_0	GND	RX_CTL_1	R
T	N/C	TD3_8	N/C	TX_CTL_6	N/C	TD0_8	RD2_8	RX_CTL_6	RD2_6	GND	VDD	VDD2	VDD2	VDD	GND	TMS	RD2_3	RX_CTL_3	RD1_3	GND	RD2_1	GND	RXC_1	GND	T
U	N/C	VDD2	N/C	GND	N/C	VDD2	RD1_8	GND	RD0_6	VDD	TX_CTL_5	GND	GND	RD0_4	VDD	RD3_3	GND	RD0_3	VDD2	GND	GND	GND	VDD2	GND	U
V	N/C	RD3_6	GND	GND	GND	N/C	RD0_8	N/C	TD2_5	N/C	N/C	TD3_5	RD3_4	N/C	N/C	RD2_4	TD3_1	N/C	N/C	N/C	N/C	N/C	TD1_1	GND	V
W	N/C	GND	GND	VDD	RD3_8	GND	RXC_7	VDD2	TD1_6	GND	TD1_5	VDD2	VDD2	TD1_4	GND	TXC_4	VDD2	TD0_4	GND	RX_CTL_2	VDD	N/C	GND	GND	W
Y	AVDD	GND	GND	Sys_Res	GND	GND	TD0_6	RD3_7	TD3_6	TD0_5	TXC_6	RD3_5	RD1_5	N/C	GND	RD1_4	TD1_2	RXC_4	N/C	N/C	TX_CTL_1	N/C	N/C	TDO	Y
AA	GND	VDD2	RX_CTL_8	GND	CLK125	VDD	RX_CTL_7	GND	RD0_7	VDD	TXC_5	GND	GND	RX_CTL_4	VDD	TX_CTL_2	GND	RD0_5	VDD	TD2_4	GND	TD0_3	VDD2	TCLK	AA
AB	No Ball	TX_CTL_7	N/C	VDD	N/C	RXC_8	RD2_7	TD2_6	N/C	RD2_5	N/C	N/C	GND	GND	TD3_4	GND	RXC_5	TD0_2	TXC_3	N/C	RD3_2	N/C	RXC_2	No Ball	AB
AC	No Ball	No Ball	TD3_7	VDD2	TD1_7	GND	RD1_7	VDD2	N/C	GND	RX_CTL_5	VDD2	VDD2	TX_CTL_4	GND	GND	VDD2	TDI	GND	RD2_2	VDD2	RD0_2	No Ball	No Ball	AC
AD	No Ball	No Ball	No Ball	TD2_7	TD0_7	TXC_7	N/C	N/C	N/C	N/C	N/C	N/C	GND	GND	GND	GND	N/C	TD3_2	TD2_2	TXC_2	RD1_2	No Ball	No Ball	No Ball	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

2.0 Pin Assignments and Signal Descriptions

Figure 4 and Table 1 through Table 3 provide the signal pins used by the IXF1010

Figure 4. IXF1010 Pinout Diagram



2.1 Signal Name Conventions

Signal names may contain either a port designation (PHY interface) or a serial designation (System Interface). Signal naming conventions are as follows:

Port Designation. Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by an underscore and the Port Designation. For example, RGMII Transmit Control signals would be identified as TX_CTL_0, TX_CTL_1, TX_CTL_2, etc.

Serial Designation. A set of signals that are not tied to any specific port are designated by the Signal Mnemonic, followed by an bracketed serial designation. For example, SPI4-2 Transmit Data Bus signals would be identified as TDAT[15:0].

Port Bus Designation: A set of bus signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by a bracketed bus designation, followed by an underscore and the port designation. For example, RGMII transmit data bus signals would be identified as TD[3:0]_0, TD[3:0]_1, TD[3:0]_2, etc.

Document #: 249839
Revision #: 001
Rev. Date: April 29, 2002

Table 1. IXF1010 Signal Pins

Ball Designator	Signal Name	Type	Standard	Signal Description
SPI4-2 Interface				
G11, C9, J9, H7, E8, E9, B7, L5, C7, L8, G5, F7, G9, B5, H3, J6	TDAT15+, TDAT14+, TDAT13+, TDAT12+, TDAT11+, TDAT10+, TDAT9+, TDAT8+, TDAT7+, TDAT6+, TDAT5+, TDAT4+, TDAT3+, TDAT2+, TDAT1+, TDAT0+,	Input	LVDS	**Transmit Data Bus:** Used to carry payload data and in-hand control words to the IXF1010 link-layer device
H11, D9, K10, J8, E7, F9, C8, M5, C6, L7, H5, G6, H9, C5, J3, J5	TDAT15-, TDAT14-, TDAT13-, TDAT12-, TDAT11-, TDAT10-, TDAT9-, TDAT8-, TDAT7-, TDAT6-, TDAT5-, TDAT4-, TDAT3-, TDAT2-, TDAT1-, TDAT0-,	Input	LVDS	**Transmit Data Bus:** Used to carry payload data and in-hand control words to the IXF1010 link-layer device
D3, E4	TDCLK+, TDCLK-	Input	LVDS	**Transmit Data Clock:** Clock associated with TDAT and TCTL. Data and control lines are driven off the rising and falling edges of the clock
M10, N10	TCTL+, TCTL-	Input	LVDS	**Transmit Control:** TCTL is High when a control word is present on TDAT (15:0). Otherwise, TCTL is Low
C11	TSCLK	Input	CMOS 2.5V	**Transmit Status Clock:** Clock associated with TSTAT [1:0]
E6, E5	TSTAT1, TSTAT0	Input	CMOS 2.5V	**Transmit FIFO Status:** Used to carry round-robin FIFO status information, along with associated error detection and framing
K12, F16, E13, A13, J16, G17, D18, C16, M15, E16, L17, J18, G21, F18, B20, E19	RDAT15+, RDAT14+, RDAT13+, RDAT12+, RDAT11+, RDAT10+, RDAT9+, RDAT8+, RDAT7+, RDAT6+, RDAT5+, RDAT4+, RDAT3+, RDAT2+, RDAT1+, RDAT0+	Output	LVDS	**Receive Data:** Carries payload data and in-band control from the IXF1010 link-layer device
K13, G16, E14, A14, K15, G18, E18, D16, N15, E17, L18, J19, H20, G19, C20, E20	RDAT15-, RDAT14-, RDAT13-, RDAT12-, RDAT11-, RDAT10-, RDAT9-, RDAT8-, RDAT7-, RDAT6-, RDAT5-, RDAT4-, RDAT3-, RDAT2-, RDAT1-, RDAT0-	Output	LVDS	**Receive Data:** Carries payload data and in-band control from the IXF1010 link-layer device
C18, C19	RDCLK+, RDCLK-	Output	LVDS	**Receive Data Clock:** Clock associated with RDAT and RCTL. Data and control lines are driven off the rising and falling edges of the clock

Table 1. IXF1010 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
H16, H18	RCTL+, RCTL-	Output	LVDS	**Receive Control:** RCTL is High when a control word is present on RDAT[15:0]. Otherwise, RCTL is Low
J17	RSCLK	Input	CMOS 2.5V	**Receive Status Clock:** Clock associated with RSTAT [1:0]
J20, L20	RSTAT1, RSTAT0	Input	CMOS 2.5V	**Receive FIFO Status:** Used to carry round-robin FIFO status information, along with associated error detection and framing
RGMII Interface				
N1, N5, AD6, Y11, AA11, W16, AB19, AD20, R20, R22	TXC_9, TXC_8, TXC_7, TXC_6, TXC_5, TXC_4, TXC_3, TXC_2, TXC_1, TXC_0	Output	CMOS 2.5V	**Transmit Reference Clock**: Operates at: 125 MHz for 1 Gigabit operation 25 MHz for 100 Mbps operation
P2, M1, L2, P4, T2, R5, P8, T6, AC3, AD4, AC5, AD5, Y9, AB8, W9, Y7, V12, V9, W11, Y10, AB15, AA20, W14, W18, R12, R13, R15, AA22, AD18, AD19, Y17, AB18, V17, N20, V23, P17, L22, L21, M24, L23	TD[3:0]_9 TD[3:0]_8 TD[3:0]_7 TD[3:0]_6 TD[3:0]_5 TD[3:0]_4 TD[3:0]_3 TD[3:0]_2 TD[3:0]_1 TD[3:0]_0	Output	CMOS 2.5V	**Transmit Data:** This bus contains bits 3:0 on the rising edge of the TXC and bits 7:4 on the falling edge of TXC.
L1, R7, AB2, T4, U11, AC14, M20, AA16, Y21, N24	TX_CTL_9, TX_CTL_8, TX_CTL_7, TX_CTL_6, TX_CTL_5, TX_CTL_4, TX_CTL_3, TX_CTL_2, TX_CTL_1, TX_CTL_0	Output	CMOS 2.5V	**Transmit Control:** This signal is TXEN on the rising edge of TXC and a logical derivative of TXEN and TXERR on the falling edge.
R1, AB6, W7, R10, AB17, Y18, P21, AB23, T23, J21	RXC_9, RXC_8, RXC_7, RXC_6, RXC_5, RXC_4, RXC_3, RXC_2, RXC_1, RXC_0,	Input	CMOS 2.5V	**Receiver reference clock:** 125 MHz for 1 Gigabit operation 25 MHz for 100 Mbps operation
R3, P1, M3, L4, W5, T7, U7, V7, Y8, AB7, AC7, AA9, V2, T9, L6, U9, Y12, AB10, Y13, AA18, V13, V16, Y16, U14, U16, T17, T19, U18, AB21, AC20, AD21, AC22, P23, T21, P24, M22, M18, K20, K24, K22	RD[3:0]_9 RD[3:0]_8 RD[3:0]_7 RD[3:0]_6 RD[3:0]_5 RD[3:0]_4 RD[3:0]_3 RD[3:0]_2 RD[3:0]_1 RD[3:0]_0	Input	CMOS 2.5V	**Receive Data:** This bus contains bits 3:0 on the rising edge of the clock and bits 7:4 on the falling edge.

Table 1. IXF1010 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
L3, AA3, AA7, T8, AC11, AA14, T18, W20, R24, L24	RX_CTL_9, RX_CTL_8, RX_CTL_7, RX_CTL_6, RX_CTL_5, RX_CTL_4, RX_CTL_3, RX_CTL_2, RX_CTL_1, RX_CTL_0,	Input	CMOS 2.5V	**Receive Control:** This signal is RXDV on the rising edge of RXC and a logical derivative of RXDV and RXERR on the falling edge.
CPU Interface				
C2 F1 F5 C3 G1 E2 E3 H1 F3 G4 J1	uPx_Add10 uPx_Add9 uPx_Add8 uPx_Add7 uPx_Add6 uPx_Add5 uPx_Add4 uPx_Add3 uPx_Add2 uPx_Add1 uPx_Add0	Input	CMOS 2.5V	**Address bus**
F20	$\overline{\text{uPx\_Cs}}$	Input	CMOS 2.5V	**Chip Select Signal**
C23 B22 A21 B18 A17 C17 A16 G14 E15 B16 G13 A15 A12 F14 C14 D14 D7 F11 E10 G12 A11 E12 A9 A10 A8 C13 E11 C12 A7 B9 A4 B3	uPx_Data31 uPx_Data30 uPx_Data29 uPx_Data28 uPx_Data27 uPx_Data26 uPx_Data25 uPx_Data24 uPx_Data23 uPx_Data22 uPx_Data21 uPx_Data20 uPx_Data19 uPx_Data18 uPx_Data17 uPx_Data16 uPx_Data15 uPx_Data14 uPx_Data13 uPx_Data12 uPx_Data11 uPx_Data10 uPx_Data9 uPx_Data8 uPx_Data7 uPx_Data6 uPx_Data5 uPx_Data4 uPx_Data3 uPx_Data2 uPx_Data1 uPx_Data0	Bi_Dir	CMOS 2.5V	**Bi-directional data bus**
A18	$\overline{\text{uPx\_Wr}}$	Input	CMOS 2.5V	**Write Strobe**
H14	$\overline{\text{uPx\_Rd}}$	Input	CMOS 2.5V	**Read Strobe**

Document #: 249839
Revision #: 001
Rev. Date: April 29, 2002

Table 1. IXF1010 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
C22	$\overline{\text{uPx\_Rdy}}$	Output	CMOS 2.5V	Cycle complete indicator
Pause Control Interface				
J7	TxPauseFr	Input	CMOS 2.5V	Insert PAUSE frame control signal
K1 J2 G2 G3	TxPauseAdd3 TxPauseAdd2 TxPauseAdd1 TxPauseAdd0	Input	CMOS 2.5V	Port Selection for PAUSE frames
MDIO Interface				
J22	MDIO	Input/ Output	CMOS 2.5V	Management Data Input/Output
H22	MDC	Output	CMOS 2.5V	Management Clock to external devices
LED Interface				
A19	LED_CLK	Output	CMOS 2.5V	Clock output for the LED block
A20	LED_DATA	Output	CMOS 2.5V	Data output for the LED block
K18	LED_LATCH	Output	CMOS 2.5V	Latch enable for the LED block
JTAG Interface				
AA24	TCLK	Input	CMOS 2.5V	JTAG Test Clock
T16	TMS	Input	CMOS 2.5V	JTAG Test Mode Select
AC18	TDI	Input	CMOS 2.5V	JTAG Test Data Input
N18	TRST	Input	CMOS 2.5V	JTAG Test Reset
Y24	TDO	Output	CMOS 2.5V	JTAG Test Data Output
System Interface				
AA5	CLK125	Input	CMOS 2.5V	Input clock to PLL
C21	CLK50	Input	CMOS 2.5V	Input clock to SPI4-2 RX PLL
Y4	$\overline{\text{Sys\_Res}}$	Input	CMOS 2.5V	System hard reset (active Low)

Table 2. IXF1010 Power Supply Signal Descriptions

Ball #	Signal Name	Type	Standard	Signal Description
D6, D10, D15, D19, F4, F21, H10, H15, J11, J14, K4, K8, K17, K21, L9, L11, L14, L16, P9, P11, P14, P16, R4, R8, R17, R21, T11, T14, U10, U15, W4, W21, AA6, AA10, AA15, AA19, AB4	VDD	–	–	1.8V core supply.
B4, B8, B12, B13, B17, B21, D2, D23, F8, F12, F13, F17, H2, H6, H19, H23, J12, J13, M2, M6, M9, M12, M13, M16, M19, M23, N2, N6, N9, N12, N13, N16, N19, N23, T12, T13, U2, U6, U19, U23, W8, W12, W13, W17, AA2, AA23, AC4, AC8, AC12, AC13, AC17, AC21	VDD2	–	–	2.5V I/O supply.
B6, B10, B15, B19, D8, D12, D13, D17, F2, F6, F10, F15, F19, F23, H4, H8, H12, H13, H17, H21, J10, J15, K2, K6, K9, K11, K14, K16, K19, K23, L10, L12, L13, L15, M4, M8, M11, M14, M17, M21, N4, N8, N11, N14, N17, N21, P10, P12, P13, P15, R2, R6, R9, R11, R14, R16, R19, R23, T10, T15, U4, U8, U12, U13, U17, U21, W2, W6, W10, W15, W19, W23, AA8, AA12, AA13, AA17, AC6, AC10, AC15, AC19	GND	–	–	Ground return for all signals.

Document #: 249839
Revision #: 001
Rev. Date: April 29, 2002

Table 3. IXF1010 Unused Balls/Reserved

Ball #	Signal Name	Type	Standard	Signal Description
A5, A6, B11, B14, C10, C15, E22, E23, F22, F24, G7, G8, G15, G20, G22, G23, G24, H24, J24, K7, L19, M7, N3, N7, N22, P3, P5, P6, P7, P18, P19, P20, P22, R18, T1, T3, T5, U1, U3, U5, V1, V6, V8, V10, V11, V14, V15, V18, V19, V20, V21, V22, W1, W22, Y14, Y19, Y20, Y22, Y23, AB3, AB5, AB9, AB11, AB12, AB20, AB22, AC9, AD7, AD8, AD9, AD10, AD11, AD12, AD17	N/C	–	–	No connection.
A2, A3, A22, A23, A24, B1, B2, B23, B24, C1, C24, AB1, AB24, AC1, AC2, AC23, AC24, AD1, AD2, AD3, AD22, AD23, AD24	No Ball	–	–	Balls removed from substrate.
A1	No Pad	–	–	Pad removed from substrate.

3.0 Functional Descriptions

3.1 Media Access Controller (MAC)

3.1.1 General Description

The main functional block used in the IXF1010 consists of a 100/1000 Mbps Ethernet MAC. The MAC supports the following features:

- Full compliance with the Reduced Gigabit Media Independent Interface (RGMII)
- 100/1000 Mbps full-duplex operation
- Independent enable/disable of any port
- Detection of length error, and runt or overly large packets
- RMON statistics and error counters
- Cyclic Redundancy Check (CRC) calculation and error detection
- Programmable option to:
  - Filter packets with errors
  - Filter, broadcast, multicast, and unicast address packets
  - Automatically pad transmitted packets less than the minimum frame size
- Compliance with IEEE 802.3x Standard for Flow Control (symmetric pause capability)

The MAC is fully integrated, designed for use with Ethernet 802.3 Frame types, and is compliant to all of the required IEEE 802.3 MAC requirements.

The MAC adds preamble and SFD to all frames sent to it (transmit path) and removes preamble and SFD on all frames received by it (receive path). A CRC check is also applied to all transmit and receive packets. Packets with a bad CRC are marked, counted in the statistics block, and may be optionally dropped.

The MAC operates in full-duplex mode only. The PHY, to which the MAC is attached, must advertise full-duplex mode during any auto-negotiation process.

3.1.2 Features

The following sections cover the MAC functions.

3.1.2.1 Padding of Undersized Frames on Transmit

The padding feature allows Ethernet frames smaller than 64 bytes to be transferred across the SPI4-2 interface and automatically padded up to 64 bytes by the MAC. This feature is enabled by setting bit 7 of the DiverseConfigWrite Register = 1 (Address Port_Index + 0x18h).

3.1.2.2 Automatic CRC Generation

The Automatic CRC Generation is used in conjunction with the padding feature to generate and append a correct CRC to any incoming frame from the SPI4-2. This feature is enabled by setting bit 6 of the DiverseConfigWrite Register = 1 (Address Port_Index + 0x18h).

Note: When padding of undersized frames on transmit is enabled, the automatic CRC generation must be enabled for proper operation of the IXF1010.

3.1.2.3 Filtering of Receive Packets

This feature allows the MAC to filter receive packets under various conditions and drop the packets via an interaction with the Receive FIFO control.

3.1.2.3.1 Filter on Unicast Packet Match

This feature is enabled when bit 0 of the PacketFilterControl Register = 1. Any frame received in this mode that does not match the StationAddress is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all unicast frames are sent to the SPI4-2 interface.

3.1.2.3.2 Filter on Multicast Packet Match

This feature is enabled when bit 1 of the PacketFilterControl Register = 1. Any frame received in this mode that does not match the PortMulticastAddress is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable register = 1. Otherwise, all multicast frames are sent to the SPI4-2 interface.

3.1.2.3.3 Filter Broadcast Packets

This feature is enabled when bit 2 of the PacketFilterControl Register = 1. Any broadcast frame received in this mode is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all broadcast frames are sent to the SPI4-2 interface.

3.1.2.3.4 Filter VLAN Packets

This feature is enabled when bit 3 of the PacketFilterControl Register = 1. VLAN frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all VLAN frames are sent to the SPI4-2.

3.1.2.3.5 Filter PAUSE Packets

This feature is enabled when bit 4 of the PacketFilterControl Register = 0. PAUSE frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all PAUSE frames are sent to the SPI4-2.

Table 4. Pause Packets Drop Enable Behavior

PauseFramePass	FrameDropEn	Actions
1	0	Packets are passed to the SPI4-2. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and sent to the switch or Network Processor, regardless of the FrameDropEn setting.
0	1	PAUSE Packets are marked as bad, are dropped in the RX FIFO, and never appear at the SPI4-2.

3.1.2.3.6 Filter CRC Errored Packets

Frames received with an errored CRC are marked as bad frames and may optionally be dropped in the RX FIFO. Otherwise, the frames are sent to the SPI4-2 and may be dropped by the switch or system controller (see Table 5 on page 21).

Table 5. CRC Errored Packets Drop Enable Behavior

CRCErroredPASS	FrameDropEn	Actions
1	0	Packets are passed to the SPI4-2. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and are sent to the switch or Network Processor regardless of the FrameDropEn setting.
0	1	CRC errored packets are marked as bad, dropped in the RX FIFO, and never appear at the SPI4-2.

3.1.2.4 PAUSE Command Frames

The MAC acts on any PAUSE Command frames received from the link partner by checking the entire frame and verifying that it is a valid PAUSE control frame addressed to either the Multicast Address (01-80-c2-00-00-01 as specified in IEEE 802.3, Annex 31B) or the Station Address. If the PAUSE frame is valid, the Transmit side of the MAC pauses for the required number of Pause Quanta, as specified in IEEE 802.3u, Clause 31 (see Table 4 on page 21).

Note: PAUSE does not begin until completion of the frame currently being transmitted.

3.1.2.5 Auto-Negotiation

Auto-negotiation is carried out by the PHY connected to the RGMII interface. The IXF1010 should communicate its supported abilities to the PHY. The PHY registers should be configured to select the appropriate advertisements and enable auto-negotiation.

The MDIO interface block contains the logic through which the registers in the connected PHYs can be accessed. For more information on the MDIO interface of the IXF1010, refer to Section 3.4, “MDIO Control and Interface” on page 37.

The following IXF1010 capabilities should be advertised during auto-negotiation in the connected PHY's Auto-Negotiation Advertisement Register.

- Speed
  - — The IXF1010 supports both 100 and 1000 Mbps operation. All required speed adjustments, clocks, etc., are supplied by the IXF1010. The operating speed of the MAC is programmable via the RGMII Speed Register.
- Duplex
  - — The IXF1010 supports full-duplex only, and this must be the only mode advertised by the connected PHY during auto-negotiation. If the IXF1010 is connected to a link partner that does not support auto-negotiation and reverts to parallel detection, the duplex setting between the IXF1010 MAC and the local and remote PHYs become out of step, leading to a link collision.
- Flow Control
  - — The connected PHY should advertise that IXF1010 supports the ability to send and receive flow control frames (symmetric).

The IXF1010 polls the PHY to determine when auto-negotiation is complete. After completion of auto-negotiation by the PHY, the IXF1010 reads the PHY's Auto-Negotiation Link Partner Base Page Ability Register. From the settings in this register, the following IXF1010 registers must be programmed to match the connected PHY configuration.

- Speed: The IXF1010 Speed should be set to either 100 or 1000 Mbps in the RGMII Speed Register (Addr Port Index + 0x10) (see Table 51 on page 78).
- Link: While link is established, the user must write Link LED Enable Register (Addr 0x502) (link to register). Note: This register controls link LED (refer to Section 3.5, "LED Interface" on page 41). The link LED does not update automatically. The Link LED Register should be updated anytime there is a change in link status in order to have the link LED Green show expected behavior.
- Flow Control: If the link partner does not support flow control, the FC Enable Register (Addr Port Index + 0x12) must be updated to reflect this change (see Table 52 on page 78).

Note: If a change is detected, the user must once again update the IXF1010 registers if any changes in the speed, duplex, or flow control capabilities of the link partner change.

3.1.3 RMON Statistics Support

3.1.3.1 RMON Statistics

The IXF1010 supplies RMON statistics via the CPU interface. These statistics are available in the form of counter values that can be accessed at specific addresses in the IXF1010 memory map. Once read, these counters automatically reset and begin counting from zero. A separate set of RMON statistics is available for each MAC device in the IXF1010.

Implementation of the RMON Statistics block is similar to the functionality provided by existing Intel switch and router products. This allows the IXF1010 to provide all of the RMON Statistics group as defined by RFC2819.

The following statistics are supported on a per-port basis:

etherStatsDropEvents (RX)	
etherStatsOctets [31:0] (RX)	etherStatsOctets [31:0] (TX)
etherStatsPkts (RX)	etherStatsPkts (TX)
etherStatsBroadcastPkts (RX)	etherStatsBroadcastPkts (TX)
etherStatsMulticastPkts (RX)	etherStatsMulticastPkts (TX)
etherStatsCRCAlignErrors (RX)	etherStatsCRCAlignErrors (TX)
etherStatsUndersizePkts (RX)	etherStatsUndersizePkts (TX
etherStatsOversizePkts (RX)	etherStatsOversizePkts (TX)
etherStatsFragments (RX)	etherStatsFragments (TX)
etherStatsJabber (RX)	etherStatsJabber (TX)
etherStatsPkts64Octets (RX)	etherStatsPkts64Octets (TX)
etherStatsPkts65to127Octets (RX)	etherStatsPkts65to127Octets (TX)
etherStatsPkts128to255Octets (RX)	etherStatsPkts128to255Octets (TX)
etherStatsPkts256to511Octets (RX)	etherStatsPkts256to511Octets (TX)
etherStatsPkts512to1023Octets (RX)	etherStatsPkts512to1023Octets (TX)
etherStatsPkts1024to1518Octets (RX)	etherStatsPkts1024to1518Octets (TX)

3.1.4 Transmit Pause Control Interface

The Transmit Pause Control interface is a completely asynchronous interface. It consists of four address signals (TxPauseAdd[3:0]) and a strobe signal (TxPauseFr). The required address for this interface operation is placed on the TxPauseAdd[3:0] pins and the TxPauseFr is pulsed High and then returned Low. The timing for the interface is shown in Table 7 on page 24. The valid decodes for the TxPauseAdd[3:0] signals are shown in Table 6. Figure 5 on page 24 displays the transmit pause control interface.

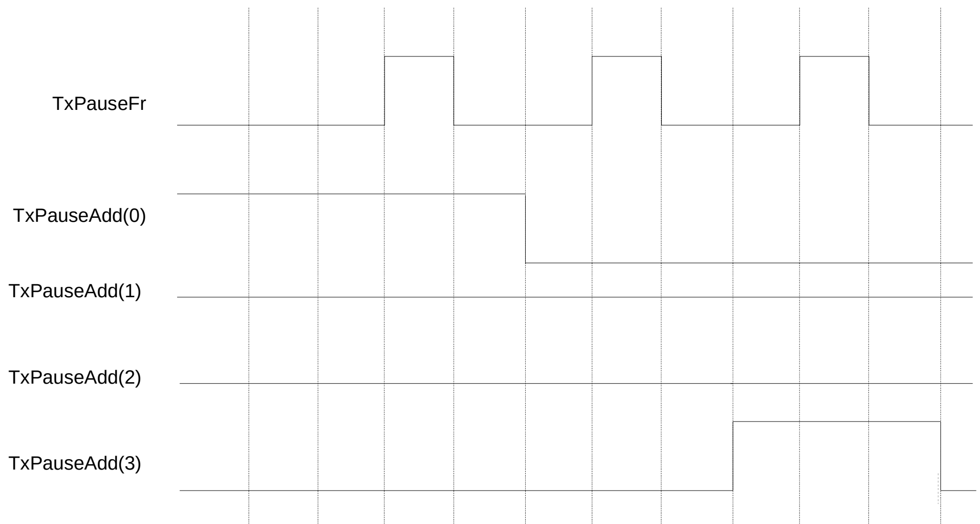
Table 6. Valid Decodes for TxPauseAdd[3:0]

TxPauseAdd[3:0]	Operation of Tx Pause Interface
00h	Sends out a PAUSE frame on every port with a pause_time = ZERO (for example, cancels all previous pause commands)
01h to 0Ah	Sends a PAUSE frame out on the selected port with pause_time = to the value programmed into that port's register set
0Bh to 0Eh	Reserved. These are invalid decodes and should not be used. The Tx Pause Interface will not operate under these conditions.
0Fh	Sends a PAUSE frame out on every port with pause_time = to the value programmed into that ports register set.

Table 7. Interface Timing

Timing Parameter	Min	Max
TxPauseFr pulse width	16 ns	–
TxPauseAdd[3:0] setup time before TxPauseFr rising edge	16 ns	–
TxPauseAdd[3:0] hold time after TxPauseFr rising edge	32 ns	–
Time between TxPauseFr pulses	48 ns	–

Figure 5. Transmit Pause Control Interface



This example shows the following conditions:

Strobe 1:
- Port 0 : Transmit Pause Packet

Strobe 2:
- All Ports : Transmit Pause Packet with pause_time = 0

Strobe 3:
- Port 7 : Transmit Pause Packet

3.2 System Packet Interface Level 4 Phase 2

The System Packet Interface Level 4 Phase 2 (SPI4-2) provides a high-speed connection to a network processor or an ASIC. The interface implemented on the IXF1010 operates at data rates up to 12.8 Gbps and supports up to ten 1 Gbps MAC channels in the IXF1010. The data path is 16 lanes wide in each direction, with each lane operating at up to 800 Mbps. Port addressing, start/end packet control, and error control codes are all transferred “In-band” on the data bus. In-band addressing supports up to 10 ports. Separate transmit and receive FIFO status lines are used for flow control. By keeping the FIFO status information out-of-band, the transmit and receive interfaces may be decoupled to operate independently.

3.2.1 Data Path

Transfer of complete packets or shorter bursts is controlled by the programmed MaxBurst1 or MaxBurst2 in conjunction with the FIFO status bus. The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted between burst transfers only. Once a transfer begins, data words are sent uninterrupted until end-of-packet, or until a multiple of 16 bytes is reached as programmed in MaxBurst1 and MaxBurst2. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words and/or training patterns.

Note: The system designer should be aware that the MAC Transfer Threshold Register must be set to a value which exceeds MaxBurst1 number of bytes. Otherwise, a TX FIFO under-run may result.

The minimum and maximum supported packet lengths are determined by the application. Because the IXF1010 is targeted at the Ethernet Environment, the minimum frame size is 64 bytes and the maximum frame size is 1522 bytes for VLAN packets (1518 bytes for non-VLAN packets). For larger frames, adjust the Max Frame Size Register value, seen in Table 50 on page 78. However, for ease of implementation, successive start-of-packets must occur not less than eight cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

Note: Data Packets with frame lengths less than 64 bytes cannot be transferred to the IXF1010 unless packet padding is enabled. If this rule is disregarded, unwanted fragments may be generated on the network at the RGMII interface.

Figure 6 on page 26 shows cycle-by-cycle behavior of the data path for valid state transitions. The states correspond to the type of words transferred on the data path. Transitions from the “Data Burst” state (to “Payload Control” or “Idle Control”) are possible only on the integer multiples of eight cycles (corresponding to multiples of 16-byte segmentations) or upon end-of-packet. A data burst must immediately follow a payload control word on the next cycle. Arcs not annotated correspond to single cycles.

In the IXF1010, the RX FIFO Status channel operates in a pessimistic mode. For example, if there is a DIP-2 check error found, all previously granted credits are cancelled and the internal status for each channel is set to SATISFIED. Any current data burst in transmission is completed. No new credits are granted until a complete FIFO status cycle has been received and validated by a correct DIP-2 check. This is the only method of operation that can eliminate the possibility of an overrun in the link partner device. It is termed as pessimistic because it has the longest latency and largest impact on usable bandwidth. However, as a DIP-2 check error is a rare event, there will be no ‘real world’ effect on bandwidth utilization and no possibility of data loss.

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Figure 6. Data Path State Diagram

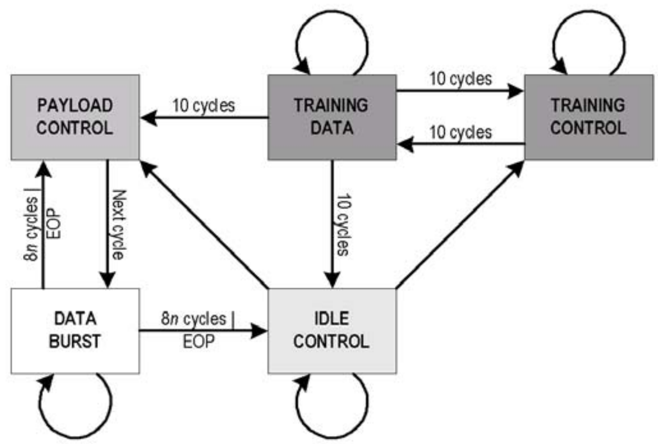
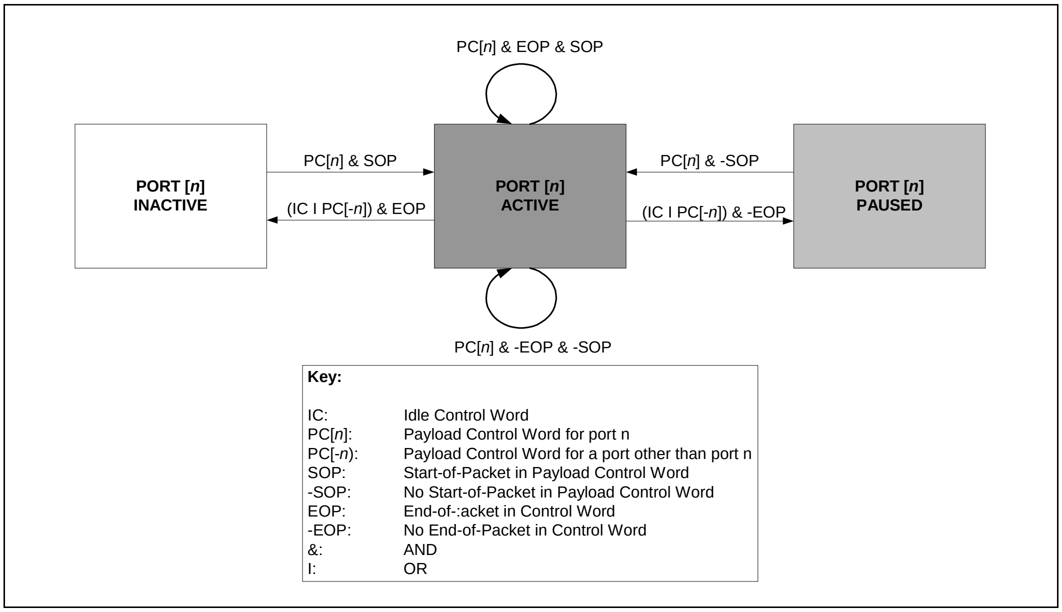


Figure 7 on page 27 shows per-port state transitions at control-word boundaries. At any given time, a port may be active (sending data), paused (not sending data but pending the completion of an outstanding packet), or inactive (not sending data, no outstanding packet).

The SPI4-2 Specification details all available Payload Control Words and should be used to reference the specific meaning of each. The IXF1010 supports all required functions per this specification. However, there are various specifics in the way certain Control Words effect the balance of the IXF1010 operation, such as how the device deals with EOP Aborts.

The SPI4-2 Specification allows the EOP Abort Payload Control word, which signals that the data associated with a particular frame is errored and should be dropped, or errored and dropped by the far-end link partner. In the IXF1010, all TX SPI4-2 transfers that end with an EOP Abort code have the TX RGMII CRC corrupted. This is true regardless of the MAC configuration.

Figure 7. Per-Port State Diagram with Transitions at Control Words



3.2.2 Start-Up Parameters

3.2.2.1 CALENDAR_LEN

CALENDAR_LEN specifies the length of each calendar sequence. As the IXF1010 is a 10-port device, CALENDAR_LEN is fixed at 10 for both TX and RX data paths.

3.2.2.2 CALENDAR_M

CALENDAR_M specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence.

In the IXF1010, the TX path CALENDAR_M is fixed at 1, therefore the port status for ports 0 - 9 will be transmitted only once between the framing and DIP2 cycle of the calendar sequence.

In the IXF1010, the RX path CALENDAR_M is configurable. The default value of expected RX CALENDAR_M is 1 as per the TX path. Table 88, "SPI4-2 RX Calendar Register (Addr: 0x702)" on page 113, bits 3 to 0 specify CAL_M, which is the number of times the calendar sequence will be repeated over the default value of 1.

The default value for CAL_M is 0, thus the default value of both Tx and RX CALENDAR_M parameters is 1.

3.2.2.3 DIP2_Thr

DIP2_Thr is a parameter specifying the number of consecutive correct DIP2s required by the RX SPI4-2 to validate a calendar sequence and therefore terminate sending training sequences. Table 88, "SPI4-2 RX Calendar Register (Addr: 0x702)" on page 113, bits 19 to 16 specify this parameter. The default value for DIP2_Thr is 1.

3.2.2.4 Loss_Of_Sync

Loss_Of_Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and therefore restart training sequences. Table 88, "SPI4-2 RX Calendar Register (Addr: 0x702)" on page 113, bits 11 to 8 specify this parameter. The default value for Loss_Of_Sync is 3.

3.2.2.5 DATA_MAX_T

DATA_MAX_T is an RX SPI4-2 parameter specifying the interval between transmission of periodic training sequences. Table 87, "SPI4-2 RX Training Register (Addr: 0x701)" on page 112, bits 15 to 0 specify this parameter. The default value for DATA_MAX_T is 0x0000, which disables periodic training sequence transmission.

3.2.2.6 REP_T

REP_T is an RX SPI4-2 parameter specifying the number of repetitions of the training sequence to be scheduled every DATA_MAX_T interval. Table 87, "SPI4-2 RX Training Register (Addr: 0x701)" on page 112, bits 23 to 16 specify this parameter. The default value for REP_T is 0x00.

3.2.2.7 DIP4_UnLock

DIP4_UnLock is a TX SPI4-2 parameter specifying the number of consecutive incorrect DIP4 fields to be detected in order to declare loss of synchronization and drive TSTAT bus with framing. Table 89, "SPI4-2 TX Synchronization Register (Addr: 0x703)" on page 113, bits 7 to 4 specify this parameter. The default value for DIP4_UnLock is 0x4.

3.2.2.8 DIP4_Lock

DIP4_Lock is a TX SPI4-2 parameter specifying the number of consecutive correct DIP4 fields to be detected in order to declare synchronization achieved and enable the calendar sequence. Table 89, "SPI4-2 TX Synchronization Register (Addr: 0x703)" on page 113, bits 3 to 0 specify this parameter. The default value for DIP4_Lock is 0x5.

3.2.2.9 MaxBurst1

MaxBurst1 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates "starving". Bits 24 to 16 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst1 is 0x006, indicating a MaxBurst1 of 96 bytes (see Section 86, "SPI4-2 RX Burst Size Register (Addr: 0x700)" on page 112).

3.2.2.10 MaxBurst2

MaxBurst2 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates "hungry". Bits 8 to 0 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst2 is 0x002, indicating a MaxBurst1 of 32 bytes (see Section 86, "SPI4-2 RX Burst Size Register (Addr: 0x700)" on page 112).

3.2.3 Training Sequence for Dynamic Phase Alignment (Data Path Deskew)

3.2.3.1 Training at Start-up

The SPI4-2 Specification states that on power-up or after a reset, the training sequence (as defined in the SPI4-2 Specification) is sent indefinitely by the source side until it receives valid FIFO status on the FIFO bus. The specification also states that it is possible for the bus deskew to be completed after one training sequence takes place. Due to some inadequacies in the specification, it is unlikely that the bus can be deskewed in a single training sequence due to the presence of both random and deterministic jitter. The only way to account for the random element is to determine an average over repeated training sequences. Since the required number of repeats is dependent on several characteristics of the system in which the IXF1010 is being used, power on training (or training following loss of synchronization) will continue until synchronization is achieved and the calendar is provisioned. The length of power on training will not be a fixed number of repeats.

The number of training sequence repeats could be a fairly large number (16, 32 or 64). If this is necessary every time training is required, a significant use of interface bandwidth is needed just to train and deskew the data path. This is only done at power-up or reset for an optimal starting point interface. After this, periodic training is used to provide a better adjustment and a substantially lower bandwidth overhead.

3.2.3.2 Periodic Training

A scheduled training sequence is sent at least once every pre-configured bounded interval (DATA_MAX_T) on both the transmit and receive paths. These training sequences are used by the receiving end of each interface for deskewing bit arrival times on the data and control lines. The sequence allows the receiving end to correct for relative skew difference of up to +/- 1 bit time. The training sequence consists of one (1) idle control word followed by one or more repetitions of a 20-word training pattern consisting of 10 (repeated) training-control words.

The initial idle control word removes dependencies of the DIP-4 in the training control words from preceding data words. Assuming a maximum of +/- bit time alignment jitter on each line, and a maximum of +/- bit time relative skew between lines, there are at least eight bit times when a receiver can detect a training control word prior to deskew. The training data word is chosen to be orthogonal to the training control word. In the absence of bit errors in the training pattern, a receiver should be able to successfully deskew the data and control lines with one training pattern. The sending side of the data path on both the transmit and receive interfaces must schedule the training sequence at least once every DATA_MAX_T cycles.

Note: DATA_MAX_T may be set to zero, disabling periodic training on the interface (refer to Table 87, “SPI4-2 RX Training Register (Addr: 0x701)” on page 112). This is done when a system shows very little drift during normal operation, and no fine-grain correction on an on-going basis is needed. This allows the maximum possible bandwidth for data transfer. The transmit and receive interface training sequences are scheduled independently.

3.2.3.3 Training in a Practical Implementation

The OIF Standard states that it should be possible to train and deskew the data input in a single training cycle. However, from the research carried out and the variances in jitter and skew due to board layout and clock tolerance issues, some sort of averaging over several repeated training patterns are required to reliably determine the optimal point at which to capture the incoming data. This is true for both static alignment and dynamic phase alignment. Therefore, several training patterns are required for an average. The more training patterns, the more accurate the average.

The deskew circuit in the IXF1010 uses dynamic phase alignment with a typical averaging requirement of 32 training patterns required to deliver a reliable result. During power-on training, an unlimited number of training cycles are sent by the data sourcing device. (The standard states that training must be sourced until a calendar has been provisioned). In the IXF1010, the deskew circuit waits until completion of its programmed average over the training patterns, ensuring that the required number of good DIP-4s is seen. Only then will a calendar be provisioned.

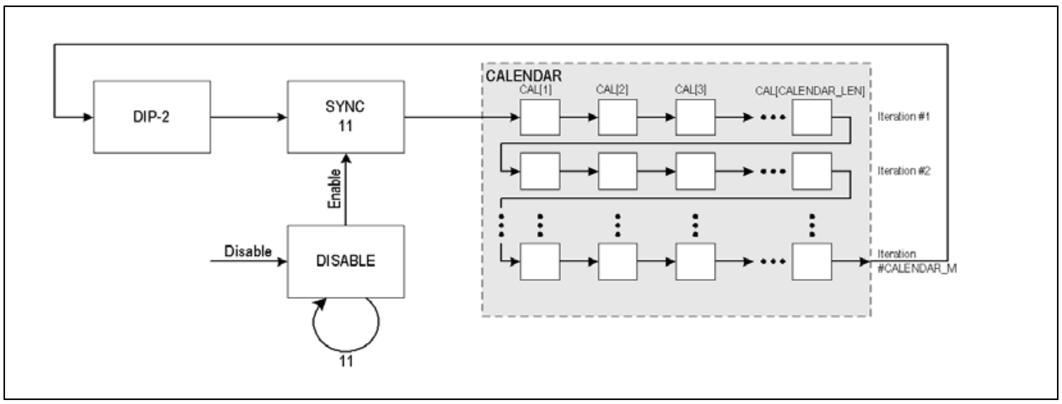
During periodic training, it is important to ensure that the training result is no less accurate than that already used for the initial decision during power-on training. Thus a similar number of training cycles must be averaged over (32). This could make the overhead associated with periodic training large if it is required to be carried out too often. We therefore recommend that periodic training be schedule infrequently (DATA_MAX_T = a large number) and that the number of repetitions of training be = 32(α).

3.2.4 FIFO Status Channel

FIFO status information is sent periodically over the TSTAT link from the IXF1010 to the upper layer processor device, and over the RSTAT link from the link processor to the IXF1010. The status channels operate independently.

Figure 8 shows the operation of the FIFO status channel. The sending side of the FIFO status channel is initially in the DISABLE state and sends the “1 1” pattern repeatedly. When FIFO status transmission is enabled, there is a transition to the SYNC state and the “1 1” framing pattern is sent. FIFO status words are then sent according to the calendar sequence, repeating the sequence CALENDAR_M times, followed by the DIP-2 code.

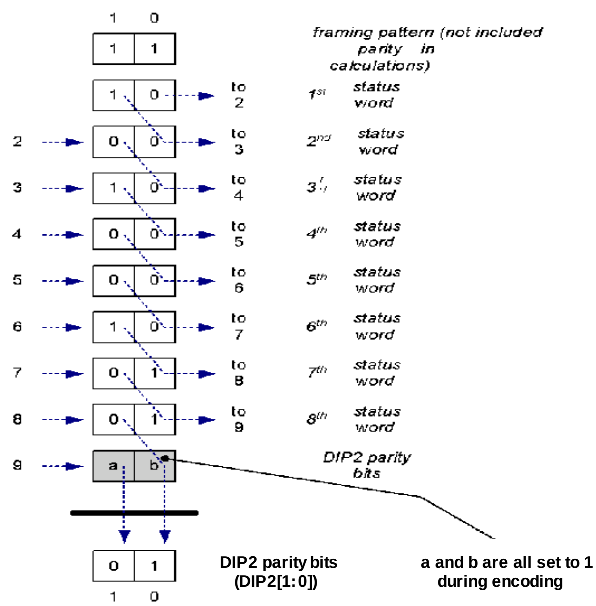
Figure 8. FIFO Status State Diagram



The FIFO status of each port is encoded in a 2-bit data structure, which is defined in Table 8, “FIFO Status Format” on page 32. The most significant bit of each port status is sent over TSTAT/RSTAT [1] and the least significant bit is sent over TSTAT/RSTAT [0]. The “1 1” pattern is reserved for In-band framing, which must be sent once prior to the start of the FIFO status sequence.

Immediately before the “1 1” framing pattern, a DIP-2 odd parity checksum is sent at the end of each complete sequence. The DIP-2 code is computed over all preceding FIFO status indications sent after the last “1 1” framing pattern and diagonally over TSTAT/RSTAT [1] and TSTAT/RSTAT [0], as shown in Figure 9 on page 31. The first word is at the top of the figure and the last word is at the bottom. The parity bits are computed by summing diagonally. Bits a and b in line 9 correspond to the space occupied by the DIP-2 parity bits and are set to 1 during encoding. The “1 1” framing pattern is not included in the parity calculation. The procedure described applies to either parity generation on the egress path or to check parity on the ingress path.

Figure 9. Example of DIP-2 Encoding



While the parity bits mimic the “1 1” pattern, the receiving end still frames successfully by syncing onto the last cycle in a repeated “1 1” pattern, and by making use of the configured sequence length when searching for the framing pattern.

To permit more efficient FIFO utilization, the MaxBurst1 and MaxBurst2 credits are granted and consumed in increments of 16-byte blocks. For any given port, these credits correspond to the most recently received FIFO status. They are not cumulative and supersede previously granted credits for the given port. A burst transfer shorter than 16 bytes (for example, an end-of-packet fragment) consumes an entire 16-byte credit.

A continuous stream of repeated “1 1” framing patterns indicates a disabled status link. For example, it may be sent to indicate that the data path deskew is not yet completed or confirmed. When a repeated “1 1” pattern is detected, all outstanding credits are cancelled and set to zero.

Table 8. FIFO Status Format

MSB	LSB	Description
1	1	Reserved for framing or to indicate a disabled status link.
1	0	SATISFIED: Indicates that the corresponding port's FIFO is almost full. When SATISFIED is received, only transfers using the remaining previously granted 16-byte blocks (if any) may be sent to the corresponding port until the next status update. No additional transfers to that port are permitted while SATISFIED is indicated.
0	1	HUNGRY: When HUNGRY is received, transfers for up to MaxBurst2 16-byte blocks, or the remainder of what was previously granted (whatever is greater), may be sent to the corresponding port until the next status update.
0	0	STARVING: Indicates that buffer underflow is imminent in the corresponding PHY port. When STARVING is received, transfers for up to MaxBurst1 16-byte blocks may be sent to the corresponding port until the next status update

The indicated FIFO status is based on the latest available information. A STARVING indication provides additional feedback information, so that transfers are scheduled accordingly. Applications which do not distinguish between HUNGRY and STARVING may only examine the most significant FIFO status bit.

Note: If a port is disabled on the IXF1010, FIFO status for the port is set to SATISFIED to avoid the possibility of any data being sent to it by the controlling device. This applies to the IXF1010 transmit path.

Upon reset, the FIFOs in the data path receiver are emptied, and any outstanding credits are cleared in the data path transmitter. After reset, and before active traffic is generated, the data transmitter sends continuous training patterns. Transmission of the training patterns continue until valid information is received on the FIFO Status Channel. The receiver ignores all incoming data until it has observed the training pattern and acquired synchronization with the data. Synchronization may be declared after a provisional number of consecutive correct DIP-4 code words are seen. Loss of synchronization may be reported after a provisional number of consecutive DIP-4 code words are detected. (For details, see Table 89, “SPI4-2 TX Synchronization Register (Addr: 0x703)” on page 113).

As stated above, the DIP-4 thresholds are programmable. However, there is a potential issue where it is possible that a given link which shows DIP-4 errors may never lose synchronization and re-train to fix the issue. This would mean an on-going and potentially significant loss of data on the link affecting all ports transferring data at that time.

This issue may be seen in two instances:

- During training (most likely periodic training)
- During data transfers where each of the data transfers (MaxBurst1 or MaxBurst2) are separated by more than one idle control word

The mechanism for both issues is the same. It is due to the fact that data will not change during a repeated period of the same control word being transmitted on the link. If there have been some consecutive DIP-4 errors, they will be incremented towards the Loss-of-Sync threshold. This is most likely to occur from a path requiring deskew. If either a stream of idles or training control words follow the burst and the DIP-4 associated with each of the words is checked, only the first one and the last one will be seen as invalid. Any other control words in the middle will be seen as having a valid DIP-4 and will reset the Loss-of-Sync threshold counter back to zero.

In order to avoid this, the IXF1010 has altered the way in which the check is done for idle control words and training control words. We now only validate the first occurrence of the DIP-4 in both training control words and Idle control words for correctness. We do still check each of the words but only use the first occurrence to clear the DIP-4 Error counter. Any DIP-4 error in any of these words is still counted towards the Loss-of-Sync threshold counter. It is now impossible to mask the DIP-4 error on our interface.

3.2.5 DC Parameters

For DC parameters on SPI4-2, please refer to Table 18, “LVTTL I/O Electrical Characteristics” on page 53 and Table 19, “LVDS I/O Electrical Characteristics” on page 53.

3.3 Reduced Gigabit Media Independent Interface (RGMII)

IXF1010 supports Reduced Gigabit Media Independent Interface (RGMII) standards as defined in the Hewlett-Packard RGMII Version 1.2a specification. The RGMII is an alternative to the IEEE 802.3u MII, the IEEE 802.3z GMII, and the Ten-Bit Interface (TBI).

3.3.1 Purpose

The RGMII reduces the number of pins required to interconnect the MAC and the PHY, from a maximum of 28 pins (TBI) to 12 pins, in a cost-effective and technology-independent manner. The data paths and all associated control signals are reduced, control signals are multiplexed together, and both edges of the clock are used. For Gigabit operation, the clocks operate at 125 MHz, and for 100 Mbps operation, the clocks operate at 25 MHz. For 100 Mbps operation, the RGMII interface data path reverts to standard MII operational mode, as defined in IEEE 802.3, Clause 22. The multiplexed control signals operate as defined in RGMII Specification 1.2a.

3.3.2 1000 Mbps Operation

3.3.2.1 Multiplexing of Data and Control

Multiplexing of data and control information is achieved by utilizing both edges of the reference clocks and sending the lower 4 bits on the rising edge and the upper 4 bits on the falling edge. Control signals are multiplexed into a single clock cycle using the same technique (see Figure 19, “RGMII 1000 Mbps Multiplexing and Timing Diagram” on page 55).

3.3.2.2 Timing Specifics

This interface requires that the clock and data are generated simultaneously by the source of the signals, thus skew between the clock and data is critical for proper operation. This approach is used to provide tighter control of skew. Table 20, “RGMII 1000 Mbps Timing Specifics” on page 55 provides these timing specifics.

3.3.3 100 Mbps Operation

3.3.3.1 Multiplexing of Data and Control

The control signals are multiplexed, as in the 1000 Mbps operation, by using both edges of the clock. The data signals, however, do not need to be multiplexed. The data signals are driven off the rising edge of the clock. The clock rate is reduced to 25 MHz for 100 Mbps operation. The MAC generates the Transmit Reference Clock (TXC) and the Receive Reference Clock (RXC) is generated by the PHY. During packet reception, the RXC is stretched on either the positive or negative pulse to accommodate transition from the free-running clock to a data-synchronous clock domain (see Figure 20, “RGMII 100 Mbps Multiplexing and Timing Diagram” on page 57.

3.3.3.2 Timing Specifics

Skew between the clock and data is critical to proper operation, so timing for this interface allows simultaneous generation of the clock and data by the source. This approach is used to provide tighter control of skew. Table 22, “RGMII 100 Mbps Timing Specifics” on page 57 provides these timing specifics.

3.3.4 TXERR and RXERR Coding

To reduce interface power, the transmit error condition (TXERR) and the receive error condition (RXERR) are encoded on the RGMII interface to minimize transitions during normal network operation (refer to Table 10 on page 35 for the encoding method). Table 9 provides signal definitions for RGMII. Figure 10 shows the transitions for frames with and without errors.

Table 9. RGMII Signal Definitions

IXF1010 Symbol	RGMII Standard Symbol	Source	Description
TXC	TXC	MAC	Depending on speed, the transmit reference clock is 125 MHz or 25 MHz +/- 100 ppm.
TD[3:0]_*n*	TD<3:0>	MAC	Contains Register bits 3:0 on the rising edge of TXC and Register bits 7:4 on the falling edge of TXC
TX_CTL	TX_CTL	MAC	TXEN on the rising edge of TXC TXEN xor TXERR on the falling edge of TXC
RXC	RXC	PHY	Continuous reference clock is 125 MHz or 25 MHz +/- 100 ppm
RD[3:0]_*n*	RD<3:0>	PHY	Contains Register bits 3:0 on the rising edge of RXC and Register bits 7:4 on the falling edge of RXC
RX_CTL	RX_CTL	PHY	RX_CTL is on the rising edge of RXC RX_CTL xor RXERR is the falling edge of RXC

Note: The value of RGMII_TXER and RGMII_TXEN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

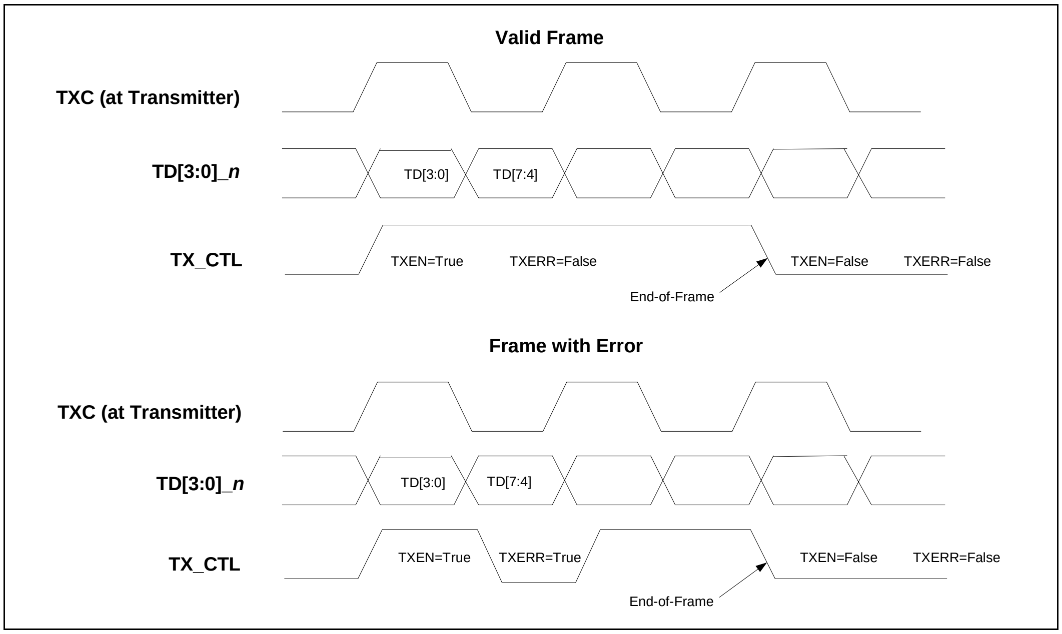
TXERR <= RGMII_TXER (XOR) RGMII_TXEN

RXERR <= RGMII_RXER (XOR) RGMII_RXDV

Table 10. TXERR and RXERR Coding Example

Condition	Description	
Receiving valid frame, no errors	RX_CTL = true Logic High on rising edge of RXC	RXERR = false Logic High on the falling edge of RXC
Receiving valid frame, with errors	RX_CTL = true Logic High on rising edge of RXC	RXERR = true Logic Low on the falling edge of RXC
Receiving invalid frame (or no frame)	RX_CTL = false Logic Low on rising edge of RXC	RXERR = false Logic Low on the falling edge of RXC
NOTE: Refer to Figure 10 for TX_CTL Behavior.		

Figure 10. TX_CTL Behavior Diagram



3.3.4.1 In-Band Status

Carrier Sense (CRS) is generated by the PHY when a packet is received from the network interface. CRS is indicated when:

- RX_CTL is true
- RX_CTL is false, RXERR is true, and a value of 0xFF exists on the RD[7:0] bits simultaneously
- RX_CTL is false, RXERR is true, and a value of 0x0F exists on RD[7:0] bits simultaneously
- RX_CTL is false, RXERR is true, and a value of 0x1F exists on RD[7:0] bits simultaneously
- RX_CTL is false, RXERR is true, and a value of 0x0E exists on RD[7:0] bits simultaneously

3.3.5 Electrical Characteristics

The RGMII signals (including MDIO/MDC) are based on 2.5V CMOS interface voltages, as defined by JEDEC EIA/JESD8-5 (see Table 21).

3.4 MDIO Control and Interface

3.4.1 MDIO Interface

IXF1010 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows the IXF1010 to monitor and control each of the PHY devices that are connected to the device's 10 ports.

3.4.2 General Description

The MDIO Master Interface block is implemented once in the IXF1010. The MDIO Interface block contains the logic through which the user accesses the registers in PHY devices connected to the MDIO/MDC interface, controlled by each port.

The MDIO Master Interface block supports the management frame format, specified by IEEE 802.3, Clause 22, Section 2.4.5. This block also supports single MDI access via the CPU interface and an autoscan mode. Autoscan allows the MDIO master to read all 32 registers of the per-port PHYs and store the contents in the IXF1010. This ability provides an external CPU-ready access to the PHY register contents via a single CPU Read without the latency of waiting on the low-speed serial MDIO data bus for each register access.

3.4.3 MDIO Register Descriptions

Table 38, "MDIO Block Register Map" on page 75 provides an overview of the MDIO Register set and Table 82, "MDI Single Command Register (Addr: 0x680)" on page 110 through Table 85, "MDI Control Register (Addr: 0x683)" on page 111 provide a register-by-register bit definition of the MDIO Register set.

3.4.4 Clear When Done

The MDI Command Register bit, in the MDI Single Command and Address Register, clears upon command completion and is set by the user to start the requested single MDIO Read or Write operation. This bit is cleared automatically upon operation completion.

3.4.5 MDC Generation

The MDC clock is used for the MDIO/MDC interface. The frequency of the MDC clock is selectable by setting the MDC speed bit in the MDI Control Register (see Table 85, "MDI Control Register (Addr: 0x683)" on page 111).

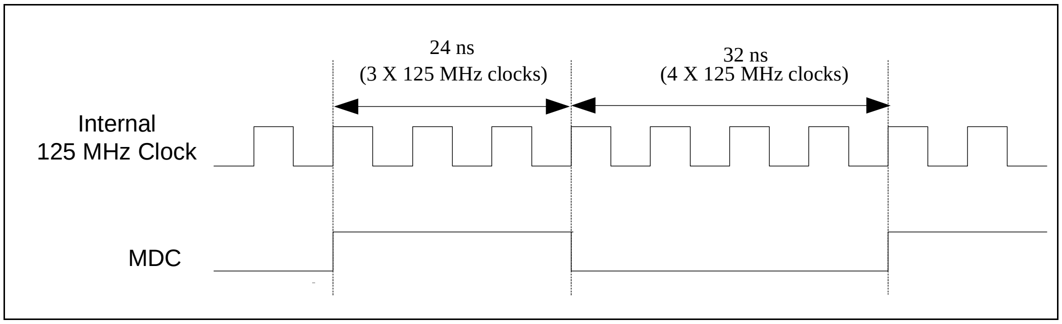
3.4.5.1 MDC High-Frequency Operation

The high-frequency MDC is 18 MHz, derived from the 125 MHz system clock by dividing the frequency by 7.

The clock duty cycle is as follows:

- MDC High duration: 3 x (1/125 MHz) = 3 X 8 ns = 24 ns
- MDC Low duration: 4 x (1/125 MHz) = 4 X 8 ns = 32 ns
- MDC runs continuously after reset

Figure 11. High-Frequency MDC Timing Diagram



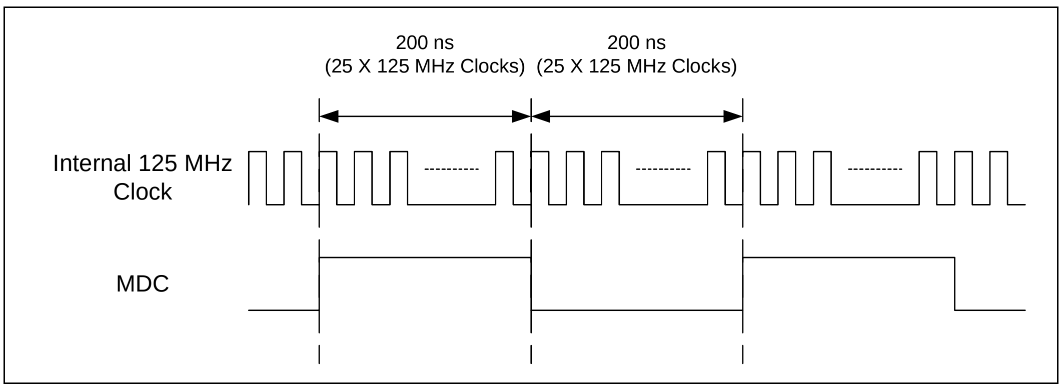
3.4.5.2 MDC Low-Frequency Operation

The low-frequency MDC is 2.5 MHz, which is derived from the 125 MHz system clock by dividing the frequency by 50.

The duty cycle is as follows:

- MDC High duration: 25 x (1/125 MHz) = 25 x 8 ns = 200 ns
- MDC Low duration: 25 x (1/125 MHz) = 25 x 8 ns = 200 ns
- MDC runs continuously after reset

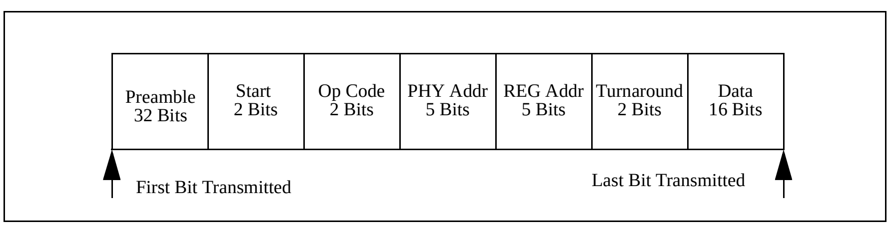
Figure 12. Low-Frequency MDC Timing Diagram



3.4.6 MDIO Management Frames

The MDIO Management interface serializes the external register access information into the format specified by IEEE 802.3, Clause 22, Section 2.4.5.

Figure 13. MDIO Management Frame Structure



3.4.7 Single MDI Command Operation

The Management Data interface is accessed through the MDI Single Command and Address Register and the MDI Single Read and Write Data Register. A single management frame is sent by setting bit 20 to Logic 1 in the MDI Single Command and Address Register, and is automatically cleared when the frame is completed.

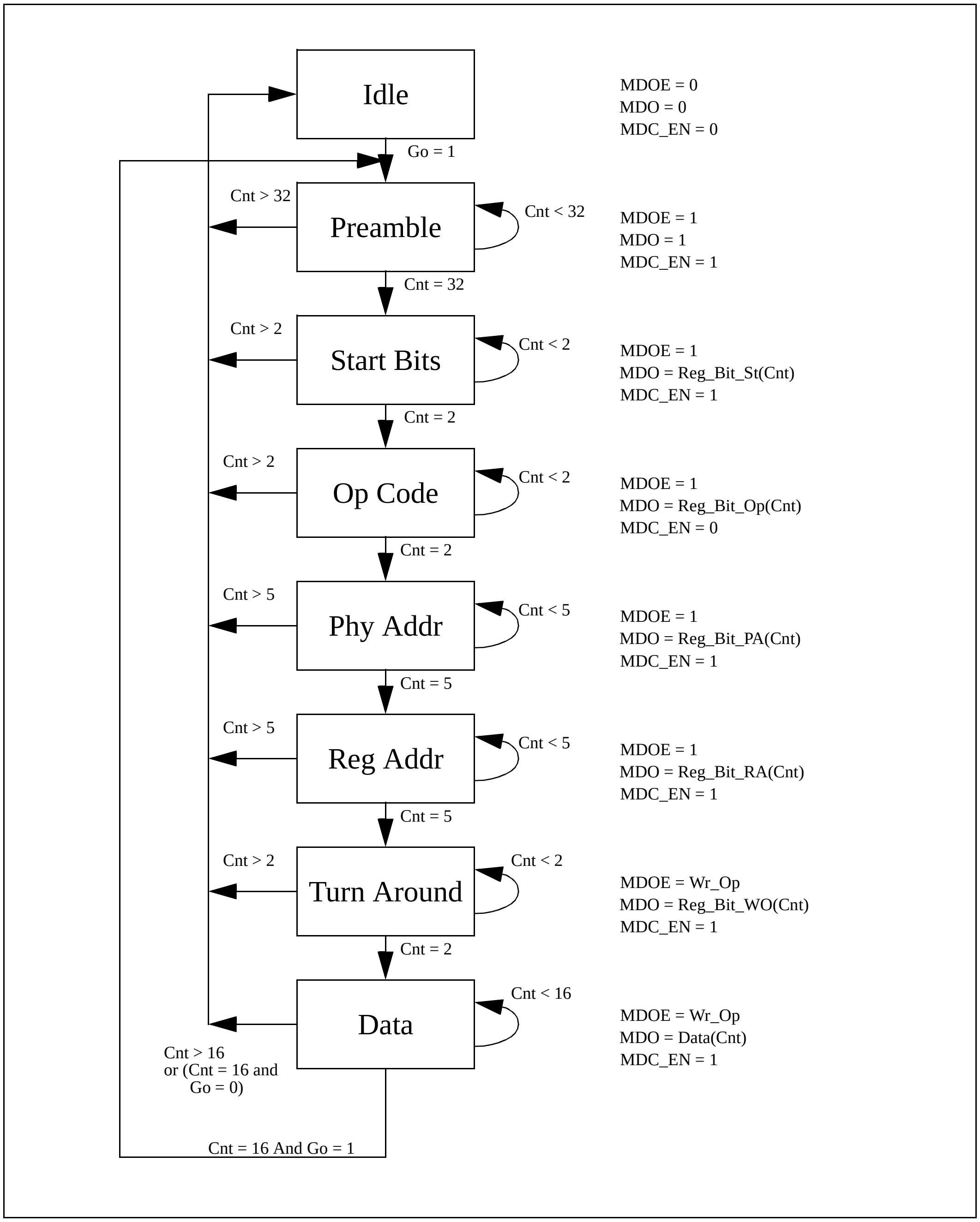
Write data is first set up in MDI Single Read and Write Data Register bits 15:0 for Write operation. The MDI Single Command and Address Register is initialized with the appropriate control information (start, op code, etc.) and MDI Single Command and Address Register bit 20 is set to Logic 1. Bit 20 is reset to Logic 0 when the frame is complete.

Read operation steps are identical except in MDI Single Read and Write Data Register bits 15:0, where the data is ignored. Data received from the MDIO is read by the CPU interface from bits 31:16.

3.4.8 MDI State Machine

The MDI State Machine sequences the information sent to it by the MDIO control registers and keeps track of the current sequence bit count, enabling or disabling the MDIO driver output (see Figure 14, “MDI State Diagram” on page 40).

Figure 14. MDI State Diagram



3.4.9 Autoscan Operation

The Autoscan PHY Address Enable Register (Table 84, "Autoscan PHY Address Enable Register (Addr: 0x682)" on page 110) is used to determine which PHY addresses are used for each of the ten IXF1010 ports. The Autoscan PHY Address Enable Register is 32 bits wide, which allows for PHY addresses 0 - 31 to be used. The bits set in this register correspond to consecutive MAC ports. The Least Significant Bit (LSB) set in the Address Enable Register is port 0 for the IXF1010; the next significant bit set is assumed to be port 1, and this continues on to port 9. If more than 10 bits are set, the bits beyond the tenth bit are ignored. If less than 10 bits are set, the round-robin process reads only the PHY registers for the reduced MAC port count.

The autoscan function stores the 32 registers in each external PHY (up to 10) internally in the IXF1010. Autoscan is enabled by setting bit 1 of the MDI Control Register (Table 85, "MDI Control Register (Addr: 0x683)" on page 111). When enabled, autoscan runs continuously, reading each PHY register. When a PHY register access is instigated through the MDIO interface, the current autoscan register Read is completed before the MDIO register access starts. Upon completion of the MDIO access, the autoscan functionality restarts from the last autoscan register access prior to the MDIO register access.

For example, the IXF1010 is connected to PHYs addressed 20-29, with the IXF1010 port 0 connected to PHY address 20, and Port 1 connected to PHY address 21. This is continued to port 9, which is connected to PHY address 29. To enable autoscan for all 10 ports on the IXF1010, bits 29:20 in the Autoscan PHY Address Enable Register must be set to 1 and all other bits set to a 0. This enables the autoscan to read PHY addresses 20-29, which allows all 32 registers of each PHY to be stored in the connected IXF1010 ports (refer to Table 34, "PHY Autoscan Register Map" on page 70).

3.5 LED Interface

3.5.1 Introduction

The IXF1010 uses a serial interface consisting of three signals to provide LED data to some form of external driver. This interface provides the data for 30 separate direct drive LEDs and allows three LEDs per MAC port.

There are two modes of operation, each with its own separate LED decode mapping. Modes of operation and LEDs are detailed in "Modes of Operation".

3.5.2 Modes of Operation

Mode selection is accomplished by using the LED_SEL_MODE bit. This bit is globally selected and controls the operation of all ports (see Table 68, "LED Control Register (Addr: 0x509)" on page 92).

There are two modes of operation:

Mode 0: (LED_SEL_MODE = 0 [Default]): This mode selects operations compatible with the SGS Thompson M5450 Led Display Driver Device. This device converts the serial data stream, output by the IXF1010, into 30 direct-drive LED outputs.

Mode 1: (LED_SEL_MODE = 1): This mode is used with standard TTL (74LS595) or HCMOS (74HC595) octal shift registers with latches, providing the most general and cost-effective implementation of the serial data stream conversion.

In addition to these physical modes of operation, there are two types of specific LED data decodes available. This option is a global selection and controls the operation of all ports (see Table 68, “LED Control Register (Addr: 0x509)” on page 92).

3.5.3 LED Interface Signal Description

The IXF1010 LED Interface consists of three output signal pins that are 2.5V CMOS level pads. Table 11 provides LED signal names, pin numbers, and descriptions.

Table 11. LED Pin Descriptions

Pin Name	Pin #	Pin Description
LED_CLK	A20	LED_CLK: This signal is an output that provides a continuous clock synchronous to the serial data stream output on the LED_DATA pin. This clock has a maximum speed of 0.5 MHz The behavior of this signal remains constant in all modes of operation.
LED_DATA	A19	LED_DATA: This signal provides the data, in various formats, as a serial bit stream. The data must be valid on the rising edge of the LED_CLK signal. In Mode 0, the data presented on this pin is TRUE (Logic 1 = High). In Mode 1, the data presented on this pin is INVERTED (Logic 1 = Low).
LED_LATCH	K18	LED_LATCH: This is an output pin and the signal is used only in Mode 1 as the Latch enable for the shift register chain. This signal is not used in Mode 0, and should be left unconnected.

3.5.4 Mode 0: Detailed Operation

Note: Please refer to the SGS Thompson M5450 datasheet for device-operation information.

The operation of the LED Interface in Mode 0 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 15 on page 42 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 15 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the M5450 device.The actual data shown in Figure 15 consists of a chain of 36 bits only, 30 of which are valid LED DATA. The 36-bit data chain is built up as follows:

Figure 15. Mode 0 Timing Diagram

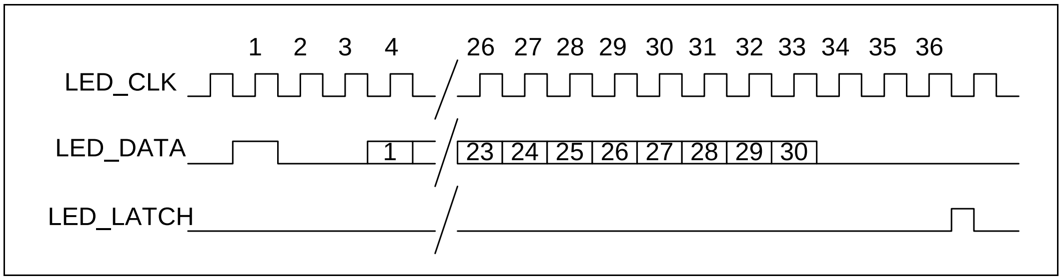


Table 12. Mode 0 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit is used to synchronize the M5450 device to expect 35 bits of data to follow.
2:3	PAD BITS	These bits are used only as fillers in the data stream to extend the length from the actual 30 bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.
4:33	LED DATA 1-30	These bits are the actual data transmitted to the M5450 device. The decode for each individual bit in each mode is defined in Table 14 on page 45. The data is TRUE. Logic 1(LED ON) = High
34:36	PAD BITS	These bits are used as fillers in the data stream to extend the length from the actual 30-bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.

When implemented on a board with the M5450 device, the LED DATA bit 1 appears on output bit 3 of the M5450 and the LED DATA bit 2 appears on output bit 4, etc. This means that output bits 1, 2, 3, 34, and 35 will never have valid data and should not be used.

3.5.5 Mode 1: Detailed Operation

Note: Please refer to manufacturers' 74LS/HC595 datasheet for information on device operation.

The operation of the LED Interface in Mode 1 is again based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 16 on page 44 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 16 shows the 36 clocks which are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for the almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the Shift Register chain devices.

The LED_LATCH signal is required in Mode 1, and is used to latch the data shifted into the shift register chain into the output latches of the 74HC595 device. As seen in Figure 16, the LED_LATCH signal is active High during the Low period on the 36th LED_CLK cycle. This avoids any possibility of trying to latch data as it is shifting through the register.

When this operation mode is implemented on a board with a shift register chain containing three 74HC595 devices, the LED DATA bit 1 is output on Shift Register bit 1, and so on up the chain. Only Shift Register bits 31 and 32 do not contain valid data. The actual data shown in Figure 16 consists of a 36-bit chain, of which 30 bits are valid LED DATA. The 36-bit data chain is built up as follows:

Note: The LED_DATA signal is now inverted from the state in Mode 0.

Figure 16. Mode 1 Timing Diagram

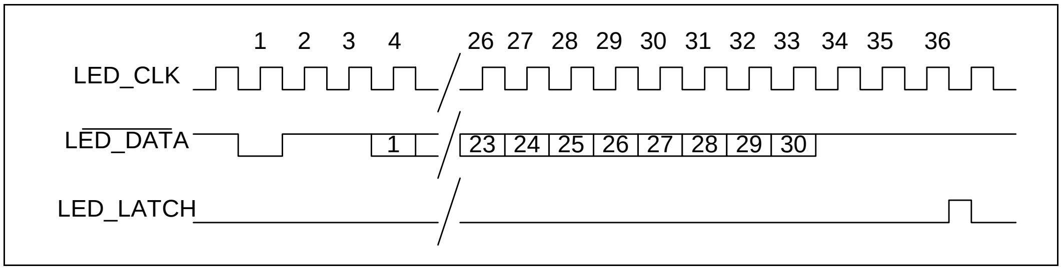


Table 13. Mode 1 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit has no meaning in Mode 1 operation and is shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
2:3	PAD BITS	These bits have no meaning in Mode 1 operation and are shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
4:33	LED DATA 1-30	These bits are the actual data to be transmitted to the 32-stage shift register chain. The decode for each bit in each mode is defined in Table 14 on page 45. The data is INVERTED. Logic 1 (LED ON) = Low.
34:36	PAD BITS	These bits have no meaning in Mode 1 operation and are latched into positions 31 and 32 in the shift register chain. These bits are not considered as valid data and should be ignored. They should always be a Logic 0 = High.

3.5.6 Power-On, Reset, and Initialization

The LED interface is disabled at power-on or reset. The system software controller must enable the LED interface. The internal state machines and output pins are held in reset until the full IXF1010 device configuration is completed. This is done by setting the LED_ENABLE bit to a logic 1 (see Table 68, "LED Control Register (Addr: 0x509)" on page 92). The power-on default for this bit is Logic 0.

3.5.7 LED Data Decodes

Table 14 shows the data decode of the data for the IXF1010.

Table 14. LED DATA Decodes

LED_DATA#	MACPORT#	IXF1010 Designation
1	0	Link LED - Amber
2		Link LED - Green
3		Activity LED - Green
4	1	Link LED - Amber
5		Link LED - Green
6		Activity LED - Green
7	2	Link LED - Amber
8		Link LED - Green
9		Activity LED - Green
10	3	Link LED - Amber
11		Link LED - Green
12		Activity LED - Green
13	4	Link LED - Amber
14		Link LED - Green
15		Activity LED - Green
16	5	Link LED - Amber
17		Link LED - Green
18		Activity LED - Green
19	6	Link LED - Amber
20		Link LED - Green
21		Activity LED - Green
22	7	Link LED - Amber
23		Link LED - Green
24		Activity LED - Green
25	8	Link LED - Amber
26		Link LED - Green
27		Activity LED - Green
28	9	Link LED - Amber
29		Link LED - Green
30		Activity LED - Green

3.5.7.1 LED Signaling Behavior

Operation in each mode for the decoded LED data in Table 14 is detailed in Table 15.

3.5.7.1.1 IXF1010 LED Behavior

Table 15. IXF1010 LED Behavior

Type	Status	Description
Link LED - Amber	Off	Port does not have an RGMII RXERR or remote fault
	On	Port does have an RGMII RXERR condition detected
	Blinking	Port remote fault
Link LED - Green	Off	Port does not have link
	On	Port is enabled and has link
Activity LED - Green	Off	Port is not transmitting and receiving
	Blinking	Port is transmitting and receiving

3.6 CPU Interface

3.6.1 General Description

The CPU Interface block provides access to registers and statistics in the IXF1010. The interface is asynchronous externally and operates within the 125 MHz clock domain internally. The interface provides access to the following registers:

- MAC Control
- MAC RX Statistics
- MAC TX Statistics
- PHY Auto Scan
- Global Status and Configuration
- RX Block
- TX Block
- MDIO Block
- SPI4-2 Block

3.6.2 Functional Description

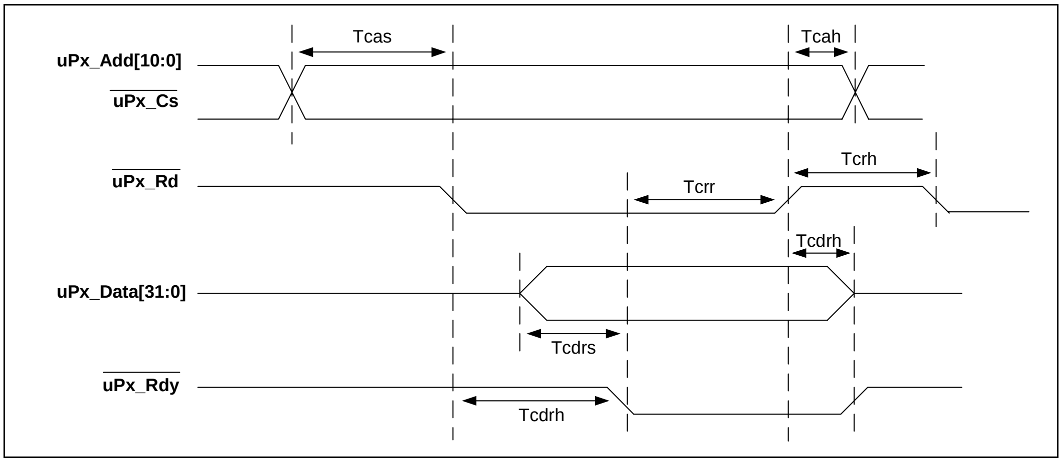
3.6.2.1 Read Access

Read access involves the following:

- Detect assertion of asynchronous Read control signal and latch address
- Generate internal Read strobe
- Drive valid data onto processor bus
- Assert asynchronous-ready signal for required length of time

Figure 17 provides the timing of the asynchronous interface for Read access.

Figure 17. Read Timing Diagram - Asynchronous Interface



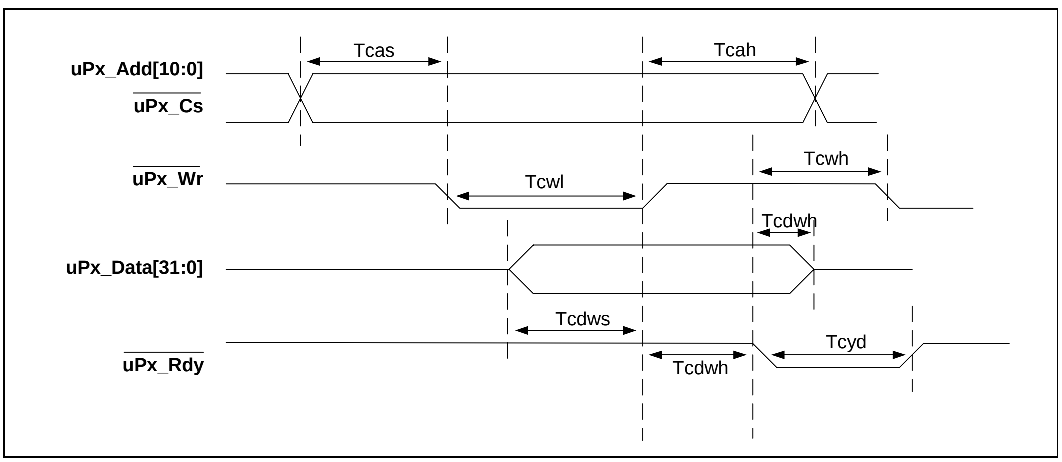
3.6.2.2 Write Access

The Write process involves the following:

- Detect assertion of Asynchronous Write control signal and latch address
- Detect de-assertion of Asynchronous Write control signal and latch data
- Generate internal Write strobe
- Assert Asynchronous Ready signal for required length of time

Figure 18 shows the timing of the asynchronous interface for Write access.

Figure 18. Write Timing Diagram - Asynchronous Interface



3.6.3 Endian

The Endian of the CPU interface may be changed to allow connection of various CPUs to the IXF1010. The Endian selection is determined by setting the Endian bit in the CPU Interface Register (see Table 67 on page 92).

3.7 Clocks

The IXF1010 device has system interface reference clocks, SPI4-2 data path input and output clocks, RGMII input and output clocks, MDIO output clock, JTAG input clock, and LED output clock. All of these clock sources have unique requirements. This section will detail these requirements.

3.7.1 System Interface Reference Clocks

There are two system interface clocks required by the IXF1010 devices.

The system interface clock, which supplies the clock to the majority of the internal circuitry, is the 125 MHz clock. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- +/- 50ppm
- Maximum duty cycle distortion 40/60

The other system interface clock supplies the clock source for the SPI4-2 receive circuitry. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- 1/8 frequency of the SPI4-2 data path frequency
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS.

3.7.2 SPI4-2 Receive and Transmit Data Path Clocks

The SPI4-2 data path clocks are compliant with the OIF 2000.88.4 Specification.

The IXF1010 has the following requirements on the transmit data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable (frequency and level) when reset is removed or when sourced, whichever happens last

The IXF1010 meets the following specifications on the receive data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS

- Stable when sourced

3.7.3 RGMII Clocks

The RGMII interface is governed by the HP 1.2a specification. The IXF1010 is fully specification compliant as follows:

- 2.5 V CMOS drive
- Maximum duty cycle distortion 40/60
- +/- 100 ppm
- 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps

3.7.4 MDC Clock

The IXF1010 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. The IXF1010 supports two speed options (18 MHz and 2.5 MHz) selectable by the MDC Speed bit in the MDI Control Register. The clock drive meets the 2.5 V CMOS specification.

3.7.5 JTAG Clock

The IXF1010 supports JTAG. The clock source must meet the 2.5 V CMOS specification. The maximum clock input frequency of 11 MHz with a maximum duty cycle distortion of 40/60.

3.7.6 LED Clock

The IXF1010 supports a serial LED data stream. This interface implements a 2.5 V CMOS output clock with a maximum frequency of 500 kHz.

4.0 Applications

4.1 TX and RX FIFO Operation

4.1.1 TX FIFO

The IXF1010's TX FIFOs are implemented with 4.5 KB for each channel. This provides enough space for at least one maximum size packet per port storage and ensures that no under-run conditions occur, assuming that the sending device can supply data at the required data rate.

The MAC threshold parameter, which is user programmable, determines when data is transmitted out of the MAC. This parameter is configurable for specific block sizes and the user must ensure that an under-run does not occur. The threshold must be set to a value that exceeds the programmed MaxBurst1 parameter. This method of operation eliminates the possibility of under-run, except when the controlling switch device fails.

4.1.2 RX FIFO

The IXF1010 RX FIFOs are provisioned so that each port has its own 17.0 KB memory space. This is enough memory to ensure that there is never an over-run on any channel while transferring normal Ethernet frame size data.

The FIFOs automatically generate Pause control frames to halt the link partner when the High watermark is reached and to restart the link partner when the data stored in the FIFO falls below the Low-watermark.

4.2 Reset and Initialization

When powering up the IXF1010, the hardware reset signal, $\overline{\text{Sys\_Res}}$, should be held active low for a minimum of 100 ns after all of the power rails have fully stabilized to their nominal values and the input clocks have reached their nominal frequency (TDCLK = 400 MHz, CLK125 = 125 MHz, and CLK50 = 50 MHz).

Note: In systems where the $\overline{\text{Sys\_Res}}$ pin is driven from a single board-wide reset signal, the switch or network processor will only come out of reset at the same time as the IXF1010, or possibly later. This means that the TDCLK will not be stable when the $\overline{\text{Sys\_Res}}$ pin is released. In the IXF1010, a built-in feature reactivates the internal reset once TDCLK is applied. It is essential in this case to ensure that the switch or network processor does not output TDCLK until it is stable and has reached its nominal operating frequency.

The IXF1010 extends this hardware reset internally to ensure synchronization of all internal blocks within the system. The internal reset is extended for a minimum of 220 µs after all clocks are stable. Before attempting to access the internal register set via the CPU interface allow for a minimum of 500 µs from all clocks being stable.

At this point, the device is correctly initialized and ready to be used. Clocks start to appear at the relevant device ports and the SPI4-2 interface begins to source a training pattern on the receive side while waiting for a training pattern on the transmit side. The SPI4-2 interface syncs up with the connected switch or network processor per the SPI4-2 Specification.

The CPU accesses can begin to configure the device for any existing user preferences desired. By default all ports on the IXF1010 are enabled after power-up. The device is ready for use at this time if the default settings are to be used. Otherwise access the required registers via the CPU interface and configure the control registers to the required settings.

5.0 Test Specifications

Table 16 through Table 30 on page 65 and Figure 19 on page 55 through Figure 30 on page 65 represent the target specifications of the IXF1010. These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 18 through Table 30 on page 65 apply over the recommended operating conditions specified in Table 17.

Table 16. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage		VDD	-0.3	2.4	Volts
		AVDD	-0.3	2.4	Volts
		VDD2	-0.3	3.0	Volts
Operating Temperature	Ambient	TOPA	-15	+85	°C
	Case	TOPC	–	+130	°C
Storage Temperature		TST	-65	-150	°C

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Operating Conditions

Parameter		Symbol	Min	Typ[1]	Max	Units
Recommended Supply Voltage		VDD	1.71	1.80	1.89	Volts
		AVDD	1.71	1.80	1.89	Volts
		VDD2	2.375	2.50	2.625	Volts
Operating Current	1000BASE-T	VDD, AVDD	–	2.062	–	Amps
		VDD2	–	0.432	–	Amps
Recommended Operating Temperature	Ambient	TOPA	0	–	70	°C
	Case with Heat Sink	TOPC-HS	0	–	119	°C
	Case without Heat Sink	TOPC-NHS	0	–	118	°C
Power Consumption	1000BASE-T full-duplex TX and RX at 25 °C	PC	–	4.8	–	Watts

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 18 provides the DC specifications for the LVTTL I/Os, which are used in the following interfaces:

- SPI4-2 FIFO Status Path
- RGMII
- MDIO
- CPU
- LED
- Pause Control
- Clocks
- Reset
- JTAG

Table 18. LVTTL I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	VIL	–	–	0.70	V	VCC=MIN
Input High Voltage	VIH	1.7	–	–	V	VCC=MIN
Output Low Voltage RGMII	VOLRG	–	–	0.40	V	VCC=MIN, IOL=6.9mA
Output Low Voltage All others	VOL	–	–	0.40	V	VCC=Min, IOL=3.9mA
Output High Voltage RGMII	VOHRG	2.0	–	–	V	VCC=MIN, IOH=-5.2mA
Output High Voltage All Others	VOH	2.0	–	–	V	VCC=MIN, IOH=-2.9mA
Output Leakage Current	IOZ	–	–	10	µA	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Table 19 provides the DC specifications for the LVDS I/Os, which are used for the SPI4-2 data path.

Table 19. LVDS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Voltage Range	VI	-0.20	–	VddMax+ 0.20	V	–
Differential Input Voltage	|VID|	100	–	–	mV	@400 MHz
Input Common-Mode Current	ICM	–	–	–	µA	LVDS Input VOS = 1.2 V
Threshold Hysteresis	TH	25	–	–	mV	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Table 19. LVDS I/O Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Differential Input Impedance	RIN	85	–	115	Ω	Typical 100 Ω
Output Low Voltage	VOL	0.95	–	–	V	–
Output High Voltage	VOH		–	1.51	V	–
Differential Output Voltage	|VOD|	330	–	446	mV	–
Delta Differential Output Voltage (Complementary States)	–	–	–	25	mV	–
Offset (Common-Mode) Voltage	VOS	1.12	–	1.3	V	–
Output Leakage Current	IOZ	–	–	10	µA	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 19. RGMII 1000 Mbps Multiplexing and Timing Diagram

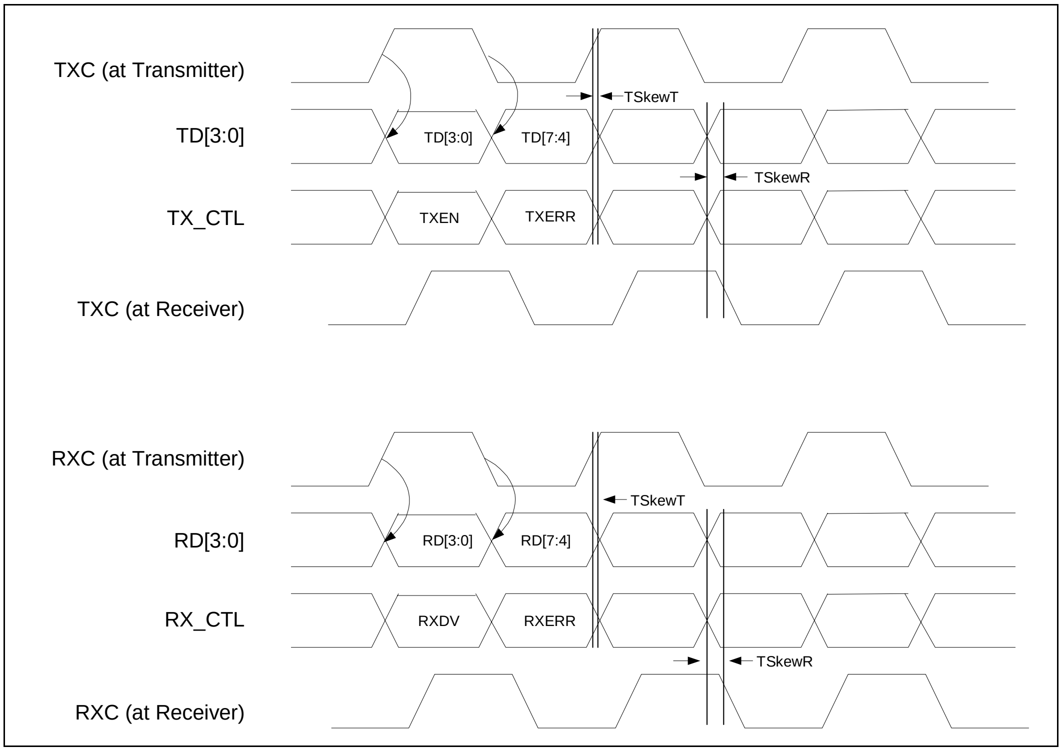


Table 20. RGMII 1000 Mbps Timing Specifics

Parameter	Symbol	Min	Typ[4]	Max	Unit	Test Conditions
Data-to-Clock Output Skew (at Transmitter)	TskewT	-500	0	500	ps	–
Data-to-Clock Input Skew (at Receiver)[1]	TskewR	1		2.8	ns	–
Clock Cycle Duration[2]	Tcyc	7.2	8	8.8	ns	–
Duty Cycle for Gigabit[3]	Duty_T	45	50	55	%	–
Duty Cycle for 100T[3]	Duty_G	40	50	60	%	–
Rise/Fall Time (20-80%)	Tr/Tf	–	–	.75	ns	–

1. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
2. For 100 Mbps, Tcyc scales to 40 ns +/- 4 ns.
3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain, as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
4. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Table 21. RGMII I/O Electrical Characteristics

Parameter	Symbol	Min	Max	Units	Test Conditions
Output High Voltage	V_{OH}	2.0	VDD +.3	V	I_{OH} = -1.0 mA; V_{CC} = MIN
Output Low Voltage	V_{OL}	GND -.3	0.40	V	I_{OL} = 1.0 mA; V_{CC} = MIN
Input High Voltage	V_{IH}	–	–	V	V_{IH} > V_{IH_MIN}; V_{CC} = MIN
Input Low Voltage	V_{IL}	–	.70	V	V_{IH} > V_{IL_MAX}; V_{CC} = MIN
Input High Current	I_{IH}	–	15	µA	V_{CC} = MAX; V_{IN} = 2.5V
Input Low Current	I_{IL}	-15	–	µA	V_{CC} = MAX; V_{IN} = 0.4V

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20. RGMII 100 Mbps Multiplexing and Timing Diagram

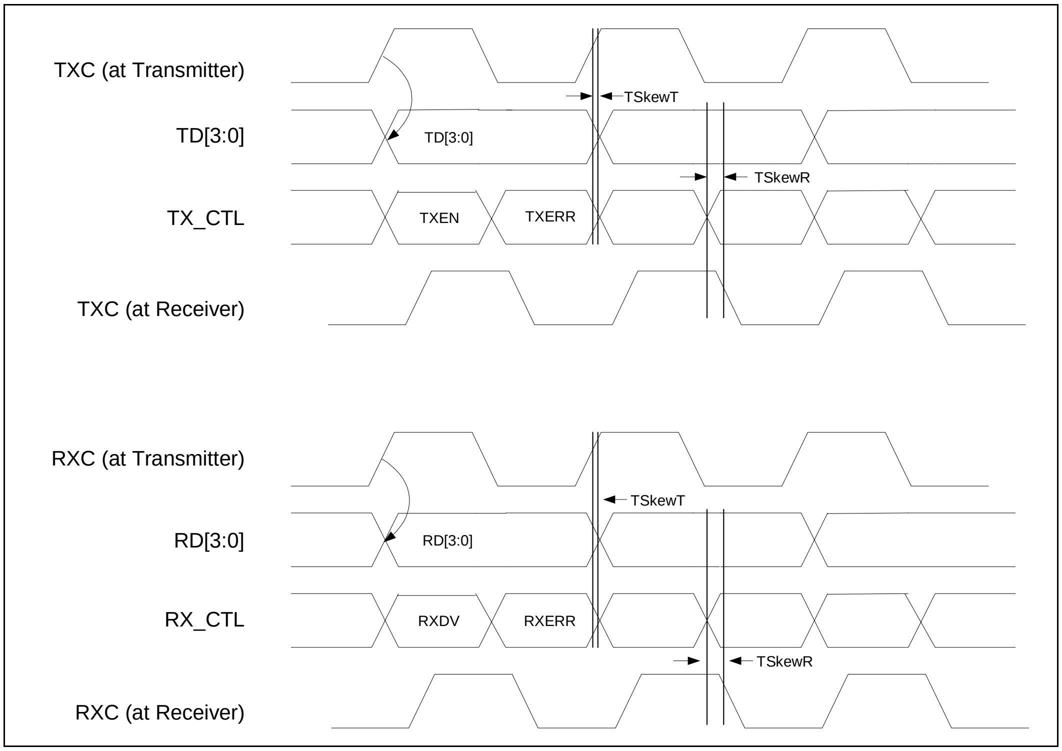


Table 22. RGMII 100 Mbps Timing Specifics

Parameter	Symbol	Min	Typ[4]	Max	Unit	Test Conditions
Data-to-Clock Output Skew (at Transmitter)	TskewT	-500	0	500	ps	–
Data-to-Clock Input Skew (at Receiver)[1]	TskewR	1	–	2.8	ns	–
Clock Cycle Duration[2]	Tcyc	36	40	44	ns	–
Duty Cycle for Gigabit[3]	Duty_T	45	50	55	%	–
Duty Cycle for 100T[3]	Duty_G	40	50	60	%	–
Rise/Fall Time (20-80%)	Tr/Tf	–	–	.75	ns	–

1. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
2. For 100 Mbps, Tcyc scales to 40 ns +/- 4 ns.
3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain, as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
4. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 21. MDIO Write Timing Diagram

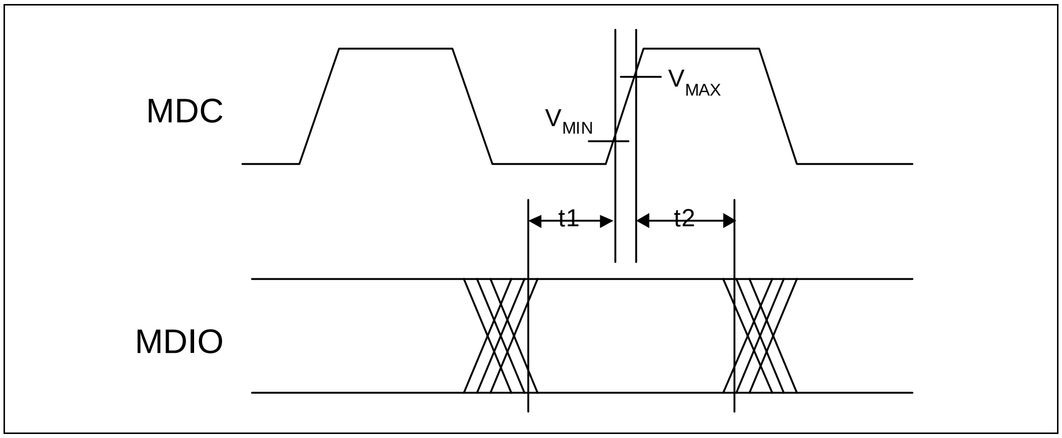


Figure 22. MDIO Read Timing Diagram

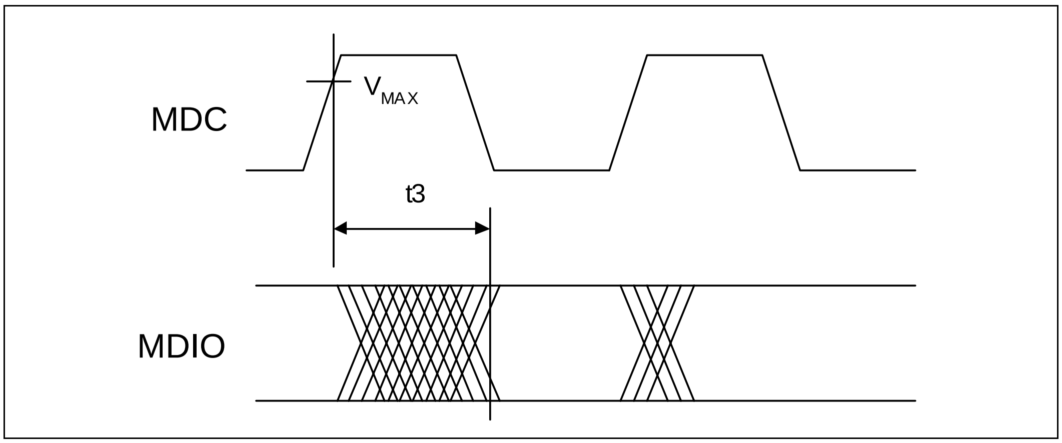


Table 23. MDIO Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
MDIO Setup before MDC.	t1	10	–	–	ns	MDC = 17.8 MHz
		10	–	–	ns	MDC = 2.5 MHz
MDIO Hold after MDC.	t2	10	–	–	ns	MDC = 17.8 MHz
		10	–	–	ns	MDC = 2.5 MHz
MDC to MDIO Output delay	t3	0	–	30	ns	MDC = 17.8 MHz
		0	–	200	ns	MDC = 2.5 MHz

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 23. CPU Port Read Timing Diagram

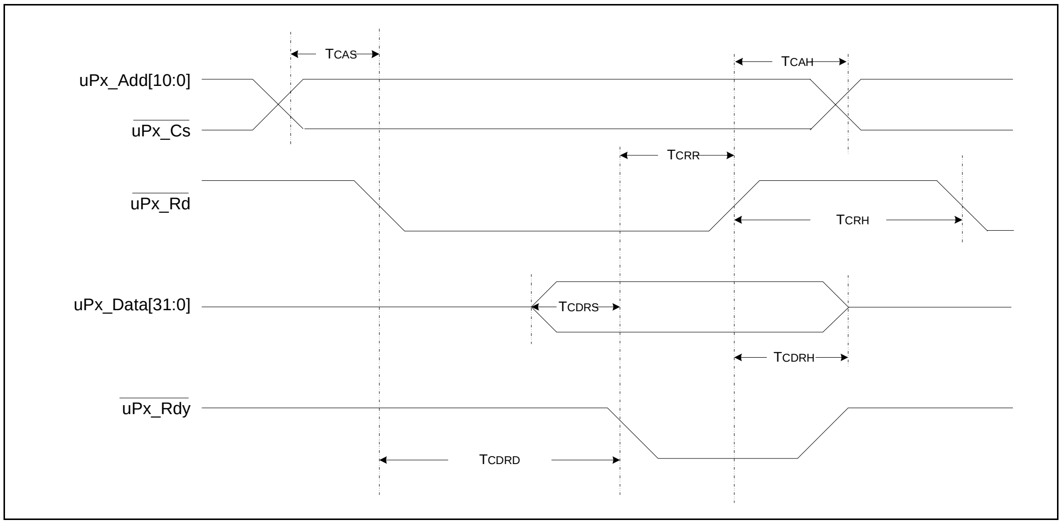


Figure 24. CPU Port Write Timing Diagram

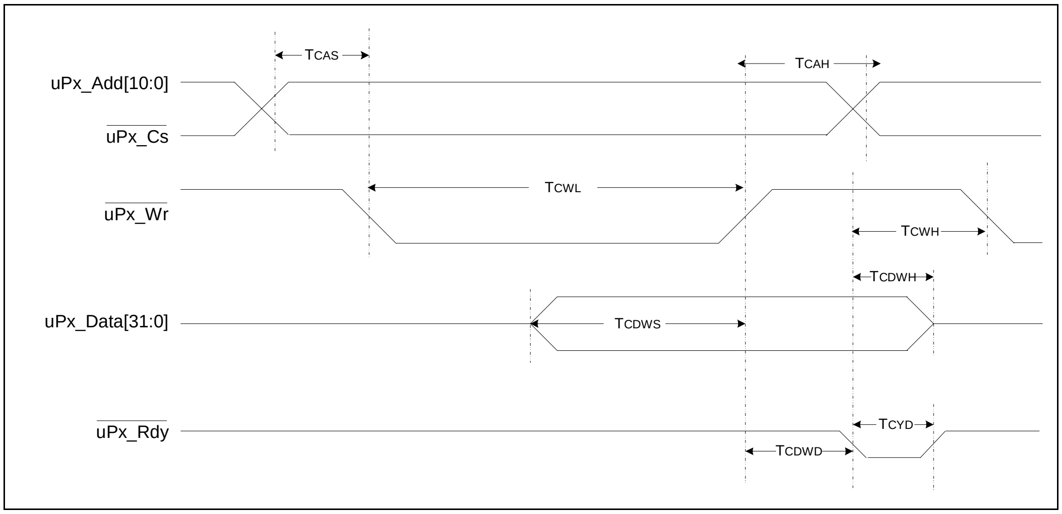


Table 24. CPU Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Test Condition
uPx_Add[12:0], uPx_Cs Setup Time	TCAS	10 ns	–	–	–
uPx_Add[12:0], uPx_Cs Hold Time	TCAH	10 ns	–	–	–
uPx_Rdy Assertion to uPx_Rd Deassertion	TCRR	10 ns	–	–	–
uPx_Rd High Width	TCRH	24 ns (3x cycle)	–	–	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

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Table 24. CPU Timing Parameters (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Test Condition
uPx_Data[31:0] to uPx_Rdy Setup Time	TCDRS	10 ns	–	–	–
uPx_Data[31:0] to uPx_Rd Hold Time	TCDRH	8 ns	–	32 ns	–
Read uPx_Data[31:0] Driving Delay	TCDRD	24 ns	–	120 ns	–
uPx_Wr Width	TCWL	40 ns	–	–	–
uPx_Rdy to uPx_Wr Hold Time	TCWH	16 ns	–	–	–
uPx_Data[31:0] to uPx_Wr Setup Time	TCDWS	10 ns	–	–	–
uPx_Rdy to uPx_Data[31:0] Hold Time	TCDWH	10 ns	–	–	–
uPx_Data[31:0] Latching Delay	TCDWD	8 ns	–	32 ns	–
uPx_Rdy Width in Write Cycle	TCYD	24 ns	–	40 ns	–
Read uPx_Rdy deassertion to uPx_Wr Assertion	TRTW	32 ns	–	–	–
Write uPx_Rdy deassertion to uPx_Rd Assertion	TWTR	32 ns	–	–	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 25. JTAG Timing Diagram

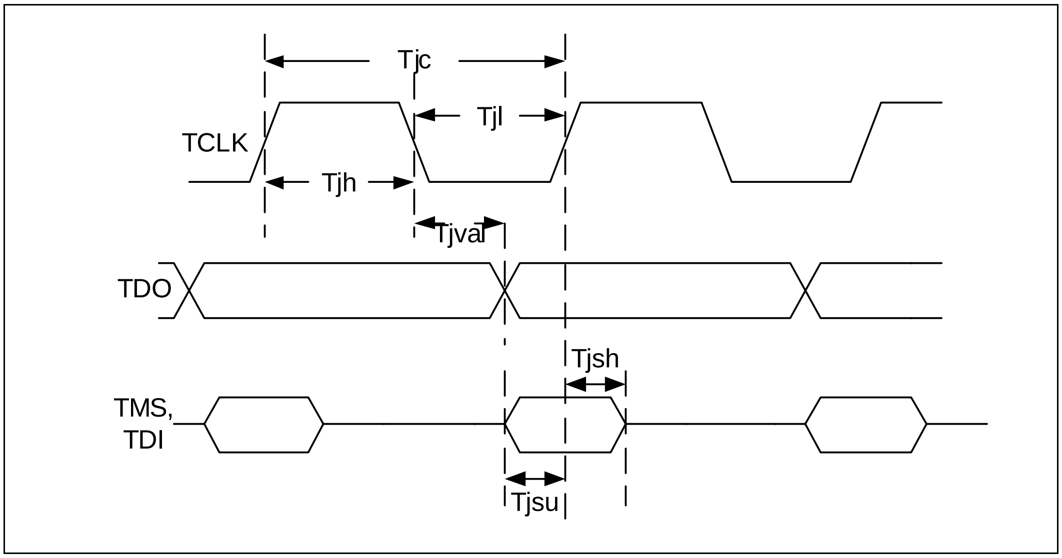


Table 25. JTAG Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TCLK Cycle Time	Tjc	90	–	–	ns	–
TCLK High Time	Tjh	0.4 x Tjc	–	0.6 x Tjc	ns	–
TCLK Low Time	Tjl	0.4 x Tjc	–	0.6 x Tjc	ns	–
TCLK Falling Edge to TDO Valid	Tjval	–	–	25	ns	–
TMS/TDI Setup to TCLK	Tjsu	20	–	–	ns	–
TMS/TDI Hold from TCLK	Tjsh	5	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 26. Transmit Pause Control Interface Diagram

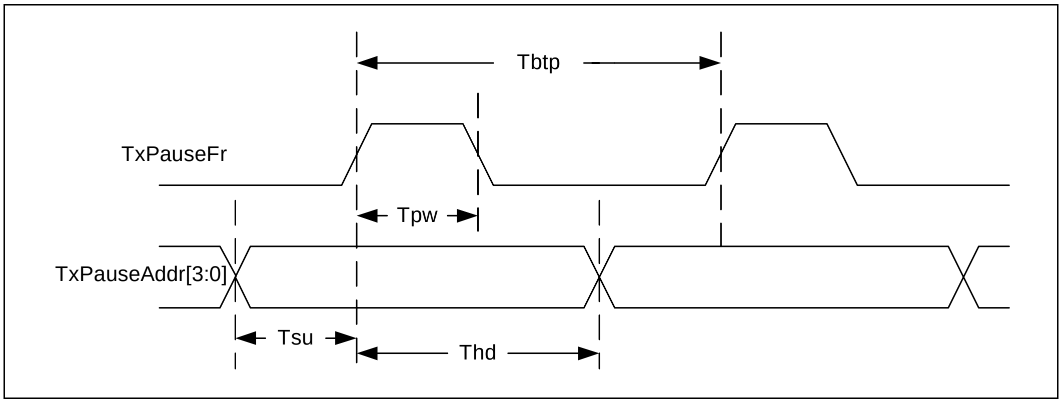


Table 26. Transmit Pause Control Interface Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TxPauseFr Width	Tpw	16	–	–	ns	–
TxPauseAddr[3:0] Setup to TxPauseFr	Tsu	16	–	–	ns	–
TxPauseAddr[3:0] Hold from TxPauseFr	Thd	32	–	–	ns	–
TxPauseFr Pulse to Pulse	Tbtp	48	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 27. Hardware Reset Timing Diagram

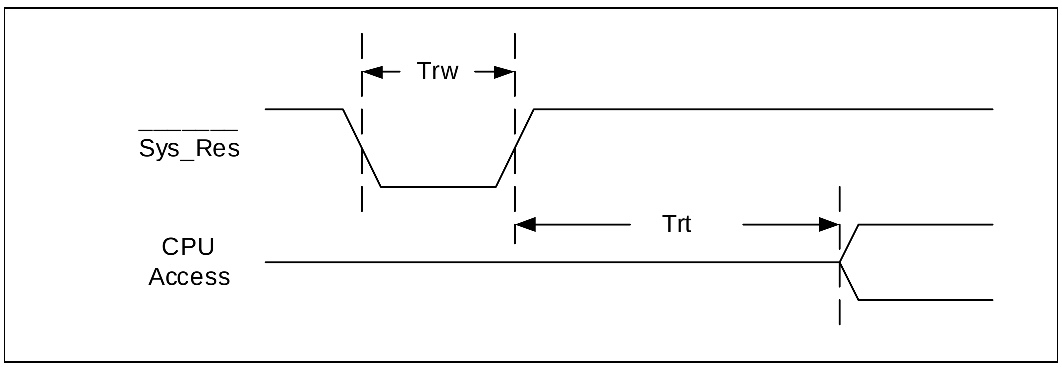


Table 27. Hardware Reset Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Reset Pulse Width	Trw	1	–	–	µs	–
Reset Recovery Time	Trt	200	–	–	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 28. LED Timing Diagram

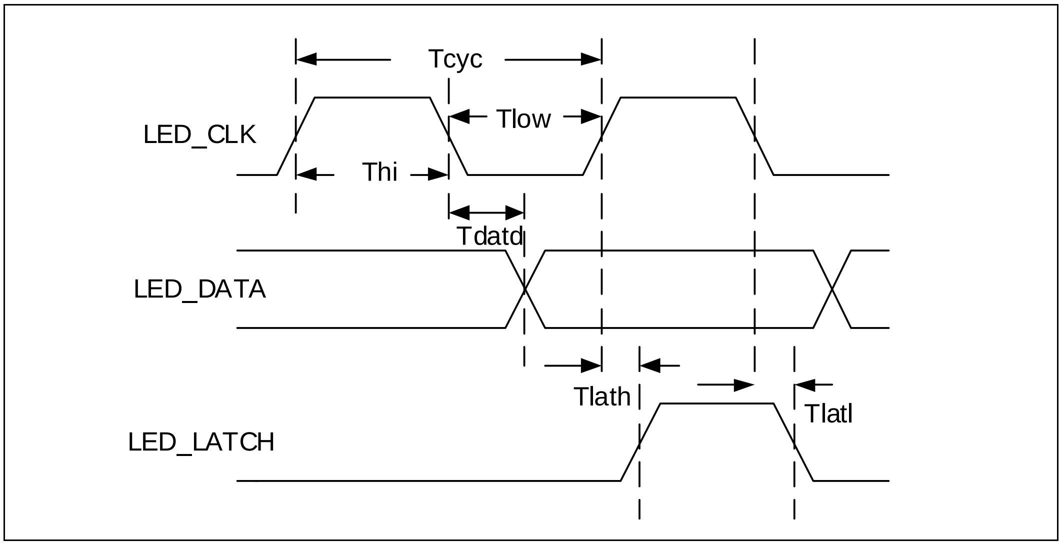


Table 28. LED Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
LED_CLK Cycle Time	Tcyc	2	–	–	µs	–
LED_CLK High Time	Thi	1	–	–	µs	50% duty cycle
LED_CLK Low Time	Tlow	1	–	–	µs	50% duty cycle
LED_CLK Falling Edge to LED_DATA Valid	Tdatd	–	–	–	ns	–
LED_CLK Rising Edge to LED_LATCH Rising Edge	Tlath	–	–	–	ns	–
LED_CLK Falling Edge to LED_LATCH Falling Edge	Tlatl	–	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 29. SPI4-2 Transmit FIFO Status Bus Timing Diagram

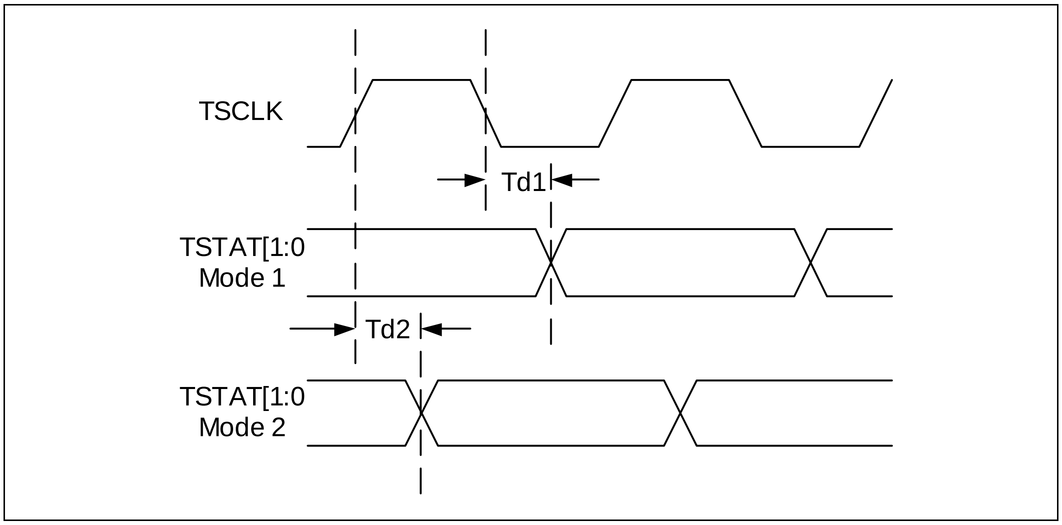


Table 29. SPI4-2 Transmit FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TSCLK Falling Edge to TSTAT[1:0] Valid (Mode 1)	Td1	–	–	280	ps	–
TSCLK Rising Edge to TSTAT[1:0] Valid (Mode 2)	Td2	–	–	280	ps	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 30. SPI4-2 Receive FIFO Status Bus Timing Diagram

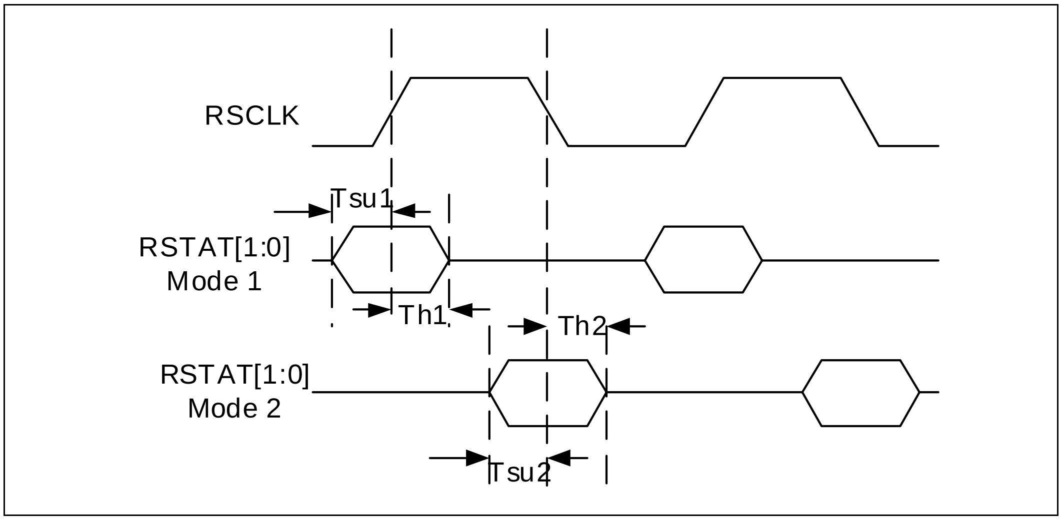


Table 30. SPI4-2 Receive FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
RSTAT[1:0] Setup to RSCLK Rising Edge (Mode 1)	Tsu1	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Rising Edge (Mode 1)	Th1	0.5	–	–	ns	–
RSTAT[1:0] Setup to RSCLK Falling Edge (Mode 2)	Tsu2	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Falling Edge (Mode 2)	Th2	0.5	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

6.0 Register Definitions

6.1 Introduction

This section provides information on the location and functionality of the control and status registers contained in the IXF1010.

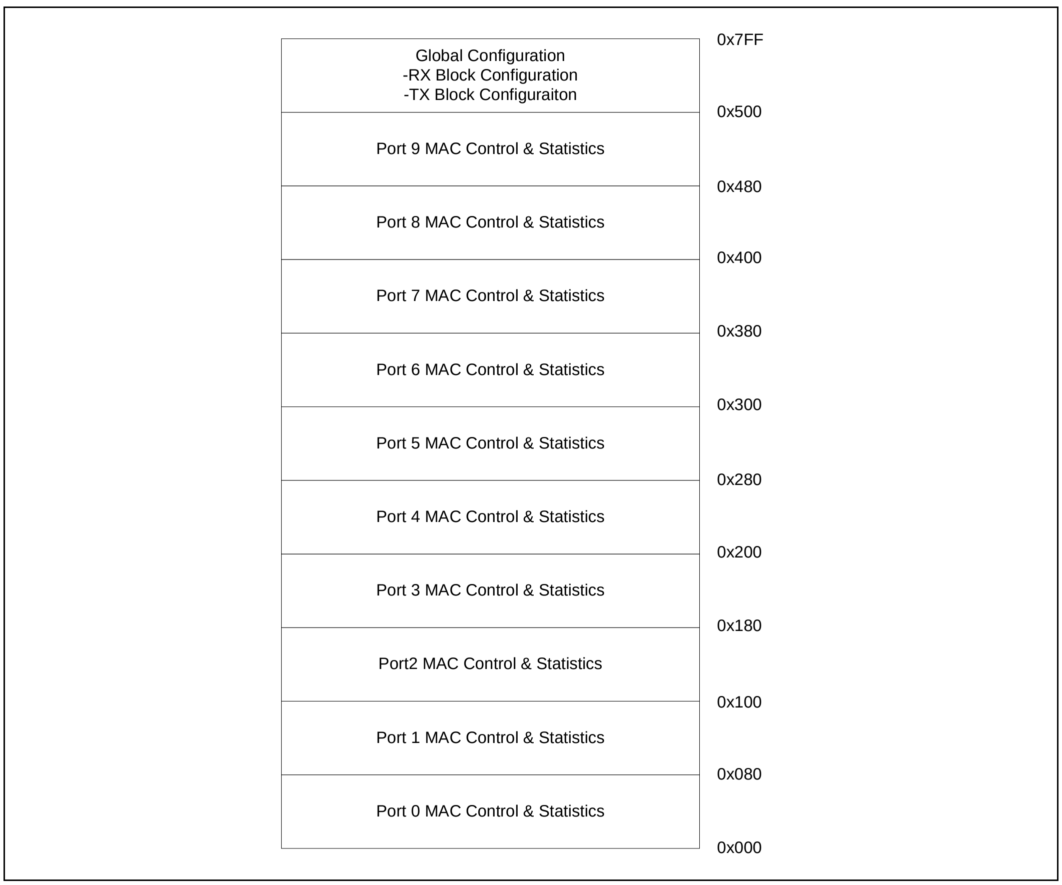
6.2 Document Structure

This document is structured to give a general overview of the register map and an in-depth description of each bit of a register in later sections.

6.3 Graphical Representation

Figure 31 represents an overview of the IXF1010 global control status registers that are used to configure or report on all ports.

Figure 31. Memory Overview Diagram

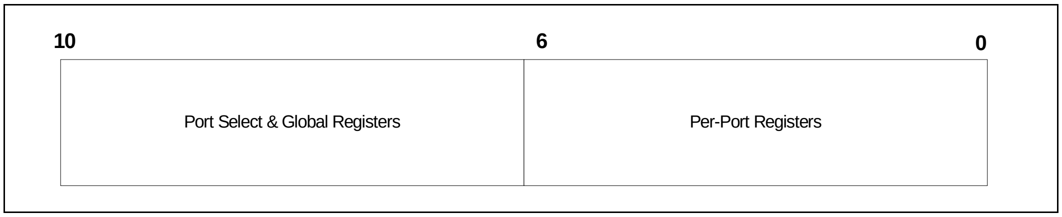


6.4 Per Port Registers

The following section covers all of the registers that are replicated in each of the 10 ports in the IXF1010. These registers perform an identical function in each port.

The address vector for the IXF1010 is 11 bits wide. This allows for 7 bits of port-specific access and a 4-bit vector to address each port and all global registers. The address format is shown in Figure 32.

Figure 32. Register Overview Diagram



6.5 Memory Map

Table 31 through Table 39 on page 75 provide the IXF1010 memory maps. A number of global control and status registers are used to configure or report on all ports, and some registers are replicated on a per-port basis.

Note: All registers in the IXF1010 are 32 bits.

Table 31. MAC Control Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
StationAddressLow	32	R/W	76	0x00
StationAddressHigh	32	R/W	76	0x01
Reserved	32	RO	–	0x02
FDFCType	32	R/W	76	0x03
Reserved	32	RO	–	0x04
Reserved	32	RO	–	0x05
Reserved	32	RO	–	0X06
FCTxTimerValue	32	R/W	76	0x07
FDFCAddressLow	32	R/W	77	0x08
FDFCAddressHigh	32	R/W	77	0x09
IPGReceiveTime1	32	R/W	77	0x0A
IPGReceiveTime2	32	R/W	77	0x0B
IPGTransmitTime	32	R/W	77	0x0C
Reserved	32	R/W	--	0x0D
PauseThreshold	32	R/W	78	0x0E
MaxFrameSize	32	R/W	78	0x0F
RGMII Speed	32	R/W	78	0x10
Reserved	32	RO	–	0x11
FCEnable	32	R/W	78	0x12
Reserved	32	RO	–	0x13
ShortRuntsThreshold	32	R/W	79	0x14
DiscardUnknownControlFrame	32	R/W	79	0x15
Reserved	32	RO	–	0x16
Reserved	32	RO	–	0x17
DiverseConfigWrite	32	R/W	79	0x18
PacketFilterControl	32	R/W	80	0x19
PortMulticastAddressLow	32	R/W	81	0x1A
PortMulticastAddressHigh	32	R/W	81	0x1B
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 32. MAC RX Statistics Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RxOctetsTotalOK	32	RR	82	0x20
RxOctetsBAD	32	RR	82	0x21
RxUCPckts	32	RR	82	0x22
RxMCPkts	32	RR	82	0x23
RxBCPkts	32	RR	82	0x24
RxPkts64Octets	32	RR	82	0x25
RxPkts65to127Octets	32	RR	82	0x26
RxPkts128to255Octets	32	RR	82	0x27
RxPkts256to511Octets	32	RR	82	0x28
RxPkts512to1023Octets	32	RR	82	0x29
RxPkts1024to1518Octets	32	RR	82	0x2A
RxPkts1519toMaxOctets	32	RR	82	0x2B
FCSErrors	32	RR	82	0x2C
Tagged	32	RR	82	0x2D
RxDataError	32	RR	82	0x2E
Align Errors	32	RR	82	0x2F
LongErrors	32	RR	82	0x30
JabberErrors	32	RR	82	0x31
PauseMacControlReceivedCounter	32	RR	82	0x32
UnknownMacControlFrameCounter	32	RR	82	0x33
VeryLongErrors	32	RR	82	0x34
RuntErrors	32	RR	82	0x35
ShortErrors	32	RR	82	0x36
CarrierExtendError	32	RR	82	0x37
SequenceErrors	32	RR	82	0x38
SymbolErrors	32	RR	82	0x39

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 33. MAC TX Statistics Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAX TX Statistics Registers (Port Index + Offset)				
OctetsTransmittedOK	32	RR	85	0x40
OctetsTransmittedBad	32	RR	85	0x41
TxUCPkts	32	RR	85	0x42
TxMCPkts	32	RR	85	0x43
TxBCPkts	32	RR	85	0x44
TxPkts64Octets	32	RR	85	0x45
TxPkts65to127Octets	32	RR	85	0x46
TxPkts128to255Octets	32	RR	85	0x47
TxPkts256to511Octets	32	RR	85	0x48
TxPkts512to1023Octets	32	RR	85	0x49
TxPkts1024to1518Octets	32	RR	85	0x4A
TxPkts1519toMaxOctets	32	RR	85	0x4B
DeferredTx	32	RR	85	0x4C
TxTotalCollisions	32	RR	85	0x4D
TxSingleCollisions	32	RR	85	0x4E
TxMultipleCollisions	32	RR	85	0x4F
TxLateCollisions	32	RR	85	0x50
ExcessiveCollisionErrors	32	RR	85	0x51
ExcessiveDeferralErrors	32	RR	85	0x52
TxExcessiveLengthDrop	32	RR	85	0x53
TxUnderrun	32	RR	85	0x54
Tagged	32	RR	85	0x55
CRCError	32	RR	85	0x56
TxPauseFrames	32	RR	85	0x57
FlowControlCollisionsSend	32	RR	85	0x58
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 34. PHY Autoscan Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
PHY Autoscan Registers (Port Index + Offset)				
Control	32	RO	--	0x60
Status	32	RO	--	0x61
PHY Identification Register 1	32	RO	--	0x62
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 34. PHY Autoscan Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Offset
PHY Autoscan Registers (Port Index + Offset)				
PHY Identification Register 2	32	RO	--	0x63
Auto-Negotiation Advertisement	32	RO	--	0x64
Auto-Negotiation Link Partner Base Page Ability	32	RO	--	0x65
Auto-Negotiation Expansion	32	RO	--	0x66
Auto-Negotiation Next Page Transmit	32	RO	--	0x67
Reserved	32	RO	--	0x68
Reserved	32	RO	--	0x69
Reserved	32	RO	--	0x6A
Reserved	32	RO	--	0x6B
Reserved	32	RO	--	0x6C
Reserved	32	RO	--	0x6D
Reserved	32	RO	--	0x6E
Reserved	32	RO	--	0x6F
Vendor Specific	32	RO	--	0x70
Vendor Specific	32	RO	--	0x71
Vendor Specific	32	RO	--	0x72
Vendor Specific	32	RO	--	0x73
Vendor Specific	32	RO	--	0x74
Vendor Specific	32	RO	--	0x75
Vendor Specific	32	RO	--	0x76
Vendor Specific	32	RO	--	0x77
Vendor Specific	32	RO	--	0x78
Vendor Specific	32	RO	--	0x79
Vendor Specific	32	RO	--	0x7A
Vendor Specific	32	RO	--	0x7B
Vendor Specific	32	RO	--	0x7C
Vendor Specific	32	RO	--	0x7D
Vendor Specific	32	RO	--	0x7E
Vendor Specific	32	RO	--	0x7F

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 35. Global Status and Configuration Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
Port Enable	32	R/W	88	0x500
Link LED Enable	32	R/W	90	0x502
Reserved	32	RO	–	0x503
Reserved	32	RO	–	0x504
MAC Soft Reset	32	R/W	91	0x505
MDIO Soft Reset	32	R/W	91	0x506
Pause Behavior	32	R/W	92	0x507
CPU Interface	32	R/W	92	0x508
LED Control	32	R/W	92	0x509
LED Flash Rate	32	R/W	93	0x50A
LED Fault Disable	32	R/W	93	0x50B
Reserved	32	RO	–	0x50C

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 36. RX Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
RX FIFO High Watermark Port 0	32	R/W	95	0x580
RX FIFO High Watermark Port 1	32	R/W	95	0x581
RX FIFO High Watermark Port 2	32	R/W	95	0x582
RX FIFO High Watermark Port 3	32	R/W	95	0x583
RX FIFO High Watermark Port 4	32	R/W	95	0x584
RX FIFO High Watermark Port 5	32	R/W	95	0x585
RX FIFO High Watermark Port 6	32	R/W	95	0x586
RX FIFO High Watermark Port 7	32	R/W	95	0x587
RX FIFO High Watermark Port 8	32	R/W	95	0x588
RX FIFO High Watermark Port 9	32	R/W	95	0x589
RX FIFO Low Watermark Port 0	32	R/W	96	0x58A
RX FIFO Low Watermark Port 1	32	R/W	96	0x58B
RX FIFO Low Watermark Port 2	32	R/W	96	0x58C
RX FIFO Low Watermark Port 3	32	R/W	96	0x58D
RX FIFO Low Watermark Port 4	32	R/W	96	0x58E
RX FIFO Low Watermark Port 5	32	R/W	96	0x58F
RX FIFO Low Watermark Port 6	32	R/W	96	0x590
RX FIFO Low Watermark Port 7	32	R/W	96	0x591

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 36. RX Block Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Address
RX FIFO Low Watermark Port 8	32	R/W	96	0x592
RX FIFO Low Watermark Port 9	32	R/W	96	0x593
Number of Frames Removed on Port 0	32	RR	97	0x594
Number of Frames Removed on Port 1	32	RR	97	0x595
Number of Frames Removed on Port 2	32	RR	97	0x596
Number of Frames Removed on Port 3	32	RR	97	0x597
Number of Frames Removed on Port 4	32	RR	97	0x598
Number of Frames Removed on Port 5	32	RR	97	0x599
Number of Frames Removed on Port 6	32	RR	97	0x59A
Number of Frames Removed on Port7	32	RR	97	0x59B
Number of Frames Removed on Port8	32	RR	97	0x59C
Number of Frames Removed on Port 9	32	RR	97	0x59D
Reserved	32	RO	–	0x59E
RX FIFO Errored Frames Drop Enable	32	R/W	98	0x59F
RX FIFO Overflow Event	32	RR	100	0x5A0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 37. TX Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO High Watermark Port 0	32	R/W	101	0x600
TX FIFO High Watermark Port 1	32	R/W	101	0x601
TX FIFO High Watermark Port 2	32	R/W	101	0x602
TX FIFO High Watermark Port 3	32	R/W	101	0x603
TX FIFO High Watermark Port 4	32	R/W	101	0x604
TX FIFO High Watermark Port 5	32	R/W	101	0x605
TX FIFO High Watermark Port 6	32	R/W	101	0x606
TX FIFO High Watermark Port 7	32	R/W	101	0x607
TX FIFO High Watermark Port 8	32	R/W	101	0x608
TX FIFO High Watermark Port 9	32	R/W	101	0x609
TX FIFO Low Watermark Port 0	32	R/W	101	0x60A
TX FIFO Low Watermark Port 1	32	R/W	102	0x60B
TX FIFO Low Watermark Port 2	32	R/W	102	0x60C
TX FIFO Low Watermark Port 3	32	R/W	102	0x60D
TX FIFO Low Watermark Port 4	32	R/W	102	0x60E
TX FIFO Low Watermark Port 5	32	R/W	102	0x60F

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 37. TX Block Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO Low Watermark Port 6	32	R/W	102	0x610
TX FIFO Low Watermark Port 7	32	R/W	102	0x611
TX FIFO Low Watermark Port 8	32	R/W	102	0x612
TX FIFO Low Watermark Port 9	32	R/W	102	0x613
MAC Transfer Threshold Port 0	32	R/W	104	0x614
MAC Transfer Threshold Port 1	32	R/W	104	0x615
MAC Transfer Threshold Port 2	32	R/W	104	0x616
MAC Transfer Threshold Port 3	32	R/W	104	0x617
MAC Transfer Threshold Port 4	32	R/W	104	0x618
MAC Transfer Threshold Port 5	32	R/W	104	0x619
MAC Transfer Threshold Port 6	32	R/W	104	0x61A
MAC Transfer Threshold Port 7	32	R/W	104	0x61B
MAC Transfer Threshold Port 8	32	R/W	104	0x61C
MAC Transfer Threshold Port 9	32	R/W	104	0x61D
TX FIFO Overflow Event	32	RR	107	0x61E
Reserved	32	RO	–	0x61F
Reserved	32	RO	–	0x620
Info Out of Sequence	32	RR	108	0x621
Number of Frames Dropped on Port 0	32	RR	109	0x622
Number of Frames Dropped on Port 1	32	RR	109	0x623
Number of Frames Dropped on Port 2	32	RR	109	0x624
Number of Frames Dropped on Port 3	32	RR	109	0x625
Number of Frames Dropped on Port 4	32	RR	109	0x626
Number of Frames Dropped on Port 5	32	RR	109	0x627
Number of Frames Dropped on Port 6	32	RR	109	0x628
Number of Frames Dropped on Port 7	32	RR	109	0x629
Number of Frames Dropped on Port 8	32	RR	109	0x62A
Number of Frames Dropped on Port 9	32	RR	109	0x62B

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 38. MDIO Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MDI Single Command	32	R/W	110	0x680
MDI Single Read and Write Data	32	R/W	110	0x681
Autoscan PHY Address Enable	32	R/W	110	0x682
MDI Control	32	R/W	111	0x683
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 39. SPI4-2 Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
SPI4-2 Block Registers (Port Index + Offset)				
SPI4-2 Rx Burst Size Register	32	R/W	112	0x700
SPI4-2 Rx Training Register	32	R/W	112	0x701
SPI4-2 Calendar Register	32	R/W	113	0x702
SPI4-2 Tx Synchronization Register	32	R/W	113	0x703
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.1 MAC Control Registers

Table 40 through Table 58 on page 81provide details on the control and status registers associated with each MAC port. The register address is '**Port_index + 0x****', where the port index is set at any value from 0x0 through 0x5. All registers are 32 bits.

Table 40. Station Address Register (Low) (Addr: Port_Index + 0x00)

Bit	Name	Description	Type[1]	Default
31:0	StationAddress Low	Source MAC address bit 31-0. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 41. Station Address Register (High) (Addr: Port_Index + 0x01)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	StationAddress High	Source MAC address bit 47-32. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x0000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 42. FDFC Type Register (Addr: Port_Index + 0x03)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFCType	Contains the value of the type field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0x8808

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 43. FC TX Timer Value Register (Addr: Port_Index + 0x07)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FCTxTimer Value	The pause length sent to the receiving station in 512 bit times	R/W	0x005E

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 44. FDFC Address Low Register (Addr: Port_Index + 0x08)

Bit	Name	Description	Type[1]	Default
31:0	FDFC AddressLow	Contains the value of the lowest 32 bits of the destination address field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0xC2000001
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 45. FDFC Address High Register (Addr: Port_Index + 0x09)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFC AddressHigh	Contains the value of the highest 16 bits of the destination address filed transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0x0180
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 46. IPG Receive Time 1 Register (Addr: Port_Index + 0x0A)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPGReceive Time1	First part of the IPG time for non back-to-back transmissions	R/W	0x0008
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 47. IPG Receive Time 2 Register (Addr: Port_Index + 0x0B)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPGReceive Time2	Second part of the IPG time for non back-to-back transmissions	R/W	0x0007
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 48. IPG Transmit Time Register (Addr: Port_Index + 0x0C)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPGTransmit Time	IPG time for back-to-back transmissions	R/W	0x0008
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 49. Pause Threshold Register (Addr: Port_Index + 0x0E)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Pause Threshold	When a pause frame is sent, an internal timer checks when a new pause frame must be scheduled for transmission to keep the link partner in pause mode. The pause threshold value is the minimum time to send before the earlier pause frame is aged out.	R/W	0x002F
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 50. Max Frame Size Register (Addr: Port_Index + 0x0F)

Bit	Name	Description	Type[1]	Default
31:14	Reserved	Reserved	RO	0x0000
13:0	MaxFrameSize	The maximum frame size the MAC can receive or transmit without activating any error counters, and without truncation. The maximum frame size is internally adjusted by +4 if VLAN is tagged.	R/W	0x05EE
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 51. RGMII Speed Register (Addr: Port_Index + 0x10)

Bit	Name	Description	Type[1]	Default
31:2	Reserved	Reserved	RO	0x00000000
1:0	RGMII Speed	These bits are used to define the speed of the IXF1010 operation. 01 = 100 Mbps - RGMII TX_CLK is 25 MHz 1x = 1 Gbps - RGMII TX_CLK is 125 MHz	R/W	11
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 52. FC Enable Register Bit Definition (Addr: Port_Index + 0x12)

Bit	Name	Description	Type[1]	Default
Register Description: Indicates flow control settings of the IXF1010.				
31:2	Reserved	Reserved	RO	0x00000001
1	TXFDFC	1 = Enable TX FD Flow Control 0 = Disables	R/W	1
0	RXFDFC	1 = Enable RX FD Flow Control 0 = Disables	R/W	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 53. Short Runts Threshold Register (Addr: Port_Index + 0x14)

Bit	Name	Description	Type[1]	Default
31:5	Reserved	Reserved	RO	0x0000000
4:0	ShortRunts Threshold	Holds the value in bytes, which applies to the threshold in determining between runts and short.	R/W	01000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 54. Discard Unknown Control Frame Register (Addr: Port_Index + 0x15)

Bit	Name	Description	Type[1]	Default
31:1	Reserved	Reserved	RO	0x00000000
0	DiscardUnknown ControlFrame	0 = Keep unknown control frames 1 = Discard unknown control frames.	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 55. Diverse Config Register (Addr: Port_Index + 0x18)

Bit	Name	Description	Type[1]	Default
Register Description: This register enables the padding of undersized frames on transmit and automatic CRC generation. For proper operation, if padding of undersized frames is enabled, the automatic CRC generation must be enabled.				0x0000110D
31:8	Reserved	Reserved	RO	0
7	pad_enable	Enable padding of undersized packets	R/W	0
6	crc_add	Enable automatic CRC appending	R/W	0
5:0	Reserved	Reserved	RO	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

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Table 56. Packet Filter Control Register (Addr: Port_Index + 0x19)

Bit	Name	Description	Type[1]	Default
Register Description: This register allows for specific packet types to be marked for filtering, and is used in conjunction with the RX FIFO Errored Frames Drop Enable Register				0x00000000
31:6	Reserved	Reserved		0x000000
5	CRCErrorPass	This bit enables a Global filter on frames with a CRC Error. When CRCErrorPASS = 0, all frames with a CRC Error are marked as bad. **Note:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 74 on page 98). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When CRCErrorPASS = 1, frames with a CRC Error are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
4	PauseFramePass	This bit enables a Global filter on Pause frames. When PauseFramePass = 0, all Pause frames are marked as bad. **Note:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 74 on page 98). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When PauseFramePass = 1, all Pause frames are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
3	VLANDropEn	This bit enables a Global filter on VLAN frames. When VLANDropEn = 0, all VLAN frames are passed to the SPI4-2 Interface. When VLANDropEn = 1, all VLAN frames are dropped.	R/W	0
2	B/CastDropEn	This bit enables a Global filter on Broadcast frames. When B/CastDropEn = 0, all broadcast frames are passed to the SPI4-2 Interface. When B/CastDropEn = 1, all broadcast frames are dropped.	R/W	0
1	M/CastMatchEn	This bit enables a filter on multicast frames. If this bit = 0, all multicast frames are good and are passed to the SPI4-2 Interface. If this bit = 1, only multicast frames with a destination address that matches the PortMulticastAddress is forwarded. All other multicast frames are dropped.	R/W	0
0	U/CastMatchEn	This bit enables a filter on unicast frames. If this bit = 0, all unicast frames are good and are passed to the SPI4-2 interface. If this bit = 1, only unicast frames with a destination address that matches the Station Address is forwarded. All other unicast frames are dropped.	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 57. Port Multicast Address Low Register Bit Definition (Addr: Port_Index + 0x1A)

Bit	Name	Description	Type[1]	Default
31:0	Port Multicast Address Low	This address is used to compare against multicast frames at the receiving side if multicast filtering is enabled. This register contains bits 31:0 of the address.	R/W	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 58. Port Multicast Address High Register Bit Definition (Addr: Port_Index + 0x1B)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Port Multicast Address High	This address is used to compare against multicast frames at the receiving side if Multicast filtering is enabled. This register contains bits 47:32 of the address.	R/W	0x0000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.2 MAC RX Statistics Register Overview

The MAC RX Statistics Registers contain the MAC receiver statistic counters and are cleared when read. The software polls these registers and accumulates values to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 59 covers the RX statistics for the10 MAC ports. The address is identical to the port number.

Table 59. RX Statistics Registers Addr: Port_Index + 0x20 - Port_Index + 0x39)

Name	Description	Address	Type[1]	Default
RxOctetsTotalOK	Counts the bytes received in all legal frames, including all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x20	RR	0x00000000
RxOctetsBAD[2]	Counts the bytes received in all bad frames of a size greater than or equal to 64 bytes. A bad frame is defined as a properly framed packet containing a CRC, alignment error, or code violation. The 64-byte value is measured from the destination address, up to and including CRC. The initial preamble and SFD are not included in this value. **Note:** This register does not increment the Bad Octet count on undersized receive packets.	Port_Index + 0x21	RR	0x00000000
RxUCPkts	The total number of unicast packets received (excluding bad packets) **Note:** This count includes non-pause control and VLAN packets, which are also counted in other counters. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x22	RR	0x00000000
RxMCPkts	The total number of multicast packets received (excluding bad packets **Note:** This count includes pause control packets, which are also counted in the PauseMacControl-ReceivedCounter. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x23	RR	0x00000000
RxBCPkts	The total number of Broadcast packets received (excluding bad packets)	Port_Index + 0x24	RR	0x00000000
RxPkts64Octets	The total number of packets received (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x25	RR	0x00000000
RxPkts65to127 Octets	The total number of packets received (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x26	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*maxframesize, dependent on where the maxframesize variable is set. If maxframesize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1.

Table 59. RX Statistics Registers Addr: Port_Index + 0x20 - Port_Index + 0x39) (Continued)

Name	Description	Address	Type[1]	Default
RxPkts128t0255 Octets	The total number of packets received (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field	Port_Index + 0x27	RR	0x00000000
RxPkts256to511 Octets	The total number of packets received (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x28	RR	0x00000000
RxPkts512to1023 Octets	The total number of packets received (including bad packets) that were [512-1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x29	RR	0x00000000
RxPkts1024to1518 Octets	The total number of packets received (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x2A	RR	0x00000000
RxPkts1519toMax Octets	The total number of packets received (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max, including the tag	Port_Index + 0x2B	RR	0x00000000
FCSErrors	Number of frames received with legal size, but with wrong CRC field (also called FCS field)	Port_Index + 0x2C	RR	0x00000000
Tagged	Number of frames (including bad packets) with VLAN tag (Type field = 0x8100)	Port_Index + 0x2D	RR	0x00000000
RxDataError	Number of frames received with legal length, containing a code violation (signaled with RX_ERR on RGMII)	Port_Index + 0x2E	RR	0x00000000
AlignErrors	Frames with a legal frame size, but containing less than 8 additional bits. The CRC of the frame is wrong when the additional bits are stripped. If the CRC is OK, the frame is not counted, but treated as an OK frame.	Port_Index + 0x2F	RR	0x00000000
LongErrors[2]	Frames bigger than the maximum allowed, with both OK CRC and the integral number of octets Default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register Frames bigger than the larger of 2*maxframesize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x30	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*maxframesize, dependent on where the maxframesize variable is set. If maxframesize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1.

Table 59. RX Statistics Registers Addr: Port_Index + 0x20 - Port_Index + 0x39) (Continued)

Name	Description	Address	Type[1]	Default
JabberErrors	Frames bigger than the maximum allowed, with either a bad CRC or a non-integral number of octets. The default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*maxframesize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x31	RR	0x00000000
PauseMacControl ReceivedCounter	Number of Pause MAC control frames received	Port_Index + 0x32	RR	0x00000000
UnknownMac ControlFrame Counter	Number of MAC control frames received with an op code different from 0001 (Pause)	Port_Index + 0x33	RR	0x00000000
VeryLongErrors[2]	Frames bigger than the larger of 2*maxframesize and 50000 bits	Port_Index + 0x34	RR	0x00000000
RuntErrors	The total number of packets received that are less than 64 octets in length, but longer than or equal to 96 bit times. **Note:** The “ShortRuntsThreshold” Register controls the byte count used to determine the difference between Runts and Shorts, and therefore controls which counter is incremented for a given frame size. This counter is only updated after receipt of two good frames.	Port_Index + 0x35	RR	0x00000000
Short Errors	The total number of packets received that are less than 96 bit times, which corresponds to a 4-byte frame with a well formed preamble and SFD. This counter indicates fragment sizes illegal in all modes, and is only fully updated after reception of a good frame following a fragment.	Port_Index + 0x36	RR	0x00000000
Carrier Extend Error	Gigabit half-duplex event only Note: N/A - half-duplex only	Port_Index + 0x37	RR	0x00000000
SequenceErrors	Records the number of sequencing errors that occur. **Note:** The IXF1010 does not support fiber.	Port_Index + 0x38	RR	0x00000000
SymbolErrors	Records the number of symbol errors encountered by the PHY	Port_Index + 0x39	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*maxframesize, dependent on where the maxframesize variable is set. If maxframesize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1.

6.5.3 TX Statistics Register Overview

The MAC TX Statistics Registers contain all the MAC transmit statistic counters and are cleared when read. The software must poll these registers to accumulate values and ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 60 covers all 10 MAC ports TX statistics; the address is identical to the port number.

Table 60. STAT-TX Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
OctetsTransmittedOK	Counts the bytes transmitted in all legal frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. Any initial collided transmission attempts before a successful frame transmission do not add to this counter.	Port_Index + 0x40	RR	0x00000000
OctetsTransmittedBad	Counts the bytes transmitted in all bad frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted Late collision counted: The count is close to the actual number of bytes transmitted before the frame is discarded Excessive collision counted: The count is close to the actual number of bytes transmitted before the frame is discarded TX under-run counted: The count is expected to match the number of bytes actually transmitted before the frame is discarded TX CRC error counted: All bytes not sent with success are counted by this counter Any initial collided transmission attempts before a successful frame transmission do not add to this counter	Port_Index + 0x41	RR	0x00000000
TxUCPkts	The total number of unicast packets transmitted (excluding bad packets)	Port_Index + 0x42	RR	0x00000000
TxMCPkts	The total number of multicast packets transmitted (excluding bad packets) **Note:** This count includes pause control packets which are also counted in the TxPauseFrames Counter. Thus, these types of packets are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x43	RR	0x00000000
TxBCPkts	The total number of broadcast packets transmitted (excluding bad packets)	Port_Index + 0x44	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 60. STAT-TX Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58) (Continued)

Name	Description	Address	Type[1]	Default
TxPkts64Octets	The total number of packets transmitted (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x45	RR	0x00000000
Txpkts65to127Octets	The total number of packets transmitted (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x46	RR	0x00000000
Txpkts128to255Octets	The total number of packets transmitted (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128 - 255 bytes, including tag field	Port_Index + 0x47	RR	0x00000000
Txpkts256to511Octets	The total number of packets transmitted (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x48	RR	0x00000000
Txpkts512to1023Octets	The total number of packets transmitted (including bad packets) that were [512 - 1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x49	RR	0x00000000
Txpkts1024to1518Octets	The total number of packets transmitted (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x4A	RR	0x00000000
Txpkts1519toMaxOctets	The total number of packets transmitted (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1526-max, including the tag	Port_Index + 0x4B	RR	0x00000000
DeferredTx (C)	Number of times the initial transmission attempt of a frame is postponed due to another frame already being transmitted on the Ethernet network. TxTotalCollisions **Note**: N/A - half-duplex only	Port_Index + 0x4C	RR	0x00000000
TxTotal Collisions	Sum of all collision events **Note**: N/A - half-duplex only	Port_Index + 0x4D	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 60. STAT-TX Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58) (Continued)

Name	Description	Address	Type[1]	Default
TxSingleCollisions	A count of successfully transmitted frames on a particular interface where the transmission is inhibited by exactly one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the MultipleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4E	RR	0x00000000
TxMultipleCollisions	A count of successfully transmitted frames on a particular interface for which transmission is inhibited by more than one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the SingleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4F	RR	0x00000000
TxLateCollisions	The number of times a collision is detected on a particular interface later than 512 bit-times into the transmission of a packet. Such frame are terminated and discarded. **Note**: N/A - half-duplex only	Port_Index + 0x50	RR	0x00000000
ExcessiveCollisionErrors	A count of frames, which collides 16 times and is then discarded by the MAC. Not effecting xMultipleCollisions Note: N/A - half-duplex only	Port_Index + 0x51	RR	0x00000000
ExcessiveDeferralErrors	Number of times frame transmission is postponed more than 2*MaxFrameSize due to another frame already being transmitted on the Ethernet network. This causes the MAC to discard the frame. **Note**: N/A - half-duplex only	Port_Index + 0x52	RR	0x00000000
TxExcessiveLengthDrop	Frame transmissions aborted by the MAC because the frame is longer than maximum frame size. These frames are truncated by the MAC when the maximum frame size violation is detected by the MAC.	Port_Index + 0x53	RR	0x00000000
TxUnderrun	Internal TX error which causes the MAC to end the transmission before the end of the frame because the MAC did not get the needed data in time for transmission. The frames are lost and a fragment or a CRC error is transmitted.	Port_Index + 0x54	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 60. STAT-TX Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58) (Continued)

Name	Description	Address	Type[1]	Default
Tagged	Number of OK frames with VLAN tag. (Type field = 0x8100).	Port_Index + 0x55	RR	0x00000000
CRCError	Number of frames transmitted with a legal size, but with the wrong CRC field (also called FCS field)	Port_Index + 0x56	RR	0x00000000
TxPauseFrames	Number of pause MAC frames transmitted	Port_Index + 0x57	RR	0x00000000
FlowControlCollisionsSend	Collisions generated on purpose on incoming frames, to avoid reception of traffic, while the port is in half-duplex and has flow control enabled, and do not have sufficient memory to receive more frames. Note: Due to the internal counting technique, a last frame might have to be transmitted after last flow control collision send to get the correct statistic. **Note**: N/A - half-duplex only	Port_Index + 0x58	RR	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.4 Global Status and Configuration Register Overview

Table 61 through Table 70 on page 93 provide an overview for the Global Control and Status Registers.

Table 61. Port Enable Register

Name	Description	Address	Type[1]	Default
Port Enable Register	A control register for each port in IXF1010. Port ID = bit position in the register. To make a port active, the bit must be set High (for example, port 4 active implies register value = 0001.0000). Setting the bit to 0 de-asserts the reset. The default state for this register is for all 10 ports to be active.	0x500	R/W	0x000003FF
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 62. Port Enable Register (Addr: 0x500)

Bit	Name	Description	Type[1]	Default
Register Description: A control register for each port in IXF1010. Port ID = bit position in the register. To make a port active, the bit must be set High (for example, port 4 active implies register value = 0001.0000). Setting the bit to 0 de-asserts the reset. The default state for this register is for all 10 ports to be active.				0x000003FF
31:10	Reserved	Reserved	RO	0x00000
9	Port 9 Enable	Port 9 0 = Disable 1 = Enable	R/W	1
8	Port 8 Enable	Port 8 0 = Disable 1 = Enable	R/W	1
7	Port 7 Enable	Port 7 0 = Disable 1 = Enable	R/W	1
6	Port 6 Enable	Port 6 0 = Disable 1 = Enable	R/W	1
5	Port 5 Enable	Port 5 0 = Disable 1 = Enable	R/W	1
4	Port 4 Enable	Port 4 0 = Disable 1 = Enable	R/W	1
3	Port 3 Enable	Port 3 0 = Disable 1 = Enable	R/W	1
2	Port 2 Enable	Port 2 0 = Disable 1 = Enable	R/W	1
1	Port 1 Enable	Port 1 0 = Disable 1 = Enable	R/W	1
0	Port 0 Enable	Port 0 0 = Disable 1 = Enable	R/W	1

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 63. Link LED Enable Register (Addr: 0x502)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port bit should be set upon detection of link to enable proper operation of the link LEDs.				0x00000000
31:10	Reserved	Reserved	RO	0x00000
9	Link LED Enable Port 9	Port 9 link 0 = No link 1 = Link	R/W	0
8	Link LED Enable Port 8	Port 8 link 0 = No link 1 = Link	R/W	0
7	Link LED Enable Port 7	Port 7 link 0 = No link 1 = Link	R/W	0
6	Link LED Enable Port 6	Port 6 link 0 = No link 1 = Link	R/W	0
5	Link LED Enable Port 5	Port 5 link 0 = No link 1 = Link	R/W	0
4	Link LED Enable Port 4	Port 4 link 0 = No link 1 = Link	R/W	0
3	Link LED Enable Port 3	Port 3 link 0 = No link 1 = Link	R/W	0
2	Link LED Enable Port 2	Port 2 link 0 = No link 1 = Link	R/W	0
1	Link LED Enable Port 1	Port 1 link 0 = No link 1 = Link	R/W	0
0	Link LED Enable Port 0	Port 0 link 0 = No link 1 = Link	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 64. MAC Soft Reset Register (Addr: 0x505)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port software activated reset of the MAC core.				0x00000000
31:10	Reserved	Reserved	RO	0x00000
9	MAC Soft Reset Port 9	Port 9 0 = Disable 1 = Enable	R/W	0
8	MAC Soft Reset Port 8	Port 8 0 = Disable 1 = Enable	R/W	0
7	MAC Soft Reset Port 7	Port 7 0 = Disable 1 = Enable	R/W	0
6	MAC Soft Reset Port 6	Port 6 0 = Disable 1 = Enable	R/W	0
5	MAC Soft Reset Port 5	Port 5 0 = Disable 1 = Enable	R/W	0
4	MAC Soft Reset Port 4	Port 4 0 = Disable 1 = Enable	R/W	0
3	MAC Soft Reset Port 3	Port 3 0 = Disable 1 = Enable	R/W	0
2	MAC Soft Reset Port 2	Port 2 0 = Disable 1 = Enable	R/W	0
1	MAC Soft Reset Port 1	Port 1 0 = Disable 1 = Enable	R/W	0
0	MAC Soft Reset Port 0	Port 0 0 = Disable 1 = Enable	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 65. MDIO Soft Reset Register (Addr: 0x506)

Bit	Name	Description	Type[1]	Default
31:1	Reserved	Reserved	RO	0x00000000
0	MDIO Soft Reset	0 = Reset inactive 1 = Reset active	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 66. Pause Behavior Register (Addr: 0x507)

Bit	Name	Description	Type[1]	Default
Register Description: Provides control on how Pause frames are handled				0x00000000
31:26	Reserved	Reserved	RO	0000000
25:16	Pause Packet Forward	Pause Packet Forward. These 10 bits are set on a per-port basis to allow any Pause packets received to be forwarded to the switch fabric. If the port bit is set, the pause packet is forwarded to the switch fabric. Each bit represents a port with a Logic 1, implying that the pause packet should be forwarded. For example, if the user wants to forward pause packets on port 5, the binary value is written 0000100000.	R/W	0000000000
15:10	Reserved	Reserved	RO	000000
9:0	Pause Packet Corruption	Pause Packet Corruption. These 10 bits are set on a per-port basis to allow any Pause packets received to be corrupted (by modifying the FCS) prior to being forwarded to the switch fabric. If the bit is not set, the pause packet is forwarded without corruption. Each bit represents a port with a Logic 1, implying that the pause packet should be corrupted. For example, if the user wants only to corrupt pause packets on port 5, the binary value is written 0000100000.	R/W	0000000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 67. CPU Interface Register (Addr: 0x508)

Bit	Name	Description	Type[1]	Default
Register Description: CPU interface Endian select. This register allows the user to select the Endian of the CPU interface to allow various different CPUs to be connected to IXF1010.				0x00000000
31:1	Reserved	Reserved	RO	0x00000000
0	Endian	0 = Little Endian 1 = Big Endian	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 68. LED Control Register (Addr: 0x509)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the LED mode				0x00000000
1	LED Enable	0 = Disable LEDs 1 = Enable LEDs	R/W	0
0	LED Control	0 = Enable LED Mode 0 for use with SGS Thomson M5450 LED driver (Default) 1 = LED Mode 1 for use with Standard Octal Shift Register	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 69. LED Flash Rate Register (Addr: 0x50A)

Bit	Name	Description	Type[1]	Default
31:2	Reserved	Reserved	RO	0x00000000
1:0	LED Flash Rate	00 = 100 ms flash rate 01 = 250 ms flash rate 10 = 500 ms flash rate 11 = Reserved	R/W	00

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 70. LED Fault Disable Register Bit Definition (Addr: 0x50B)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port fault disable: Disables the LED flashing for local or remote faults				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	LED Fault Disable Port 9	Port 9 0 = Fault enabled 1 = Fault disabled	R/W	0
8	LED Fault Disable Port 8	Port 8 0 = Fault enabled 1 = Fault disabled	R/W	0
7	LED Fault Disable Port 7	Port 7 0 = Fault enabled 1 = Fault disabled	R/W	0
6	LED Fault Disable Port 6	Port 6 0 = Fault enabled 1 = Fault disabled	R/W	0
5	LED Fault Disable Port 5	Port 5 0 = Fault enabled 1 = Fault disabled	R/W	0
4	LED Fault Disable Port 4	Port 4 0 = Fault enabled 1 = Fault disabled	R/W	0
3	LED Fault Disable Port 3	Port 3 0 = Fault enabled 1 = Fault disabled	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 70. LED Fault Disable Register Bit Definition (Addr: 0x50B) (Continued)

Bit	Name	Description	Type[1]	Default
2	LED Fault Disable Port 2	Port 2 0 = Fault enabled 1 = Fault disabled	R/W	0
1	LED Fault Disable Port 1	Port 1 0 = Fault enabled 1 = Fault disabled	R/W	0
0	LED Fault Disable Port 0	Port 0 0 = Fault enabled 1 = Fault disabled	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.5 Global RX Block Register Overview

Table 71 through Table 75 on page 100 provide an overview of the RX Block Registers, which include the RX FIFO High and Low watermarks.

Table 71. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 0	High watermark for RX FIFO port 0. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x580	R/W	0x00000740
RX FIFO High Watermark Port 1	High watermark for RX FIFO port 1. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x581	R/W	0x00000740
RX FIFO High Watermark Port 2	High watermark for RX FIFO port 2. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x582	R/W	0x00000740
RX FIFO High Watermark Port 3	High watermark for RX FIFO port 3. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x583	R/W	0x00000740
RX FIFO High Watermark Port 4	High watermark for RX FIFO port 4. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x584	R/W	0x00000740
RX FIFO High Watermark Port 5	High watermark for RX FIFO port 5. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x585	R/W	0x00000740
RX FIFO High Watermark Port 6	High watermark for RX FIFO port 6. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x586	R/W	0x00000740

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
Bits 31:15 - Reserved and RO.
Bits 14:0 - Described above.

Table 71. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589) (Continued)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 7	High watermark for RX FIFO port 7. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x587	R/W	0x00000740
RX FIFO High Watermark Port 8	High watermark for RX FIFO port 8. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC	0x588	R/W	0x00000740
RX FIFO High Watermark Port 9	High watermark for RX FIFO port 9. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x589	R/W	0x00000740

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 72. RXFIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 0	Low watermark for RX FIFO port 0. The default value is 1840 bytes. When the port is in flow control, and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58A	R/W	0x00000730
RX FIFO Low Watermark Port 1	Low watermark for RX FIFO port 1. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58B	R/W	0x00000730
RX FIFO Low Watermark Port 2	Low watermark for RX FIFO port 2. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58C	R/W	0x00000730
RX FIFO Low Watermark Port 3	Low watermark for RX FIFO port 3. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58D	R/W	0x00000730
RX FIFO Low Watermark Port 4	Low watermark for RX FIFO port 4. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58E	R/W	0x00000730

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 72. RXFIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593) (Continued)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 5	Low watermark for RX FIFO port 5. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58F	R/W	0x00000730
RX FIFO Low Watermark Port 6	Low watermark for RX FIFO port 6. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x590	R/W	0x00000730
RX FIFO Low Watermark Port 7	Low watermark for RX FIFO port 7. The default value is 1840 bytes.When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x591	R/W	0x00000730
RX FIFO Low Watermark Port 8	Low watermark for RX FIFO port 8. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x592	R/W	0x00000730
RX FIFO Low Watermark Port 9	Low watermark for RX FIFO port 9. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x593	R/W	0x00000730

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 73. Number of Frames Removed on Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name[2]	Description	Address	Type[1]	Default
Number of Frames Removed on Port 0	If the RX FIFO on port 0 becomes full, the number of frames lost/removed on this port are shown in this register.	0x594	RR	0x00000000
Number of Frames Removed on Port 1	If the RX FIFO on port 1 becomes full, the number of frames lost/removed on this port are shown in this register.	0x595	RR	0x00000000
Number of Frames Removed on Port 2	If the RX FIFO on port 2 becomes full, the number of frames lost/removed on this port are shown in this register.	0x596	RR	0x00000000
Number of Frames Removed on Port 3	If the RX FIFO on port 3 becomes full, the number of frames lost/removed on this port are shown in this register.	0x597	RR	0x00000000
Number of Frames Removed on Port 4	If the RX FIFO on port 4 becomes full, the number of frames lost/removed on this port are shown in this register.	0x598	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and RO.
   Bits 21:0 - Described above.

Table 73. Number of Frames Removed on Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name[2]	Description	Address	Type[1]	Default
Number of Frames Removed on Port 5	If the RX FIFO on port 5 becomes full, the number of frames lost/removed on this port are shown in this register.	0x599	RR	0x00000000
Number of Frames Removed on Port 6	If the RX FIFO on port 6 becomes full, the number of frames lost/removed on this port are shown in this register.	0x59A	RR	0x00000000
Number of Frames Removed on Port 7	If the RX FIFO on port 7 becomes full, the number of frames lost/removed on this port are shown in this register.	0x59B	RR	0x00000000
Number of Frames Removed on Port 8	If the RX FIFO on port 8 becomes full, the number of frames lost/removed on this port are shown in this register.	0x59C	RR	0x00000000
Number of Frames Removed on Port 9	If the RX FIFO on port 9 becomes full, the number of frames lost/removed on this port are shown in this register.	0x59D	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and RO.
   Bits 21:0 - Described above.

Table 74. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in conjunction with the MAC filter bits to select whether errored or filtered frames are to be dropped.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 9: 0 = Do not drop frames 1 = Drop frames	R/W	0
8	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 8: 0 = Do not drop frames 1 = Drop frames	R/W	0
7	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 7: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 74. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F) (Continued)

Bit	Name	Description	Type[1]	Default
6	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 6: 0 = Do not drop frames 1 = Drop frames	R/W	0
5	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 5: 0 = Do not drop frames 1 = Drop frames	R/W	0
4	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 4: 0 = Do not drop frames 1 = Drop frames	R/W	0
3	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 3: 0 = Do not drop frames 1 = Drop frames	R/W	0
2	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 2: 0 = Do not drop frames 1 = Drop frames	R/W	0
1	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 1: 0 = Do not drop frames 1 = Drop frames	R/W	0
0	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the Mac Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 0: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 75. RX FIFO Overflow Event Register (Addr: 0x5A0)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a status if a FIFO-full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	RX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	RX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
6	RX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	RX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	RX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	RX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	RX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	RX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	RX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1. R = Read Only Clear on Read; W = Write only; R/W = Read/Write				

6.5.6 TX Block Register Overview

Table 76 through Table 81 on page 109 provide an overview of the TX Block Registers, which include the TX FIFO High and Low watermark.

Table 76. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 0	High watermark for TX FIFO port 0. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x600	R/W	0x00000630
TX FIFO High Watermark Port 1	High watermark for TX FIFO port 1. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x601	R/W	0x00000630
TX FIFO High Watermark Port 2	High watermark for TX FIFO port 2. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x602	R/W	0x00000630
TX FIFO High Watermark Port 3	High watermark for TX FIFO port 3. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x603	R/W	0x00000630
TX FIFO High Watermark Port 4	High watermark for TX FIFO port 4. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x604	R/W	0x00000630
TX FIFO High Watermark Port 5	High watermark for TX FIFO port 5. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x605	R/W	0x00000630
TX FIFO High Watermark Port 6	High watermark for TX FIFO port 6. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x606	R/W	0x00000630

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 76. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609) (Continued)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 7	High watermark for TX FIFO port 7. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x607	R/W	0x00000630
TX FIFO High Watermark Port 8	High watermark for TX FIFO port 8. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x608	R/W	0x00000630
TX FIFO High Watermark Port 9	High watermark for TX FIFO port 9. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x609	R/W	0x00000630

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 77. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 0	Low watermark for TX FIFO port 0. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60A	R/W	0x000001D0
TX FIFO Low Watermark Port 1	Low watermark for TX FIFO port 1. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60B	R/W	0x000001D0
TX FIFO Low Watermark Port 2	Low watermark for TX FIFO port 2. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60C	R/W	0x000001D0
TX FIFO Low Watermark Port 3	Low watermark for TX FIFO port 3. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60D	R/W	0x000001D0

1. R = Read Only Clear on Read; W = Write only; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 77. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613) (Continued)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 4	Low watermark for TX FIFO port 4. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60E	R/W	0x000001D0
TX FIFO Low Watermark Port 5	Low watermark for TX FIFO port 5. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60F	R/W	0x000001D0
TX FIFO Low Watermark Port 6	Low watermark for TX FIFO port 6. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x610	R/W	0x000001D0
TX FIFO Low Watermark Port 7	Low watermark for TX FIFO port 7. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x611	R/W	0x000001D0
TX FIFO Low Watermark Port 8	Low watermark for TX FIFO port 8. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x612	R/W	0x000001D0
TX FIFO Low Watermark Port 9	Low watermark for TX FIFO port 9. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x613	R/W	0x000001D0

1. R = Read Only Clear on Read; W = Write only; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 78. MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D)

Name[2]	Description[3]	Address	Type[1]	Default
MAC Transfer Threshold Port 0	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x614	R/W	0x00000040
MAC Transfer Threshold Port 1	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x615	R/W	0x00000040
MAC Transfer Threshold Port 2	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x616	R/W	0x00000040
MAC Transfer Threshold Port 3	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x617	R/W	0x00000040

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1010, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 78. MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name[2]	Description[3]	Address	Type[1]	Default
MAC Transfer Threshold Port 4	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x618	R/W	0x00000040
MAC Transfer Threshold Port 5	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x619	R/W	0x00000040
MAC Transfer Threshold Port 6	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61A	R/W	0x00000040
MAC Transfer Threshold Port 7	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61B	R/W	0x00000040

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1010, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

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Table 78. MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name[2]	Description[3]	Address	Type[1]	Default
MAC Transfer Threshold Port 8	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61C	R/W	0x00000040
MAC Transfer Threshold Port 9	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61D	R/W	0x00000040

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1010, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 79. TX FIFO Overflow Event Register (Addr: 0x61E)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides status that a FIFO- full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	TX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	TX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	TX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
6	TX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	TX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	TX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	TX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	TX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	TX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	TX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 80. Info Out-of-Sequence Register (Addr: 0x621)

Bit	Name	Description	Type[1]	Default
Register Description: This register signals when out-of-sequence data is detected in the TX FIFO. Events such as SOP followed by another SOP cause this bit to be set and remain so until read. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	Info Out-of-Sequence Port 9	Port 9 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
8	Info Out-of-Sequence Port 8	Port 8 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
7	Info Out-of-Sequence Port 7	Port 7 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
6	Info Out-of-Sequence Port 6	Port 6 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
5	Info Out-of-Sequence Port 5	Port 5 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
4	Info Out-of-Sequence Port 4	Port 4 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
3	Info Out-of-Sequence Port 3	Port 3 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
2	Info Out-of-Sequence Port 2	Port 2 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1	Info Out-of-Sequence Port 1	Port 1 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
0	Info Out-of-Sequence Port 0	Port 0 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 81. Number of Frames Dropped Ports 0-9 (Addr: 0x622 - 0x62B)

Name	Description	Address	Type[1]	Default
Number of Frames Removed on Port 0	When TX FIFO on port 0 becomes full or reset, the number of frames lost/removed on this port is shown in this register.	0x622	RR	0x00000000
Number of Frames Removed on Port 1	In the case of TX FIFO on port 1 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x623	RR	0x00000000
Number of Frames Removed on Port 2	In the case of TX FIFO on port 2 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x624	RR	0x00000000
Number of Frames Removed on Port 3	In the case of TX FIFO on port 3 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x625	RR	0x00000000
Number of Frames Removed on Port 4	In the case of TX FIFO on port 4 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x626	RR	0x00000000
Number of Frames Removed on Port 5	In the case of TX FIFO on port 5 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x627	RR	0x00000000
Number of Frames Removed on Port 6	In the case of TX FIFO on port 6 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x628	RR	0x00000000
Number of Frames Removed on Port 7	In the case of TX FIFO on port 7 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x629	RR	0x00000000
Number of Frames Removed on Port 8	In the case of TX FIFO on port 8 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x62A	RR	0x00000000
Number of Frames Removed on Port 9	In the case of TX FIFO on port 9 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x62B	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.7 MDIO Block Register Overview

Table 82 through Table 85 on page 111 provide an overview of the MDIO Block Registers.

Table 82. MDI Single Command Register (Addr: 0x680)

Bit	Name	Description	Type[1]	Default
Register Description: Provides the CPU with the ability to perform single MDIO Read and Write access				0x00000000
31:21	Reserved	Reserved	RO	0000000000 0
20	MDI Command	Performs an MDIO access. When set, this bit self clears upon completion of the access. 1 = Performs an MDIO access 0 = MDIO access completed	R/W	0
19:18	Reserved	Reserved	RO	00
17:16	OP Code	MDIO Op Code 00 = Reserved 01 = Write Access 10 = Read Access 11 = Reserved	R/W	01
15:13	Reserved	Reserved	RO	000
12:8	PHY Address	Address of external PHY device	R/W	00000
7:5	Reserved	Reserved	RO	000
4:0	REG Address	Address of register within external PHY	R/W	00000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 83. MDI Single Read and Write Data Register (Addr: 0x681)

Bit	Name	Description	Type[1]	Default
Register Description: Allows for MDIO Read/Write capability.				0x00000000
31:16	MDI Read Data	Read Data from external device	RO	0x0000
15: 0	MDI Write Data	Write data for MDI Writes to the external device.	R/W	0x0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 84. Autoscan PHY Address Enable Register (Addr: 0x682)

Bit	Name	Description	Address	Type[1]	Default
31:0	Autoscan PHY Address Enable	Defines valid PHY addresses Each bit enables the corresponding PHY address for autoscan operation: 1 = Enable this PHY Address 0 = Disable this PHY Address	0x682	R/W	0x000003FF
1.	1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 85. MDI Control Register (Addr: 0x683)

Bit	Name	Description	Type[1]	Default
31:4	Reserved	Set to 0000000 Hex during Write operation (Default = 0000000 Hex)	R/W	0x00000000
3	MDIO in Prog	Status of MDIO single transaction 1 = MDIO single command in progress 0 = MDIO single command not in progress (Default)	R/W	0
2	MDIO in Prog Enable	Enable the MDIO IN PROG Register bit 1 = MDIO IN PROG Register bit enabled 0 = MDIO IN PROG Register bit disabled (Default)	R/W	0
1	Autoscan Enable	Enable continuous Autoscan operation 1 = Autoscan enabled 0 = Autoscan disabled (default)	R/W	0
0	MDC Speed	Selects speed of MDC clock 1 = MDC runs at 17.8 MHz 0 = MDC runs at 2.5 MHz	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

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6.5.8 SPI4-2 Block Register Overview

Table 86 through Table 89 on page 113 provide an overview of the SPI4-2 Block Registers.

Table 86. SPI4-2 RX Burst Size Register (Addr: 0x700)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for burst size.				0x00060002
31	no_idles	Additional Idles are inserted between payloads when set. During default operation, only a single control word is used to signal the end of one frame and the start of another. When this bit is set to 1, idles are inserted between the packets and have individual control words for EOP and SOP.	R/W	0x0
30:25	Reserved	Reserved	RO	0x00
24:16	MaxBurst1	Maximum number of 16-byte blocks that the FIFO in the receive path, external to IXF1010, can accept when the FIFO Status channel indicates STARVING	R/W	0x006
15:9	Reserved	Reserved	RO	0x00
8:0	MaxBurst2	Maximum number of 16-byte blocks that the FIFO in the receive path, external to IXF1010, can accept when the FIFO Status channel indicates HUNGRY	R/W	0x002

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 87. SPI4-2 RX Training Register (Addr: 0x701)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for training sequences				0x00000000
31:24	Reserved	Reserved	RO	0x00
23:16	REP_T	Number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles	R/W	0x00
15:0	DATA_MAX_T[2]	Maximum interval (in number of cycles) between scheduling of training sequences on receive data path interface An all zero value disables training sequences.	R/W	0x0000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. The value of DATA_MAX_T is the Most Significant 16 bits of a 24-bit counter value. The Least Significant 8 bits are always 0x00. This allows for a much larger DAT_MAX_T time-out period and provides a more than adequate granularity of selection.

Table 88. SPI4-2 RX Calendar Register (Addr: 0x702)

Bit	Name	Description	Type[1]	Default Value
Register Description: SPI4-2 RX interface start-up parameters for FIFO status calendar operation.				0x00010300
31:30	RX Train Test Modes	00 = Normal mode. 01 = Do not enter training based on a repeating "11" pattern on RSTAT 1x = Train continuously	R/W	0x0
29	RSCLK_invert	When this bit = 0, the FIFO status is captured on the rising edge of the RSCLK as per the SPI4-2 specification. When this bit = 1, the FIFO status is captured on the falling edge of RSCLK	R/W	0
28	TSCLK_invert	When this bit = 0, the FIFO status is launched on the rising edge of the TSCLK as per the SPI4-2 specification. When this bit = 0, the FIFO status is launched on the falling edge of TSCLK	R/W	0
27:21	Reserved	Reserved	RO	0x000
20	DIP2_Error	Set based on an incorrect RX DIP2 result. This bit is cleared upon a read	RR	0x0
19:16	DIP-2_Thr	Defines how many consecutive correct DIP-2s are required to disable sending of training sequences.	R/W	0x1
15:12	Reserved	Reserved	RO	0x0
11:8	Loss_of_Sync	Number of consecutive calendar framing cycles required to invoke sending of training sequences.	R/W	0x3
7:4	Reserved	Reserved	RO	0x0
3:0	CAL_M	Number of times FIFO status for ports 0 through 9 repeat between framing and DIP-2 cycles	R/W	0x0
1. R0 = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 89. SPI4-2 TX Synchronization Register (Addr: 0x703)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 synchronization DIP-4 counters.				0x00000045
31:8	Reserved	Reserved	RO	0x0000000
7:4	DIP4_UnLock[2]	Number of consecutive incorrect DIP4 results that cause TSTAT being driven to "11"	R/W	0x4
3:0	DIP4_Lock	Number of consecutive correct DIP4 results to achieve synchronization and end training	R/W	0x5
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. When Periodic Training is enabled, the actual count of DIP4 errors required to lose synchronization is 1 less than the programmed value in this register. Therefore, this value should always be programmed to be 1 more than the desired value and should never be programmed to either 0 or 1.				

6.6 Package Overview

CBGA packages are suited for applications requiring high I/O counts and high electrical performance. They are recommended for high-power applications, having high noise immunity requirements.

6.6.1 Features

- Flip chip die attach; surface mount second-level interconnect
- High electrical performance
- High I/O counts
- Area array I/O options
- Multiple power zone offering supports core and four additional voltages
- JEDEC-compliant package

6.6.2 Package Specifics for IXF1010

IXF1010 uses the following packaging (see Figure 33, “IXF1010 552-Ceramic Ball Grid Array (CBGA) Package Specification” on page 115):

- 552-ball CBGA
- Ball pitch of 1.0 mm
- Overall package dimensions of 25 mm x 25 mm

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Figure 33. IXF1010 552-Ceramic Ball Grid Array (CBGA) Package Specification