EPSON

SPC8106F0C

Low Power LCD & CRT VGA Controller

■ DESCRIPTION

The SPC8106F0C is a 3.3/5 V LCD video controller based on VGA architecture and optimized for driving a 640×480 LCD panel display. VGA standard mode functionality is supported using standard IBM VGA parameters. A proprietary 256×6 bit gray scale lookup table is provided to allow remapping of the 64 possible gray shades displayed on a monochrome LCD panel. For color LCD modes, an internal 256×12 bit VGA-style lookup table is provided (4 bits each of R, G, and B). An interface to an external RAMDAC is also provided to allow connecting a standard VGA monitor to the system.

The target markets for this device are small, cost sensitive 5V sub-notebook computers, or other specialized consumer products where low cost, low power consumption, low component count, and the ability to run most VGA software on a 640×480 LCD panel display are the major design considerations. This chip is intended to operate mainly in planar graphics modes (e.g. mode 12H), and will display 16 levels of gray, or 64 levels of gray in mode 13h on a monochrome LCD display, or up to 256 colors out of a palette of 4096 colors on a color LCD display. With an external RAMDAC, standard VGA modes are supported on a CRT display.

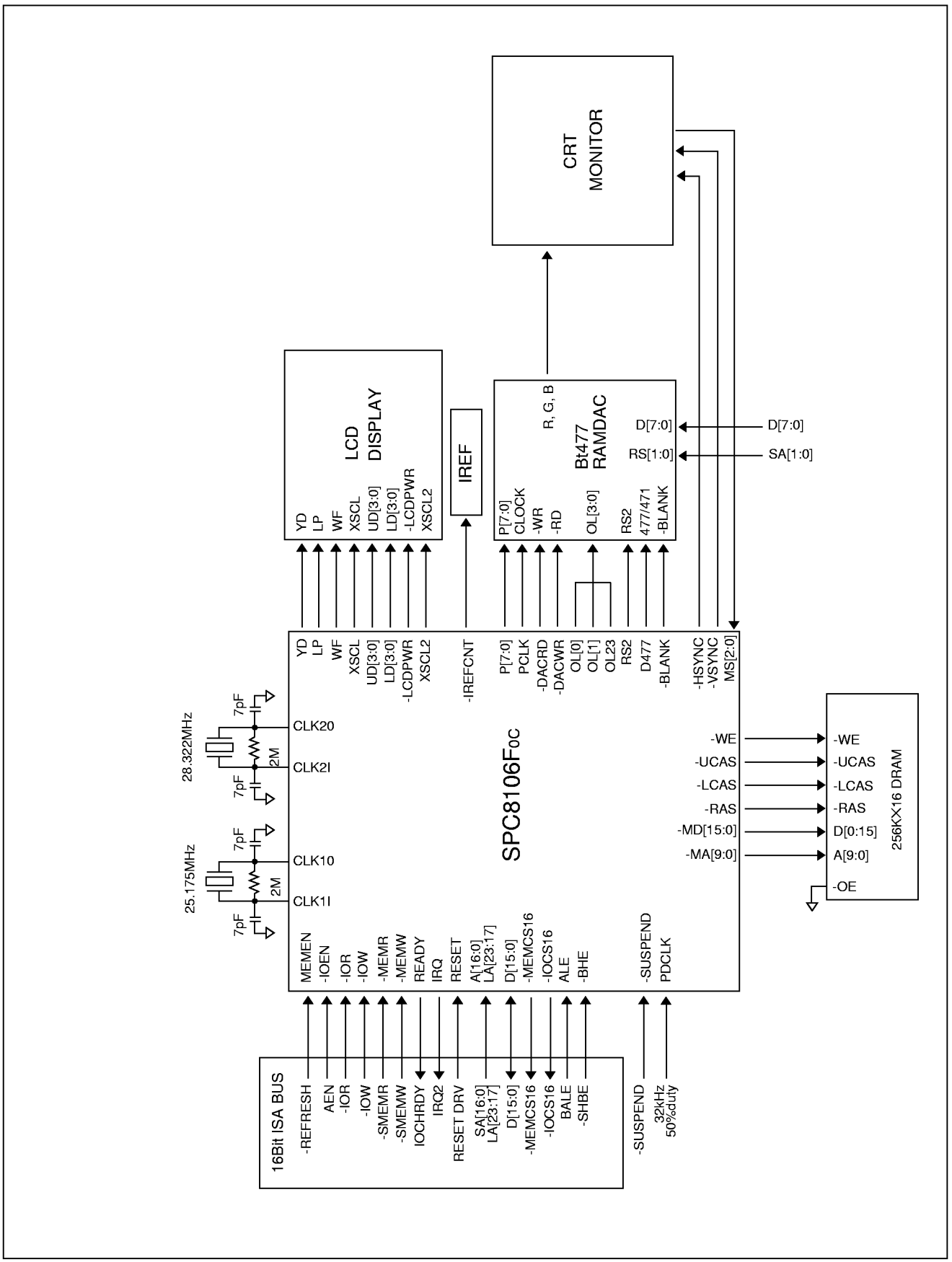
■ FEATURES

- Low-power CMOS technology
- Hardware VGA compatible
- High performance 16-bit ISA support
- One 256K×16 self-refresh DRAM
- 64×64 pixel hardware cursor
- Two-terminal crystals support
- Six power-down modes
- Video BIOS, software driver and utility support
- 3.3 and 5 volt operation
- Monochrome/color LCD panel interface, for sizes 320×200 to 640×480
- On-chip 256×6 gray-scale look-up table
- On-chip 256×12 color look-up table
- 64 gray shades by frame rate modulation and dithering
- 16 gray shades by frame rate modulation
- 3C3h and 46E8h video enable registers supported
- Vertical centering and expansion for LCDs
- Full CRT support with ÅA7 RAMDAC
- Package: QFP 17-144pin(plastic)

■ SUPPORTED LCD PANELS

8-bit Interface				4-bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	400 480	320 480 640	200 240 320 400 480

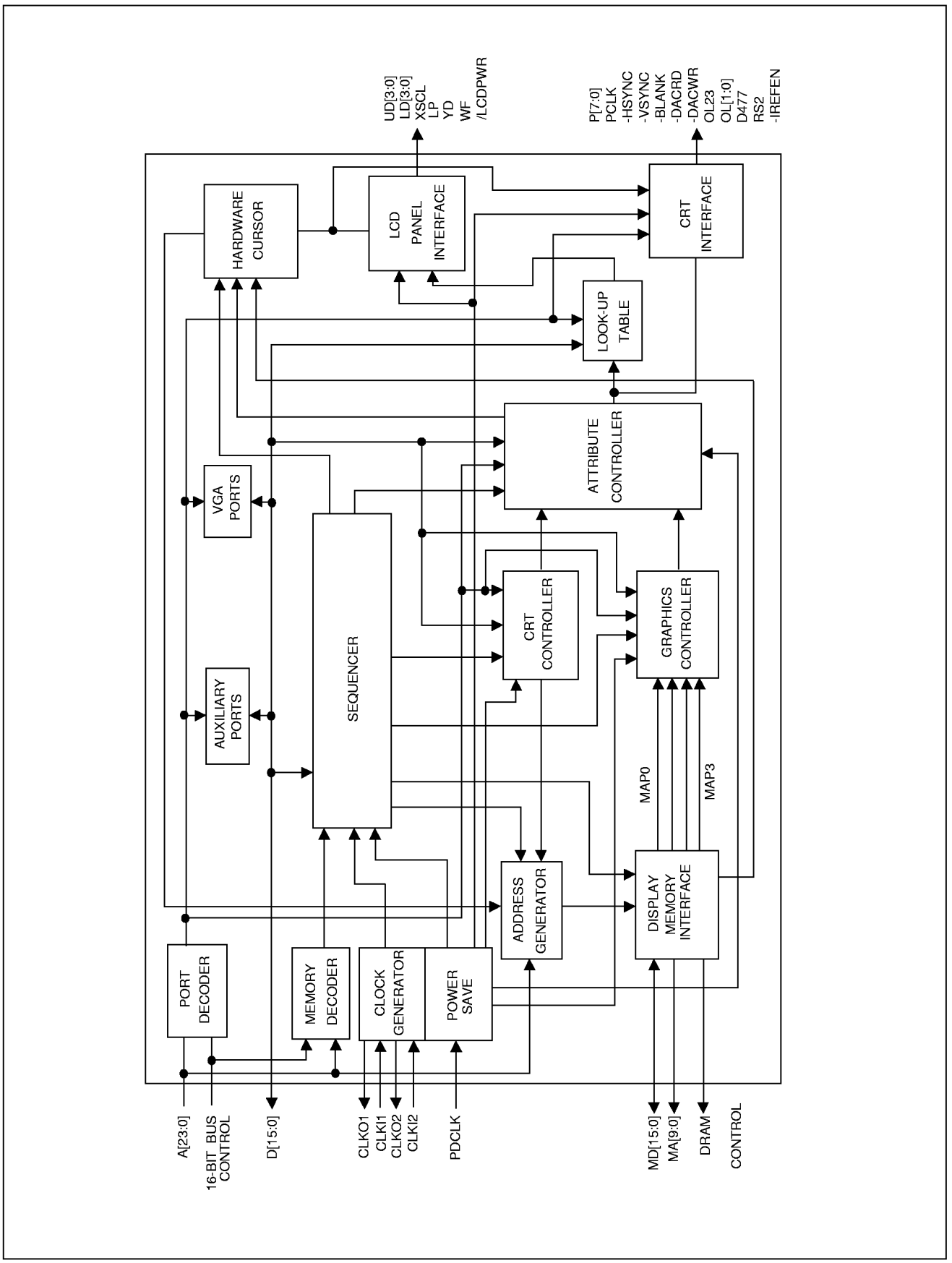
■ BLOCK DIAGRAM



■ SPC8106 LCD Display Modes

Mode No.	Mode Type	Font	Characters	Resolution	Displayd Pixels	Gray Shades	Colors	Memory Segment	Double-scan
0	Text	8×8	40×25	320×200	640×400	16	16	B800	No
0+	Text	8×14	40×25	320×350	640×350	16	16	B800	No
0++	Text	8×16	40×25	320×400	640×400	16	16	B800	No
1	Text	8×8	40×25	320×200	640×400	16	16	B800	No
1+	Text	8×14	40×25	320×350	640×350	16	16	B800	No
1++	Text	8×16	40×25	320×400	640×400	16	16	B800	No
2	Text	8×8	80×25	640×200	640×400	16	16	B800	No
2+	Text	8×14	80×25	640×350	640×350	16	16	B800	No
2++	Text	8×16	80×25	640×400	640×400	16	16	B800	No
3	Text	8×8	80×25	640×200	640×400	16	16	B800	No
3+	Text	8×14	80×25	640×350	640×350	16	16	B800	No
3++	Text	8×16	80×25	640×400	640×400	16	16	B800	No
4	Graphics	N/A	N/A	320×200	640×400	4	4	B800	No
5	Graphics	N/A	N/A	320×200	640×400	4	4	B800	No
6	Graphics	N/A	N/A	640×200	640×400	2	2	B800	No
7	Text	8×14	80×25	640×350	640×350	2	2	B000	No
7+	Text	8×16	80×25	640×400	640×400	2	2	B000	No
0D	Graphics	N/A	N/A	320×200	640×400	16	16	A000	No
0E	Graphics	N/A	N/A	640×200	640×400	16	16	A000	No
0F	Graphics	N/A	N/A	640×350	640×350	2	2	A000	No
10	Graphics	N/A	N/A	640×350	640×350	16	16	A000	No
11	Graphics	N/A	N/A	640×480	640×480	2	2	A000	Yes
12	Graphics	N/A	N/A	640×480	640×480	16	16	A000	Yes
13	Graphics	N/A	N/A	320×200	640×400	64	256	A000	No
100	Graphics	N/A	N/A	640×400	640×400	64	256	A000	No
101	Graphics	N/A	N/A	640×480	640×480	64	256	A000	Yes
108	Text	8×8	80×60	640×480	640×480	16	16	B800	Yes

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

● The Sequencer

The Sequencer generates internal signals to synchronize the operation of the chip as well as the signals to control the timing of the display DRAM. The Sequencer also arbitrates between CPU and video display accesses to the DRAM. It contains registers that allow selection of character font set, control the structure of the video memory and allow write masking of the individual plane of memory.

● CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the CRT, single panel or dual panel LCD display and character and/or pixel addresses for display data from DRAM.

● CRT Interface

The CRT Interface aligns CRT signals to the Pixel Clock and generates the I/O Control signals for CPU access to the RAMDAC.

● Address Generator

The Address Generator takes the display and refresh addresses from the CRT Controller and converts them into RAS and CAS addresses for the display DRAM and multiplexes these display accesses with CPU memory accesses.

● Attributes Controller

The Attributes Controller takes in pixel and attribute information from the Graphics Controller and display DRAM and formats the data into pixel information which then passes through the lookup table. It also controls display character attributes such as blink, underline and horizontal pixel panning.

● Graphics Controller

The Graphics Controller supplies display memory data to the Attributes Controller during display time and provides data translation between the CPU bus and the display memory during CPU read or write access cycles.

● Memory Decoder

The Memory Decoder monitors the CPU-bus activity and decodes cycles for the display DRAM. It supplies memory access control signals to the Sequencer.

● Port Decoder

The Port Decoder decodes CPU-bus I/O cycles to provide enable and write strobes for the on-chip I/O registers.

● Auxiliary Ports

The Auxiliary Ports are I/O registers used to control functions of the chip beyond the basic VGA register set. Registers are included for controlling the LCD interface circuits as well as the power save modes.

● VGA Ports

The VGA Ports contain the Miscellaneous Output Status register and the Video Subsystem Enable register used in VGA mode.

● Clock Generation

The Clock Generation contains oscillator support for an external crystal.

● Power Save

The Power Save block contains the logic to implement four software controlled and one hardware controlled power down modes.

● Lookup Table

The Lookup Table consists of a memory array of 256 locations of 6 bits each and hardware to convert VGA palette writes to gray-scale values.5

● LCD Interface

The LCD Interface block converts the display video data from the Lookup Table into LCD display data, It also generates control signals necessary to drive single or dual-panel LCD panels. The LCD interface block generates 16 levels of gray shades through frame rate modulation techniques and 64 levels of gray shades with additional dithering techniques.

● Hardware Cursor

The Hardware Cursor block generates a 64×64×4 grey shade cursor or sprite that can be overlayed on the current displayed image.

■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage	Vss-0.3 to +7.0	V
V_{IN}	Input Voltage	Vss-0.3 to V_{DD}+0.3	V
V_{OUT}	Output Voltage	Vss-0.3 to V_{DD}+0.3	V
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOL}	Soldering Temperature / Time	260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
HV_{DD}	Supply Voltage	V_{SS}=0V	4.5	5.0	5.5	V
LV_{DD}	Supply Voltage	V_{SS}=0V	3.0	3.3	3.6	V
V_{IN}	Input Voltage	V_{SS}	V_{SS}	-	V_{DD}	V
V_{OPR}	Operating Temperature		0	25	70	°C

● Input Specifications

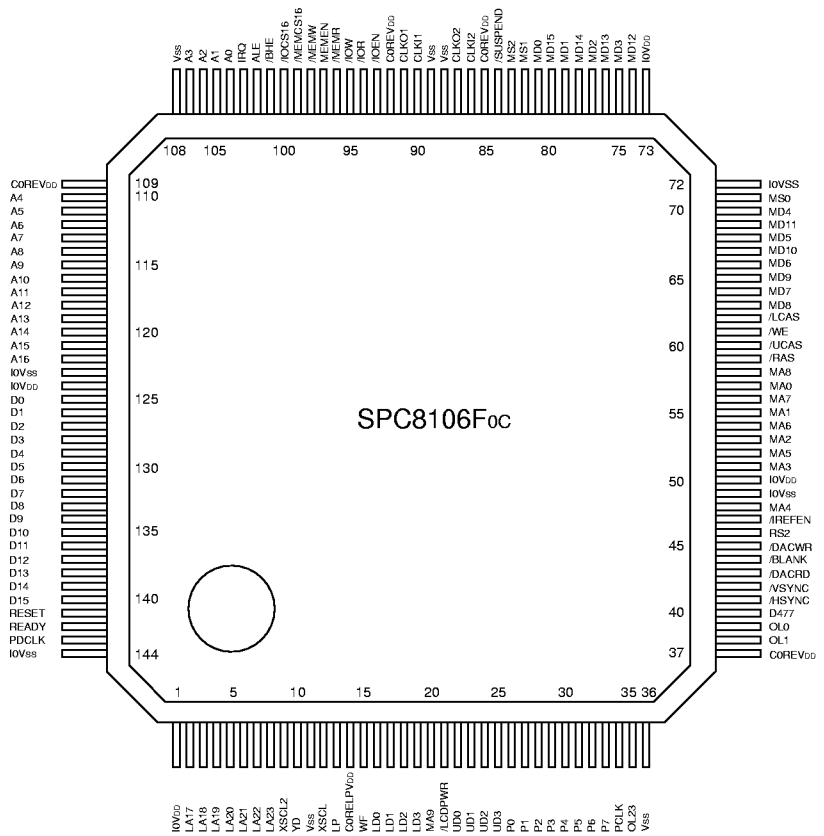
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage(CMOS Inputs)	V_{DD}=Min			1.0	V
V_{IH}	High Level Input Voltage(CMOS Inputs)	V_{DD}=Max	3.5			V
V_{IL}	Low Level Input Voltage(TTL Inputs)	V_{DD}=Min			0.8	V
V_{IH}	High Level Input Voltage(TTL Inputs)	V_{DD}=Max	2.0			V
V_{T+}	Positive-going Threshold(CMOS Schmitt inputs)	V_{DD}=5.0			4.0	V
V_{T-}	Negative-going Threshold(CMOS Schmitt inputs)	V_{DD}=5.0	0.8			V
V_H	Hysteresis Voltage(CMOS Schmitt inputs)	V_{DD}=5.0	0.3			V
V_{T+}	Positive-going Threshold(TTL Schmitt inputs)	V_{DD}=5.0			3.0	V
V_{T-}	Negative-going Threshold(TTL Schmitt inputs)	V_{DD}=5.0	0.6			V
V_H	Hysteresis Voltage(TTL Schmitt inputs)	V_{DD}=5.0	0.1			V
I_{IZ}	Input Leakage Current	V_{DD}=Max V_{IH}=V_{DD} V_{IL}=V_{SS}	-1		1	µA
C_{IN}	Input Pin Capacitance			8		pF
R_{PU2}	Pull Up Resistance	V_{DD}=5.0V	50	100	200	kΩ
R_{PU3}	Pull Up Resistance	V_{DD}=5.0V	100	200	400	kΩ
R_{PD}	Pull Down Resistance	V_{DD}=5.0V	100	200	400	kΩ

● Output Specifications

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
I_{OL2}	Low Level Output Current	$V_{OL}=V_{SS}+0.4V$ TS2	-6.0			mA
I_{OH2}	High Level Output Current	$V_{OH}=V_{DD}-0.4V$ TS2	-2.0			mA
I_{OL3}	Low Level Output Current	$V_{OL}=V_{SS}+0.4V$ TS3	12.0			mA
I_{OH3}	High Level Output Current	$V_{OH}=V_{DD}-0.4V$ TS3	-4.0			mA
I_{OL4}	Low Level Output Current	$V_{OL}=V_{SS}+0.4V$ TS4	24.0			mA
I_{OH4}	High Level Output Current	$V_{OH}=V_{DD}-0.4V$ TS4	-8.0			mA
I_{OZ}	Output Leakage Current	$V_{OH}=V_{DD}$ or $V_{OL}=V_{SS}$	-1		1	µA
C_{OUT}	Output Pin Capacitance			8		pF
C_{BID}	Bidirectional Pin Capacitance			10		pF

■ PIN CONFIGUTATION

QFP17-144pin



■ PIN DESCRIPTION

● Key

C =CMOS level input
TTL =TTL level input
TTLS =TTL level input with hysteresis
TSx =Tri-state CMOS level driver,x denotes driver type-see *D.C. Characteristics* for rating.
TSxUy =Tri-state CMOS level driver with pull up resistor (y=2: 100 kΩ typical., y=3: 200 kΩ typ.), x denotes driver type-see *D.C. Characteristics* for rating.
TSxD =Tri-state CMOS level driver with pull down resistor (200 kΩ typ.), x denotes driver type-see *D.C. Characteristics* for rating.

Note pins marked with a * in the Type column are outputs in normal operation mode, but for pin test mode, these outputs are placed in a high impedance state and these pins become inputs. Therefore these pins are actually bidirectional, although only the normal output mode is shown in this table. For these pins, the input type for this test mode is shown in parentheses (*). See PIN TEST MODE on page 118 for more information.

● CPU Interface

Pin Name	Type	Pin #	Drv	Description
A[0:16] LA[17:23]	I	104..107, 110..122, 2..4, 5..8	TTL	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off. If the value on MD[5] at RESET 1, then the ALE input pin is used to internally latch LA[19:17] and A[16:2], allowing these address bits to be driven by the processor address bus. If the value on MD[5] at RESET 0, then standard ISA address timing is assumed, where pins A[0:16], LA[17:23] should be connected to the ISA bus signals SA[0:16], LA[17:23] respectively.
ALE	I	102	TTL	ISA Bus Address Latch Enable. In Suspend Mode the ALE input is disabled. If the value on MD[5] at RESET = 1, then the ALE input is used to internally latch LA[19:17] and A[16:2], allowing these address bits to be driven by the processor address bus. In this mode, the processor ADS# output should be connected to this pin. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed, and only the LA[19:17] inputs are internally latched.
D[0:15]	I/O	125..140	TTL /TS2	16 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
MEMEN	I	97	TTLS	ISA Bus Memory Enable. This signal should be connected to the REFRESH# signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
IOR#	I	94	TTLS	ISA Bus I/O Read Strobe. In Suspend Mode the IOR# input is disabled.
IOW#	I	95	TTLS	ISA Bus I/O Write Strobe. In Suspend Mode the IOW# input is disabled.
MEMR#	I	96	TTLS	ISA Bus System Memory Read Strobe. In Suspend Mode the MEMR# input is disabled.
MEMW#	I	98	TTLS	ISA Bus System Memory Write Strobe. In Suspend Mode the MEMW# input is disabled.
IOEN#	I	93	TTLS	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode, the IOEN# input is disabled.
READY	O*	142	TS3 (*C)	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	141	TTLS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state.
IRQ	O	103	TS3	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1 (rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated). This pin also is used for the output of the NAND tree in pin test mode.
MEMCS16#	O*	99	TS4 (*C)	ISA Bus Memory Chip Select 16. Address inputs LA[23:17] are decoded to drive this output low when a valid memory address (AXXXXH, BXXXXH) appears on the bus.
IOCS16#	O*	100	TS4 (*C)	ISA Bus I/O Chip Select 16. Address inputs A[15:0] and IOEN# are decoded to drive this output low when a valid SPC8106F0C I/O register address appears on the bus,. Note that I/O addresses 3C6h-3C9h do not result in IOCS16# being driven low (i.e. RAMDAC and internal LUT register reads and writes are 8 bit cycles).
BHE#	I	101	TTL	ISA Bus Byte High Enable. In Suspend Mode the BHE# input is disabled.

● Video Memory Interface

Pin Name	Type	Pin #	Drv	Description
MA[0:9]	O*	57,55,53, 51,48,52, 54,56,58, 20	TS2 (*C)	Multiplexed row ‘column address bits for video display memory.
MD[0:15]	I/O	81,79,77, 75,70,68, 66,64,63, 65,67,69, 74,76,78, 80	TTL/ TS2U2	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] and MD[12:9] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Also, the value on MD[8:4] and MD[15:13] are used to configure various hardware options.
RAS#	O*	59	TS3 (*C)	DRAM Row Address Strobe for single 256K ~16 DRAM.
LCAS# (LWE#)	O*	62	TS3 (*C)	Multiple Function: DRAM Column Address Strobe for low byte (LCAS#).
UCAS# (CAS#)	O*	60	TS3 (*C)	Multiple Function: DRAM Column Address Strobe for high byte (UCAS#).
WE# (UWE#)	O*	61	TS3 (*C)	Multiple Function: DRAM Write Enable Strobe (WE#).

● Clock Inputs

Pin Name	Type	Pin #	Drv	Description
CLKI1	I	90	C	This pin, along with CLKO1 is the 25.175MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. if an external oscillator is used as a clock source, then this pin is the clock input.
CLKO1	O	91	•	This pin, along with CLKI1 is the 25.175MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.
CLKI2	I	86	C	This pin, along with CLKO2 is the 28.322MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. if an external oscillator is used as a clock source, then this pin is the clock input.
CLKO2	O	87	•	This pin, along with CLKI2 is the 28.322MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

● Power Supply

Pin Name	Type	Pin #	Description
$COREV_{DD}$	P	14,37,85,92,109	V_{DD} supply for core logic.
IOV_{DD}	P	1,50,73,124	V_{DD} supply for interface pins.
V_{SS}	P	11,36,88,89,108	V_{SS} supply for core logic.
IOV_{SS}	P	49,72,123,144	V_{SS} supply for interface pins.

● Power Save Mode Control

Pin Name	Type	Pin #	Drv	Description
SUSPEND#	I	84	TTLS	A low level on this pin puts the chip into a hardware power down mode. The SUSPEND# signal overrides any software initiated power down modes, and disables the ISA-Bus interface inputs except RESET. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD(3:0), LD(3:0), XSCL, XSCL2, LP, YD and WF signals are driven into a high impedance or low state (configurable) and the LCDPWR# signal is driven high.
PDCLK	I	143	TTL	Power Down Clock. This input may be used to provide a low frequency clock for generating refresh in Power Save Modes 4 and Suspend, as an optional alternative to using the pixel clock or MEMEN input as the refresh clock source. This clock input should be driven by either by a 32 kHz 50% duty cycle clock source, or a 64 kHz clock source with a high period as short as possible (but > minimum RAS low pulse width) to minimize DRAM current consumption during refresh. The PDCLK input is used to directly generate the RAS and CAS pulses during Power Save Mode 4 and Suspend.

● LCD Panel Interface

Note some of these pins have alternate uses in some display moeds. Pin Mapping for Various Display Modes on page 12

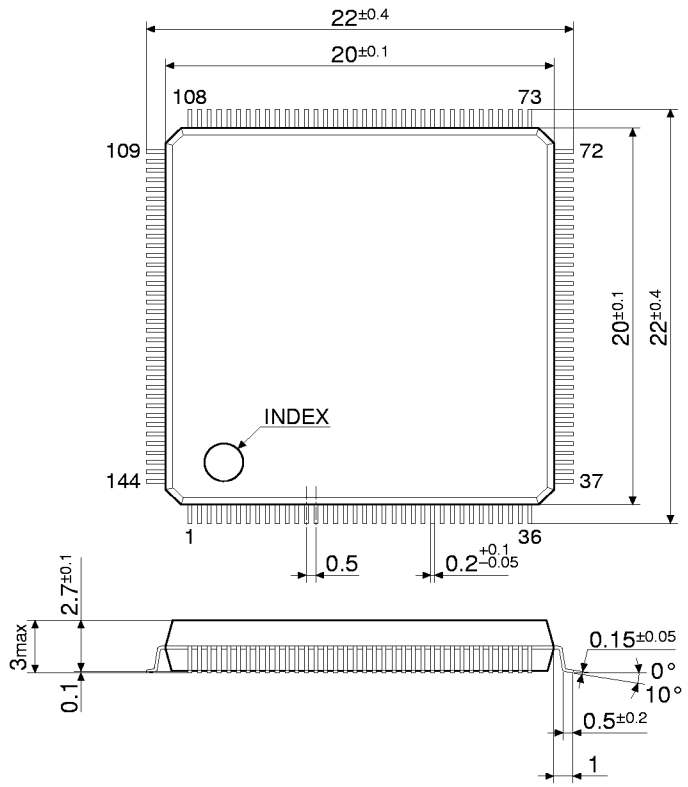
Pin Name	Type	Pin #	Drv	Description
YD	O*	10	TS4 (*C)	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O*	13	TS4 (*C)	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O*	12	TS4 (*C)	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
XSCL2	O*	9	TS4 (*C)	This second shift clock is used together with XSCL in 8-bit single color panel mode to shift in alternate sets of display data. XSCL2 is also used alone as the shift clock in 8-bit dual color panel mode and 4-bit single color panel mode.
UD[0:3]	O*	22..25	TS4 (*C)	Upper panel display data for dual panel-dual drive mode. For 8-bit single panel-single drive mode, these bits are the most significant 4-bits of the 8-bit output data to the panel (data[7:4]). For 4-bit single panel mode, these bits are the 4 bits of data output to the panel. For 16-bit LCD modes, these outputs are the multiplexed upper panel data if MD[7] = 1 at RESET, or the lower nibble of the upper panel data if MD[7] = 0 at RESET.
UD[4:7]	O*	26..29	TS2D (*C)	When MD[7] = 0 at RESET, these pins are the upper nibble of the 16-bit LCD mode upper panel data.
LD[0:3]	O*	16..19	TS4 (*C)	Lower panel display data for dual panel-dual drive mode. For 8-bit single panel-single drive mode, these bits are the least significant 4-bits of the 8-bit output data to the panel (data[3:0]). For 4-bit single panel mode, these outputs are driven low. For 16-bit LCD modes, these outputs are the multiplexed lower panel data if MD[7] = 1 at RESET, or the lower nibble of the lower panel data if MD[7] = 0 at RESET.
UD[4:7]	O*	30..33	TS2D (*TTL)	When MD[7] = 0 at RESET, these pins are the upper nibble of the 16-bit LCD mode lower panel data.
LCDPWR#	O*	21	TS2 (*C)	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, when Auxiliary Register 06 bit 0 is set to 1, or when the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF	O*	15	TS4D (*C)	LCD Backplane Bias signal. This output toggles once every n LP periods, as programmed in Auxiliary Register[0D].

● External CRT/RAMDAC Interface

Pin Name	Type	Pin #	Drv	Description
P[0:7]	O*	26..33	TS2D (*TTL)	When MD[7] = 1 at RESET, these pins are the Pixel Data outputs. These 8 bits are connected to the pixel select inputs of the external RAMDAC.
PCLK	O*	34	TS2D (*C)	Pixel Clock. Pixel data is clocked out of the chip on the falling edge of PCLK.
BLANK#	O*	44	TS2D (*C)	Blank output. This output is clocked out on the falling edge of PCLK and is driven low during display blanking periods.
HSYNC#	O*	41	TS4D (*C)	Horizontal Sync. This output is clocked out on the falling edge of PCLK and is driven to indicate the horizontal retrace period. The polarity of this signal is determined by a control bit in register 3C2H.
VSYNC#	O*	42	TS4D (*C)	Vertical Sync. This output is clocked out on the falling edge of PCLK and is driven to indicate the vertical retrace period. The polarity of this signal is determined by a control bit in register 3C2H.
DACRD#	O*	43	TS3 (*C)	RAMDAC Read Strobe. This signal goes low when a valid read access to the VGA RAMDAC is decoded by the chip.
DACWR#	O*	45	TS3 (*C)	RAMDAC Write Strobe. This signal goes low when a valid write access to the VGA RAMDAC is decoded by the chip.
RS2	O*	46	TS2D (*C)	Register Select 2 output. This output should be connected to the RS2 input of the RAMDAC (Bt477 or equivalent). The logic level on this output may be set by setting Auxiliary Register [0B] bit 3. This signal is required to allow CPU access the control and overlay registers of the external RAMDAC.
OL[0:1]	I/O	39,38	OL0 C/ TS2 OL1 TTLS/ TS2	Multiple Function: Overlay Select outputs 1:0 When MD[13] = 0 at RESET, these pins are outputs used to provide sprite/HW cursor function on the CRT display. In this case, these outputs should be connected to the OL[0:1] inputs of the RAMDAC (Bt477 or equivalent). They are used by the sprite circuitry to access the overlay registers in the RAMDAC.
OL23	O*	35	TS2D (*C)	Overlay Select output 2/3. This output should be connected to both the OL2 and OL3 inputs of the RAMDAC (Bt477 or equivalent). This signal is used by the sprite circuitry to access the overlay registers in the RAMDAC.
D477	O*	40	TS2 (*C)	477 Control Signal. This output should be connected to the 477/471 input of the RAMDAC (Bt477 or equivalent). This signal is used to access the control register of the RAMDAC and to allow it to be powered down. The logic level on this output can be controlled by setting Auxiliary Register [0B] bit 4, and is also controlled by the power save logic.
IREFEN#	O*	47	TS2U3 (*C)	IREF Enable output. This signal is used to control the external current reference source required by the RAMDAC, allowing powering down the analog circuitry when not required. When this signal is driven low, the external current reference should be enabled. When this signal is high, the external current reference should be shut off.
MS[2:0]	I/O	83,82,71	TTL/ TTLS	Monitor Sense inputs. These signals should be connected to the monitor sense lines from the CRT monitor cable. The status of these bits is readable in Auxiliary register [08] bits 2:0, and is used by BIOS software to determine the presence and type of monitor connected. Optionally, the SENSE output of the RAMDAC may be connected to one of these inputs to allow the BIOS to read the SENSE signal and detect the monitor. These pint can be forced low by the DCC2 monitor support bits in AUX [10h] bits 1:0.

■ PACKGE DIMENSIONS

Plastic QFP17-144pin



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