

# MN4022B/MN4022BS

## 4-Stage Divide-by-8 Johnson Counter

### ■ Outline

The MN4022B/S is an octal Johnson counter consisting of 4-stage D-type flip-flops.

It has a built-in decoder to convert the output into an octal number.





One of eight outputs  $O_0 \sim O_7$  becomes the "H" level according to the number of count pulses impressed on the input of  $CP_0$  or  $\overline{CP}_1$ .

The counter advances at the rise of  $CP_0$  when  $\overline{CP}_1 = "L"$  and at the fall of  $\overline{CP}_1$  when  $CP_0 = "H"$ .

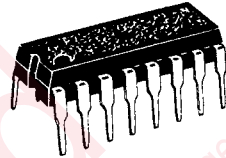
The "H" level MR input resets the counter when  $O_0 = "H"$  or when  $O_1 \sim O_7 = "L"$  irrespectively of  $CP_0$  and  $\overline{CP}_1$ .

This 4-stage divide-by-8 Johnson counter is equivalent to Motorola's MC14022B and RCA's CD4022B.

### ■ Truth Table

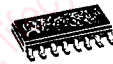
MR	$CP_0$	$\overline{CP}_1$	Operation Mode
H	×	×	$O_0 = \overline{O}_{4-7} = H, O_1 \sim O_7 = L$
L	H		Counter Advances
L		L	
L	L	×	No Change
L	×	H	
L	H		
L		L	

P-3



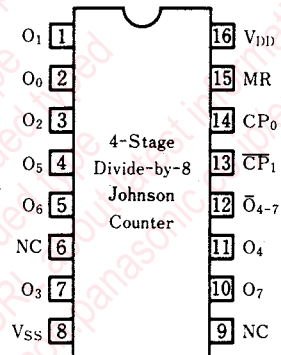
16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

Pin Configuration



### ■ Absolute Maximum Ratings (Ta=25°C)

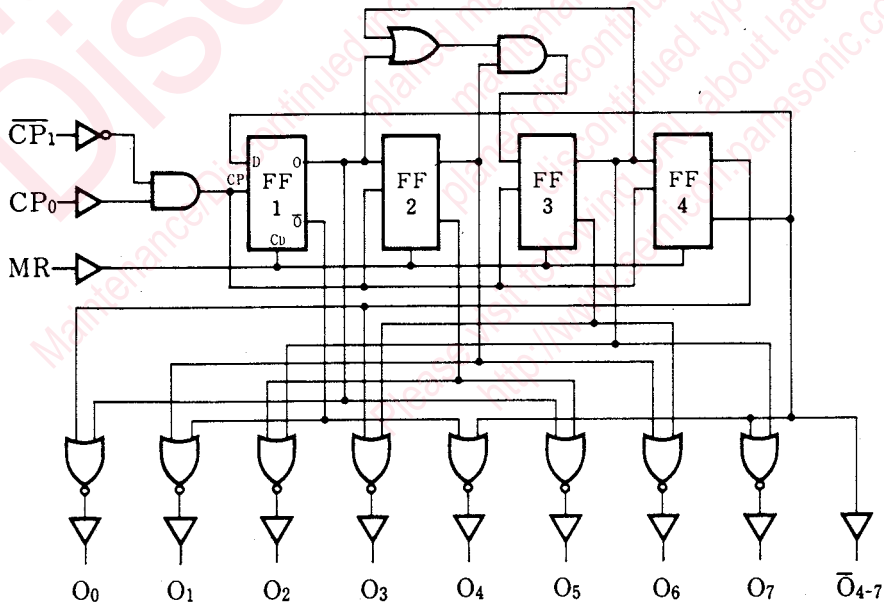
Item	Symbol	Rating	Unit
Supply voltage	$V_{DD}$	-0.5~+18	V
Input voltage	$V_i$	-0.5~ $V_{DD}+0.5^*$	V
Output pin voltage	$V_o$	-0.5~ $V_{DD}+0.5^*$	V
Peak input · output pin current	$\pm I_i$	max. 10	mA
Power dissipation (per package)	$T_a = -40 \sim +60^\circ\text{C}$	max. 400	mW
	$T_a = +60 \sim +80^\circ\text{C}$	Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)	$P_D$	max. 100	mW
Operating ambient temperature	$T_{opr}$	-40~+85	°C
Storage temperature	$T_{stg}$	-65~+150	°C

\*  $V_{DD}+0.5V$  should be lower than 18V.

■ DC Characteristics ( $V_{SS}=0V$ )

Item	$V_{DD}$ (V)	Symbol	Condition	$T_a=-40^{\circ}C$		$T_a=25^{\circ}C$		$T_a=85^{\circ}C$		Unit	
				min.	max.	min.	max.	min.	max.		
Static supply current	5	$I_{DD}$	$V_i=V_{SS}$ or $V_{DD}$	—	20	—	20	—	150	$\mu A$	
	10			—	40	—	40	—	300		
	15			—	80	—	80	—	600		
Output voltage low level	5	$V_{OL}$	$V_i=V_{SS}$ or $V_{DD}$ $ I_{O}  < 1\mu A$	—	0.05	—	0.05	—	0.05	V	
	10			—	0.05	—	0.05	—	0.05		
	15			—	0.05	—	0.05	—	0.05		
Output voltage high level	5	$V_{OH}$	$V_i=V_{SS}$ or $V_{DD}$ $ I_{O}  < 1\mu A$	4.95	—	4.95	—	4.95	—	V	
	10			9.95	—	9.95	—	9.95	—		
	15			14.95	—	14.95	—	14.95	—		
Input voltage low level	5	$V_{IL}$	$ I_{O}  < 1\mu A$	$V_O=0.5V$ or $4.5V$	—	1.5	—	1.5	—	V	
	10			$V_O=1V$ or $9V$	—	3	—	3	—		3
	15			$V_O=1.5V$ or $13.5V$	—	4	—	4	—		4
Input voltage high level	5	$V_{IH}$	$ I_{O}  < 1\mu A$	$V_O=0.5V$ or $4.5V$	3.5	—	3.5	—	3.5	V	
	10			$V_O=1V$ or $9V$	7	—	7	—	7		—
	15			$V_O=1.5V$ or $13.5V$	11	—	11	—	11		—
Output current low level	5	$I_{OL}$	$V_O=0.4V, V_i=0$ or $5V$	0.52	—	0.44	—	0.36	—	mA	
	10		$V_O=0.5V, V_i=0$ or $10V$	1.3	—	1.1	—	0.9	—		
	15		$V_O=1.5V, V_i=0$ or $15V$	3.6	—	3	—	2.4	—		
Output current high level	5	$-I_{OH}$	$V_O=4.6V, V_i=0$ or $5V$	0.52	—	0.44	—	0.36	—	mA	
	10		$V_O=9.5V, V_i=0$ or $10V$	1.3	—	1.1	—	0.9	—		
	15		$V_O=13.5V, V_i=0$ or $15V$	3.6	—	3	—	2.4	—		
Output current high level	5	$-I_{OH}$	$V_O=2.5V, V_i=0$ or $5V$	1.7	—	1.4	—	1.1	—	mA	
Input leakage current	15	$\pm I_I$	$V_i=0$ or $15V$	—	0.3	—	0.3	—	1	$\mu A$	

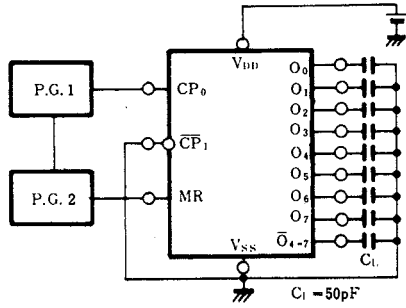
■ Logic Diagram



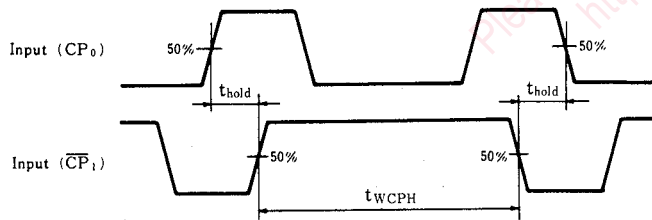
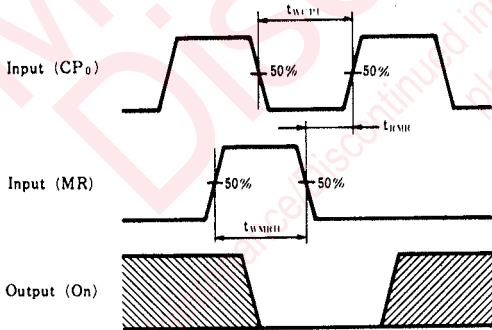
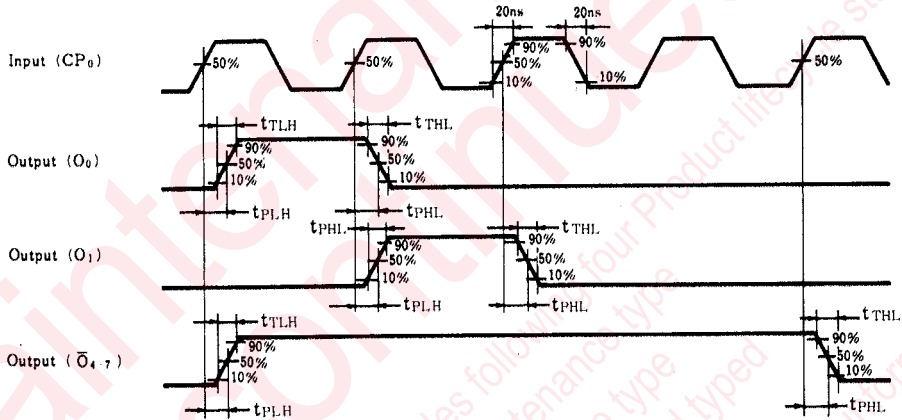
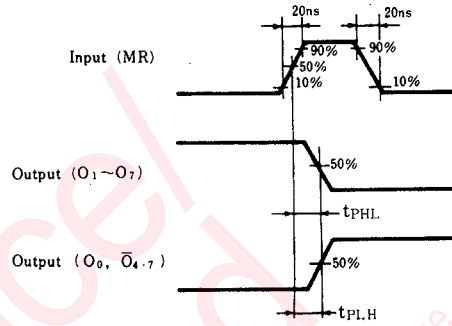
■ Switching Characteristics (Ta=25°C, V<sub>SS</sub>=0V, C<sub>L</sub>=50pF)

Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t <sub>TLH</sub>	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t <sub>THL</sub>	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation time CP <sub>0</sub> , $\overline{CP}_1 \rightarrow \text{On}$ (H→L)	5	t <sub>PHL</sub>	—	195	585	ns
	10		—	75	225	
	15		—	50	150	
Propagation time CP <sub>0</sub> , $\overline{CP}_1 \rightarrow \text{On}$ (L→H)	5	t <sub>PLH</sub>	—	245	735	ns
	10		—	95	285	
	15		—	60	180	
Propagation time CP <sub>0</sub> , $\overline{CP}_1 \rightarrow \overline{O}_{4,7}$ (H→L)	5	t <sub>PHL</sub>	—	245	735	ns
	10		—	90	270	
	15		—	60	180	
Propagation time CP <sub>0</sub> , $\overline{CP}_1 \rightarrow \overline{O}_{4,7}$ (L→H)	5	t <sub>PLH</sub>	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
Propagation time MR→O <sub>1</sub> to O <sub>7</sub> (H→L)	5	t <sub>PHL</sub>	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation time MR→O <sub>0</sub> (L→H)	5	t <sub>PLH</sub>	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation time MR→ $\overline{O}_{4,7}$ (L→H)	5	t <sub>PLH</sub>	—	110	330	ns
	10		—	45	135	
	15		—	35	105	
Hold time CP <sub>0</sub> → $\overline{CP}_1$	5	t <sub>hold</sub>	—	70	210	ns
	10		—	25	75	
	15		—	15	45	
Hold time $\overline{CP}_1$ →CP <sub>0</sub>	5	t <sub>hold</sub>	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Minimum clock pulse width	5	t <sub>wCP</sub>	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Minimum reset pulse width	5	t <sub>wMRH</sub>	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Reset recovery time	5	t <sub>RM</sub>	—	10	30	ns
	10		—	5	15	
	15		—	5	15	
Maximum clock frequency	5	f <sub>max</sub>	3	6	—	ns
	10		8	16	—	
	15		12	24	—	
Input capacitance		C <sub>i</sub>	—	—	7.5	pF

1. Switching time measuring circuit



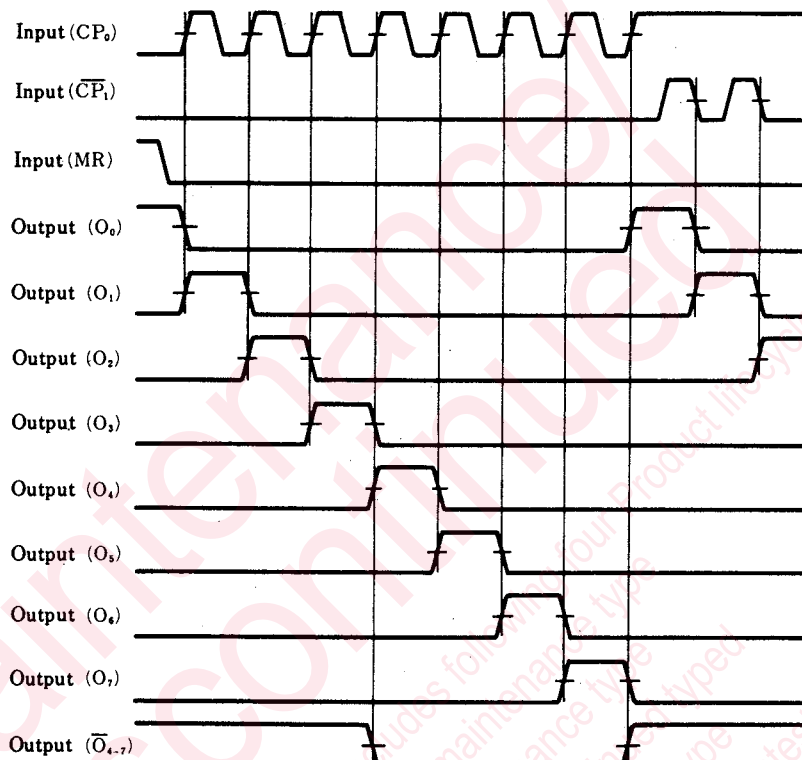
2. Switching waveforms



Waveforms showing recovery time for MR; minimum  $CP_0$  and MR pulse widths.  
 Conditions:  $\overline{CP}_1 = \text{LOW}$  while  $CP_0$  is triggered on a LOW to HIGH transition.  
 $t_{WCP}$  and  $t_{RMR}$  also apply when  $CP_0 = \text{HIGH}$  and  $\overline{CP}_1$  is triggered on a HIGH to LOW transition.

Waveforms showing hold times for  $CP_0$  to  $\overline{CP}_1$  and  $\overline{CP}_1$  to  $CP_0$ .  
 Hold times are shown as positive values, but may be specified as negative values.

■ Timing Diagram



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