

FEATURES

- Single up/down count mode control line
- Asynchronous parallel load
- Count enable, parallel load control inputs
- Cascadable
- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440 μ A source current
- 100% reliability assurance testing in compliance with MIL-STD-883

DESCRIPTION

The 25LS190 and 25LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The 25LS191 is a 4-bit binary counter and the 25LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable and down/up inputs should be made only when the clock input is high. The

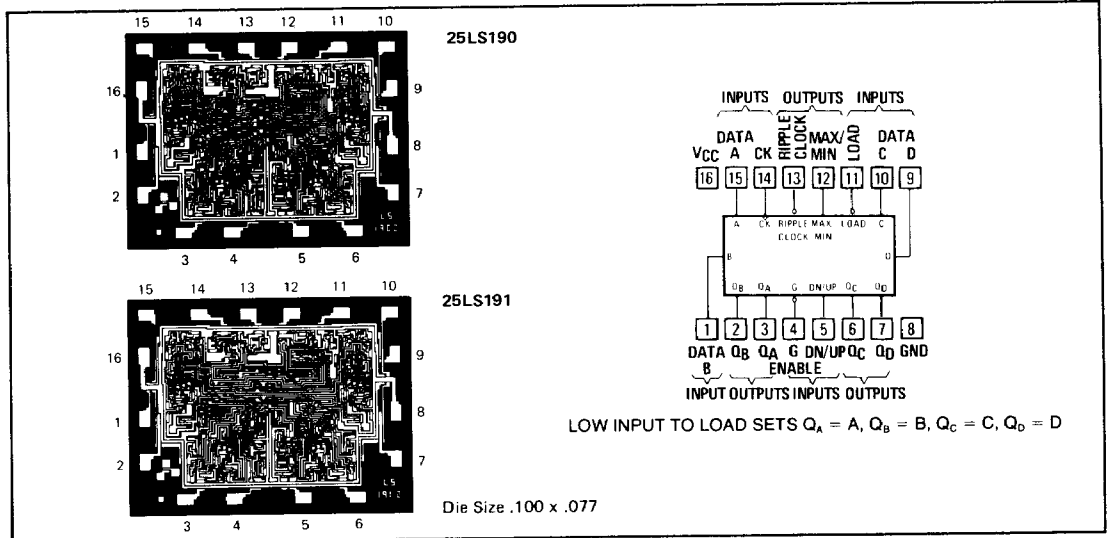
direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN-OUT DIAGRAM



Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-440			-440	μ A
Low-level output current, I_{OL}	4		8	4		8	mA
Input clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	25			25			ns
Data setup time, t_{setup} (see Figures 1 and 2)	12			12			ns
Enable to clock setup time, t_{setup}	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*	Military			Commercial			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I		$V_{CC} = \text{MIN}$, $I_I = -18\text{mA}$			-1.5			-1.5	V
V_{OH}		$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{V}$, $V_{IL} = V_{IL\text{max}}$, $I_{OH} = -440\mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}		$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{V}$, $V_{IL} = V_{IL\text{max}}$							V
		$I_{OL} = 4\text{mA}$		0.25	0.40		0.25	0.40	
		$I_{OL} = 8\text{mA}$		0.30	0.45		0.30	0.45	
I_I	Enable	$V_{CC} = \text{MAX}$, $V_I = 7\text{V}$			0.3			0.3	mA
	Others				0.1		0.1		
I_{IH}	Enable	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$			60			60	μ A
	Others				20		20		
I_{IL}	Enable	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$			-1.08			-1.08	mA
	Others				-0.4		-0.4		
I_{OS}^{\dagger}		$V_{CC} = \text{MAX}$	-15		-85	-15		-85	mA
$I_{CC}^{\dagger\dagger}$		$V_{CC} = \text{MAX}$		20	35		20	35	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.

\dagger Not more than one output should be shorted at a time.

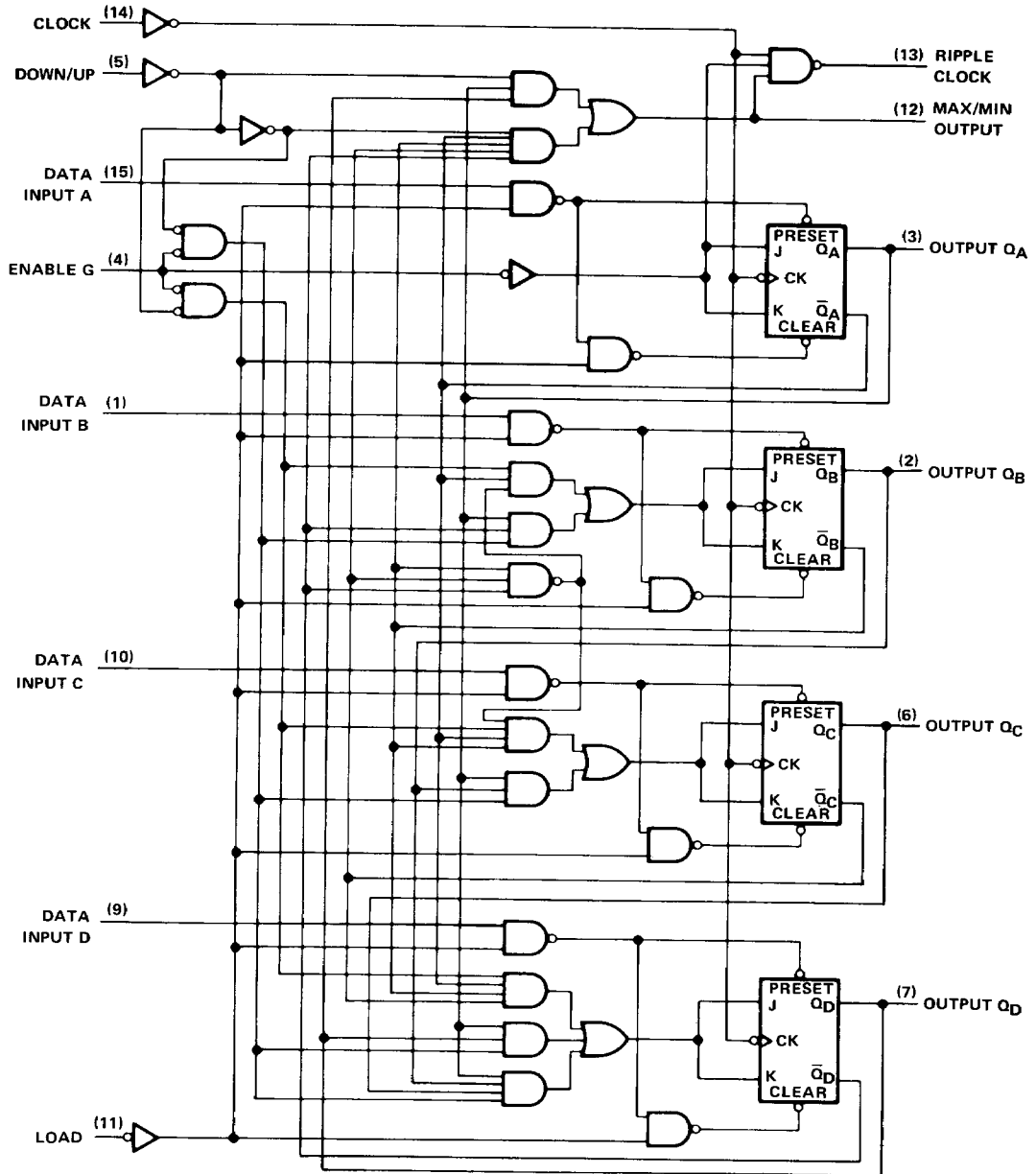
$\dagger\dagger I_{CC}$ is measured with all inputs grounded and all outputs open.

Switching Characteristics, $V_{CC} = T_A = +25^{\circ}\text{C}$

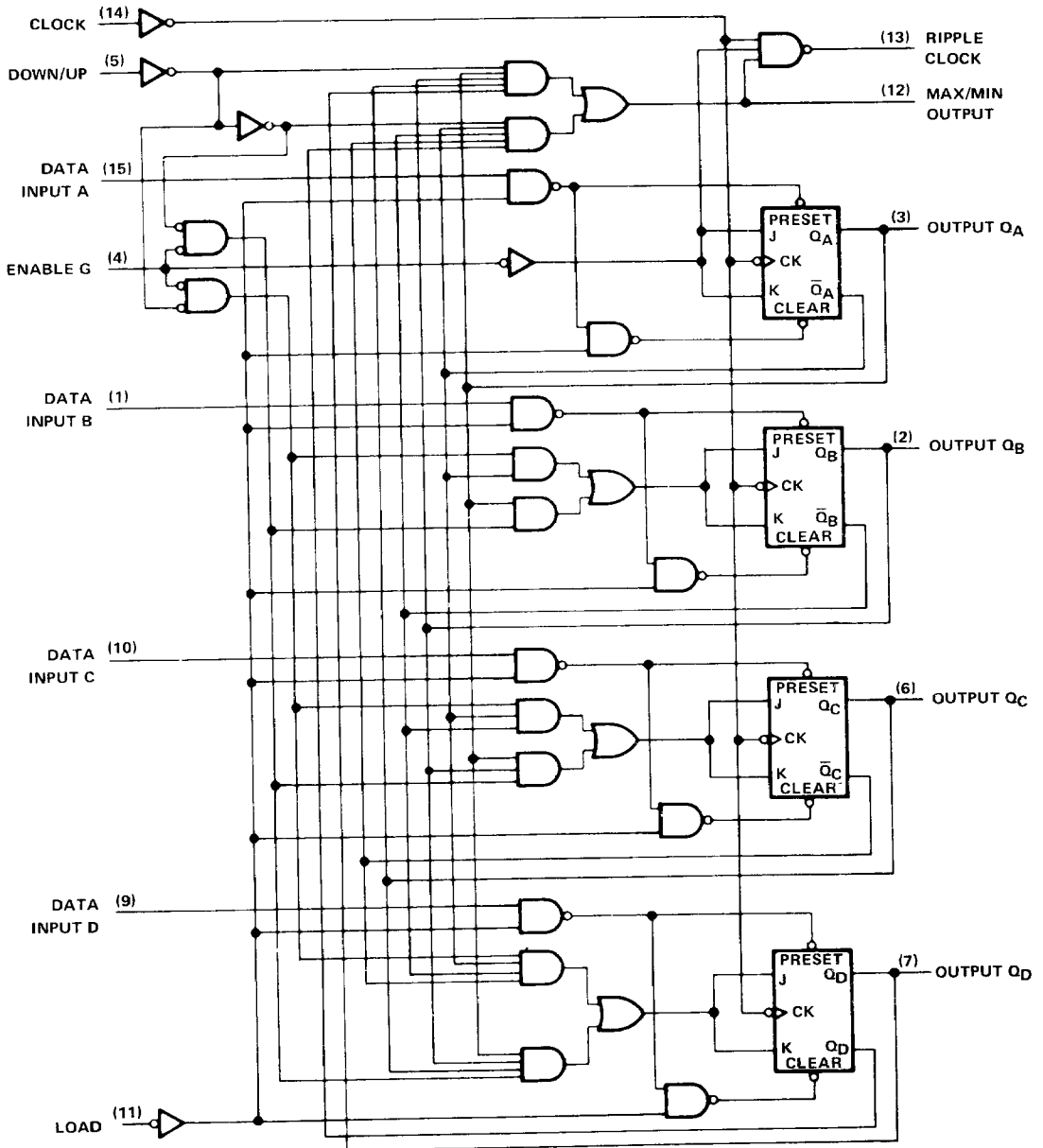
Parameter	From (input)	To (output)	+25°C			Unit
			Min	Typ	Max	
Test Conditions: $C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$ (see Fig. 1 and 3 thru 7 on pages 3-56 and 3-57 and Fig. A on page 2-174)						
f_{max}			25	35		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D		22	33	ns
t_{PHL}				30	39	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D		13	22	ns
t_{PHL}				29	39	
t_{PLH}	Clock	Ripple Clock		11	18	ns
t_{PHL}				14	21	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D		15	21	ns
t_{PHL}				16	30	
t_{PLH}	Clock	Max/Min		23	39	ns
t_{PHL}				22	39	
t_{PLH}	Down/Up	Ripple Clock		16	45	ns
t_{PHL}				25	45	
t_{PLH}	Down/Up	Max/Min		17	33	ns
t_{PHL}				12	33	
t_{PLH}	Enable	Ripple Clock		10	19	ns
t_{PHL}				14	27	

LOGIC DIAGRAM

25LS190



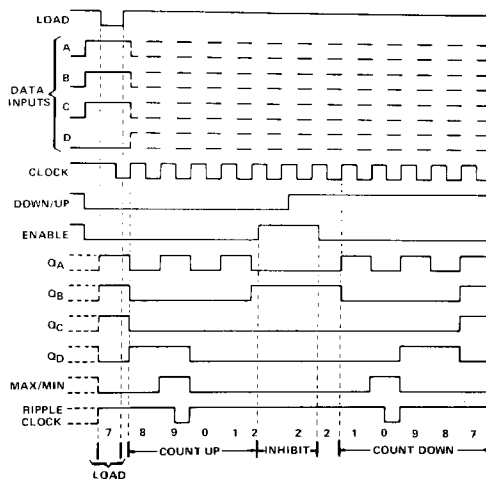
LOGIC DIAGRAM
25LS191



25LS190 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence.

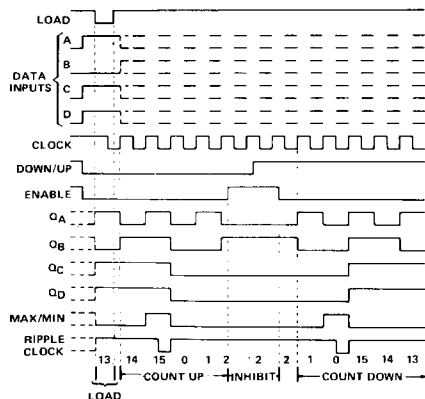
1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



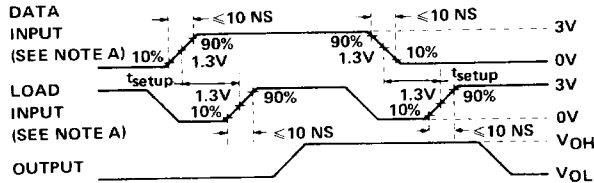
25LS191 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



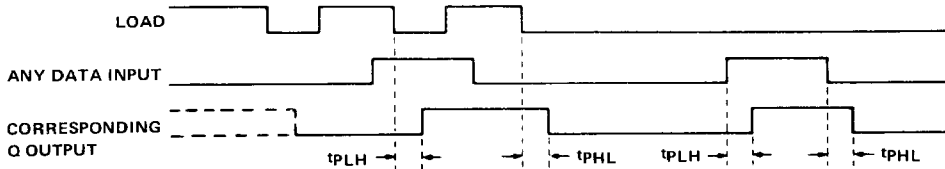
PARAMETER MEASUREMENT INFORMATION



NOTE:

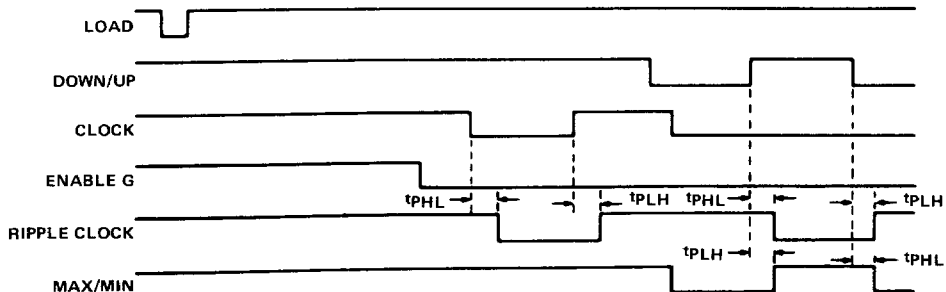
A. The inputs pulses are supplied by generators having the following characteristics: $Z_{out} = 50\Omega$, duty cycle $\leq 50\%$, PRR ≤ 1 MHz.

FIGURE 1—DATA SETUP TIME VOLTAGE WAVEFORMS



NOTE: Conditions on other inputs are irrelevant.

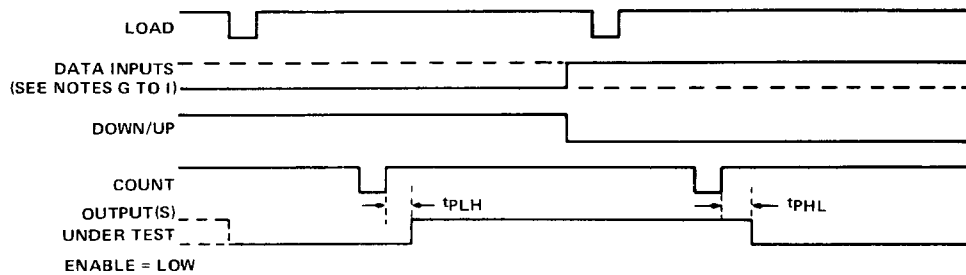
FIGURE 2—LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE: All data inputs are low.

FIGURE 3—ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO MAX/MIN

PARAMETER MEASUREMENT INFORMATION (Continued)



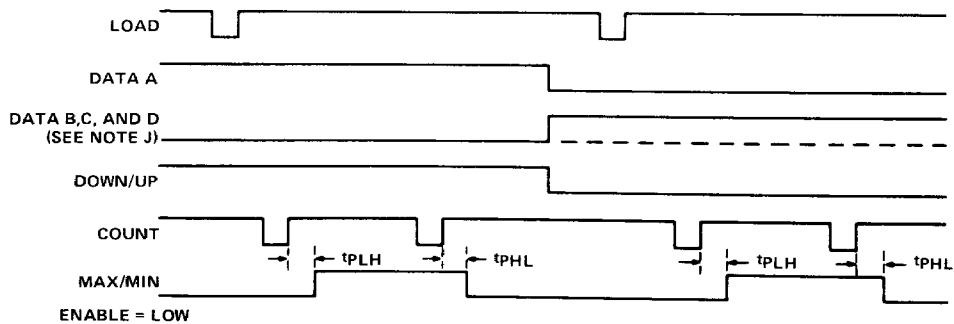
NOTES:

F. To test Q_A , Q_B , and Q_C outputs of 25LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.

G. To test Q_D output of 25LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.

H. To test Q_A , Q_B , Q_C , and Q_D outputs of 54LS191: All four data inputs are shown by the solid line.

FIGURE 4—CLOCK TO OUTPUT



NOTE 1:

Data inputs B and C are shown by the dashed line for the 25LS190 and the solid line for the 25LS191: Data input D is shown by the solid line for both devices.

FIGURE 5—CLOCK TO MAX/MIN