CONTENTS

Standard TV microcontrollers with On-Screen Display (OSD)

SAA55xx

1 FEATURES

- Single-chip microcontroller with integrated On-Screen Display (OSD)
- Versions available with integrated data capture
- One Time Programmable (OTP) memory for both program Read Only Memory (ROM) and character sets
- Single power supply: 3.0 to 3.6 V
- 5 V tolerant digital inputs and I/O
- 29 I/O lines via individual addressable controls
- Programmable I/O for push-pull, open-drain and quasi-bidirectional
- Two port lines with 8 mA sink (at <0.4 V) capability, for direct drive of Light Emitting Diode (LED)
- Single crystal oscillator for microcontroller, OSD and data capture
- Power reduction modes: Idle and Power-down
- Byte level I²C-bus with dual port I/O
- Pin compatibility throughout family
- Operating temperature: –20 to +70 °C.

2 GENERAL DESCRIPTION

The SAA55xx standard family of microcontrollers are a derivative of the Philips industry-standard 80C51 microcontroller, and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system, OSD, and some versions include an integrated data capture and display function.

The data capture hardware has the capability of decoding and displaying both 525 and 625-line World System Teletext (WST), Video Programming System (VPS) and Wide Screen Signalling (WSS) information. The same display hardware is used both for Teletext and OSD, which means that the display features available give greater flexibility to differentiate the TV set.

The SAA55xx standard family offers a range of functionality from non-text, 16-kbyte program ROM and 256-byte Random Access Memory (RAM), to a 10-page text version, 64-kbyte program ROM and 1.2-kbyte RAM.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_{DDX}	any supply voltage (V_{DD} to V_{SS})	3.0	3.3	3.6	V
I_{DDP}	periphery supply current	1	–	–	mA
I_{DDC}	core supply current	–	15	18	mA
$I_{DDC(id)}$	Idle mode core supply current	–	4.6	6	mA
$I_{DDC(pd)}$	Power-down mode core supply current	–	0.76	1	mA
$I_{DDC(stb)}$	Standby mode core supply current	–	5.11	6.50	mA
I_{DDA}	analog supply current	–	45	48	mA
$I_{DDA(id)}$	Idle mode analog supply current	–	0.87	1.0	mA
$I_{DDA(pd)}$	Power-down mode analog supply current	–	0.45	0.7	mA
$I_{DDA(stb)}$	Standby mode analog supply current	–	0.95	1.20	mA
f_{xtal}	crystal frequency	–	12	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE[2]			ROM	RAM	TEXT PAGES
	NAME	DESCRIPTION	VERSION			
SAA5500PS/nnnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	16-kbyte	256-byte	–
SAA5501PS/nnnn				32-kbyte	512-byte	–
SAA5502PS/nnnn				48-kbyte	256-byte	–
SAA5503PS/nnnn				64-kbyte	512-byte	–
SAA5520PS/nnnn				16-kbyte	256-byte	1
SAA5521PS/nnnn				32-kbyte	512-byte	1
SAA5522PS/nnnn				48-kbyte	750-byte	1
SAA5523PS/nnnn				64-kbyte	1-kbyte	1
SAA5551PS/nnnn				32-kbyte	750-byte	10
SAA5552PS/nnnn				48-kbyte	1-kbyte	10
SAA5553PS/nnnn				64-kbyte	1.2-kbyte	10

Notes

1. ‘nnnn’ is a four digit number uniquely referencing the microcontroller program mask.
2. For details of the LQFP100 package, please contact your local regional office for availability.

5 BLOCK DIAGRAM

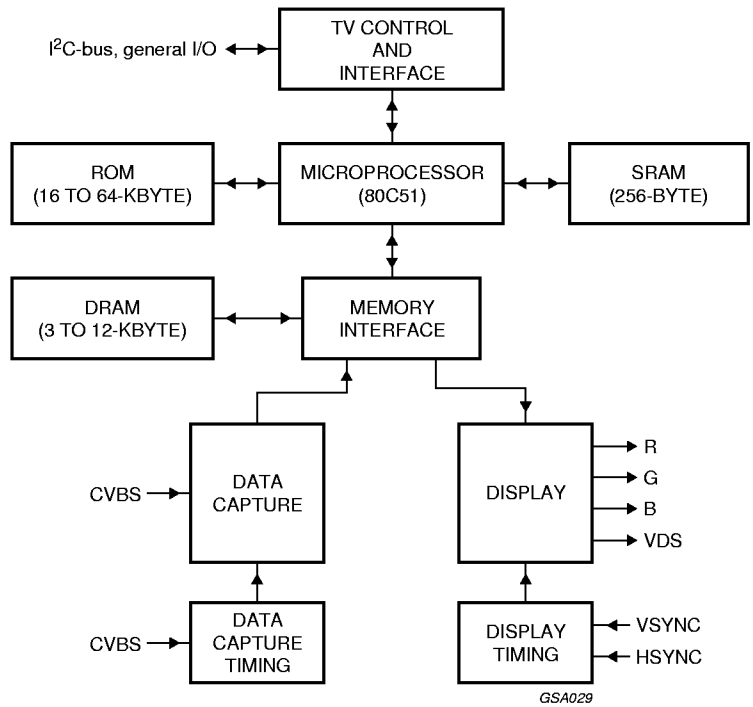


Fig.1 Block diagram (top level architecture).

6 PINNING INFORMATION

6.1 Pinning

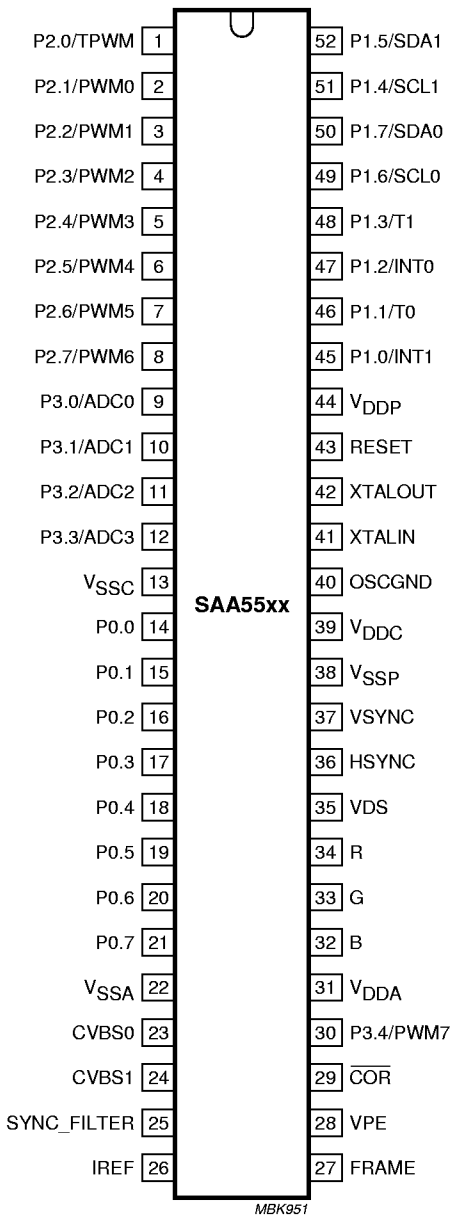


Fig.2 SDIP52 pin configuration.

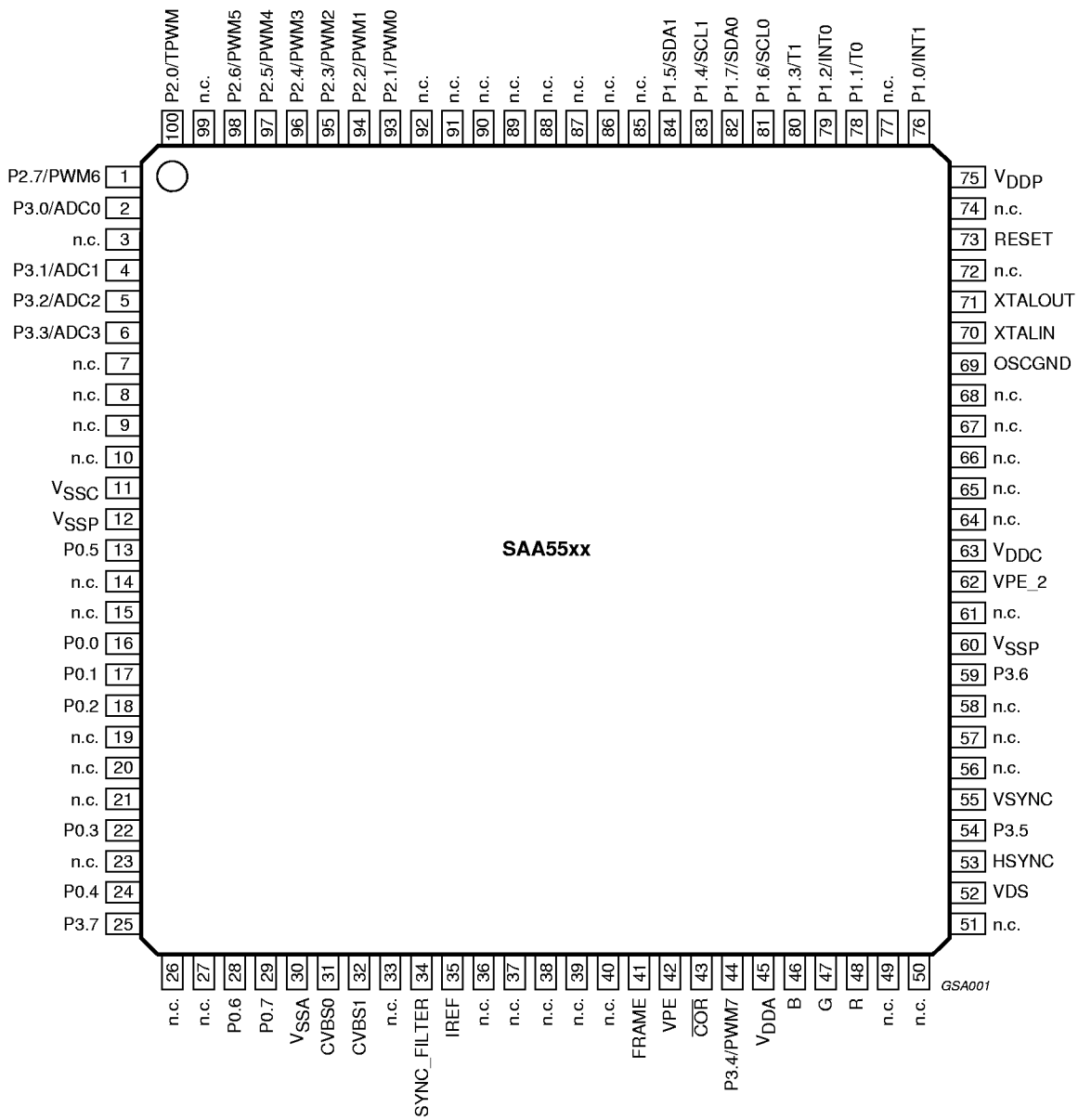


Fig.3 LQFP100 pin configuration.

6.2 Pin description

Table 1 SDIP52 and LQFP100 packages

SYMBOL	PIN		TYPE	DESCRIPTION
	SDIP52	LQFP100		
P2.0/TPWM	1	100	I/O	**Port 2.** 8-bit programmable bidirectional port with alternative functions. P2.0/TPWM is the output for the 14-bit high precision PWM and P2.1/PWM0 to P2.7/PWM6 are the outputs for the 6-bit PWMs 0 to 6.
P2.1/PWM0	2	93	I/O	
P2.2/PWM1	3	94	I/O	
P2.3/PWM2	4	95	I/O	
P2.4/PWM3	5	96	I/O	
P2.5/PWM4	6	97	I/O	
P2.6/PWM5	7	98	I/O	
P2.7/PWM6	8	1	I/O	
P3.0/ADC0	9	2	I/O	**Port 3.** 8-bit programmable bidirectional port with alternative functions. P3.0/ADC0 to P3.3/ADC3 are the inputs for the software ADC facility and P3.4/PWM7 is the output for the 6-bit PWM7. P3.5 to P3.7 have no alternative functions and are only available with the LQFP100 package.
P3.1/ADC1	10	4	I/O	
P3.2/ADC2	11	5	I/O	
P3.3/ADC3	12	6	I/O	
P3.4/PWM7	30	44	I/O	
P3.5	–	54	I/O	
P3.6	–	59	I/O	
P3.7	–	25	I/O	
V_{SSC}	13	11	–	core ground
P0.0	14	16	I/O	**Port 0.** 8-bit programmable bidirectional port. P0.5 and P0.6 have 8 mA current sinking capability for direct drive of LEDs.
P0.1	15	17	I/O	
P0.2	16	18	I/O	
P0.3	17	22	I/O	
P0.4	18	24	I/O	
P0.5	19	13	I/O	
P0.6	20	28	I/O	
P0.7	21	29	I/O	
V_{SSA}	22	30	–	analog ground
CVBS0	23	31	I	Composite video input. A positive-going 1 V (peak-to-peak) input is required; connected via a 100 nF capacitor.
CVBS1	24	32	I	
SYNC_FILTER	25	34	I	CVBS sync filter input. This pin should be connected to V_{SSA} via a 100 nF capacitor.
IREF	26	35	I	Reference current input for analog circuits, connected to V_{SSA} via a 24 kΩ resistor.
FRAME	27	41	O	De-interlace output synchronized with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits.
VPE	28	42	I	OTP programming voltage

SYMBOL	PIN		TYPE	DESCRIPTION
	SDIP52	LQFP100		
$\overline{COR}$	29	43	O	Open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display.
V_{DDA}	31	45	–	+3.3 V analog power supply
B	32	46	O	Pixel rate output of the BLUE colour information.
G	33	47	O	Pixel rate output of the GREEN colour information.
R	34	48	O	Pixel rate output of the RED colour information.
VDS	35	52	O	Video/data switch push-pull output for dot rate fast blanking.
HSYNC	36	53	I	Schmitt triggered input for a TTL-level version of the horizontal sync pulse; the polarity of this pulse is programmable by register bit TXT1.H POLARITY.
VSYNC	37	55	I	Schmitt triggered input for a TTL-level version of the vertical sync pulse; the polarity of this pulse is programmable by register bit TXT1.V POLARITY.
V_{SSP}	38	12, 60	–	periphery ground
V_{DDC}	39	63	–	+3.3 V core power supply
OSCGND	40	69	–	crystal oscillator ground
XTALIN	41	70	I	12 MHz crystal oscillator input
XTALOUT	42	71	O	12 MHz crystal oscillator output
RESET	43	73	I	If the reset input is HIGH for at least 2 machine cycles (24 oscillator periods) while the oscillator is running, the device is reset; this pin should be connected to V_{DDP} via a capacitor.
V_{DDP}	44	75	–	+3.3 V periphery power supply
P1.0/INT1	45	76	I/O	**Port 1.** 8-bit programmable bidirectional port with alternative functions. P1.0/INT1 is external interrupt 1 which can be triggered on the rising and falling edge of the pulse. P1.1/T0 is the counter/Timer 0. P1.2/INT0 is external interrupt 0. P1.3/T1 is the counter/Timer 1. P1.6/SCL0 is the serial clock input for the I^2C-bus and P1.7/SDA0 is the serial data port for the I^2C-bus. P1.4/SCL1 is the serial clock input for the I^2C-bus. P1.5/SDA1 is the serial data port for the I^2C-bus.
P1.1/T0	46	78	I/O	
P1.2/INT0	47	79	I/O	
P1.3/T1	48	80	I/O	
P1.6/SCL0	49	81	I/O	
P1.7/SDA0	50	82	I/O	
P1.4/SCL1	51	83	I/O	
P1.5/SDA1	52	84	I/O	
VPE_2	–	62	I	OTP programming voltage
n.c.	–	3, 7 to 10,14, 15, 19 to 21, 23, 26, 27, 33, 36 to 40, 49 to 51, 56 to 58, 61, 64 to 68, 72, 74, 77, 85 to 92, 99	–	not connected

7 MICROCONTROLLER

The functionality of the microcontroller used on this device is described here with reference to the industry standard 80C51 microcontroller. A full description of its functionality can be found in *"Handbook IC20, 80C51-Based 8-bit Microcontrollers"*.

7.1 Microcontroller features

- 80C51 microcontroller core standard instruction set and timing
- 1 μs machine cycle
- Maximum 64K × 8-bit Program ROM
- Maximum of 1.2K × 8-bit Auxiliary RAM
- Interrupt Controller for individual enable/disable with two level priority
- Two 16-bit Timer/Counter registers
- Watchdog Timer
- Auxiliary RAM page pointer
- 16-bit Data pointer
- Idle and Power-down modes
- 29 general I/O lines
- Eight 6-bit Pulse Width Modulator (PWM) outputs for control of TV analog signals
- One 14-bit PWM for Voltage Synthesis Tuner (VST) control
- 8-bit Analog-to-Digital Converter (ADC) with 4 multiplexed inputs
- 2 high current outputs for directly driving LEDs
- I^2C-bus byte level bus interface with dual ports.

8 MEMORY ORGANIZATION

The device has the capability of a maximum of 64-kbyte Program ROM and 1.2-kbyte Data RAM internally.

8.1 Security bits - program and verify

SAA55xx devices have a set of security bits allied with each section of the device, i.e. Program ROM, Character ROM and Packet 26 ROM. The security bits are used to prevent the ROM from being overwritten once programmed, and also the contents being verified once programmed. The security bits are one-time programmable and **cannot** be erased.

The SAA55xx memory and security bits are structured as shown in Fig.4. The SAA55xx security bits are set as shown in Fig.5 for production programmed devices and are set as shown in Fig.6 for production blank devices.

8.2 RAM organisation

The internal Data RAM is organised into two areas, Data memory and Special Function Registers (SFRs) as shown in Fig.7.

8.3 Data memory

The Data memory is 256 × 8-bit and occupies the address range 00H to FFH when using indirect addressing and 00H to 7FH when using direct addressing. The SFRs occupy the address range 80H to FFH and are accessible using direct addressing only.

The lower 128 bytes of Data memory are mapped as shown in Fig.8.

The lowest 24 bytes are grouped into 4 banks of 8 registers, the next 16 bytes above the register banks form a block of bit addressable memory space.

The upper 128 bytes are not allocated for any special area or functions.

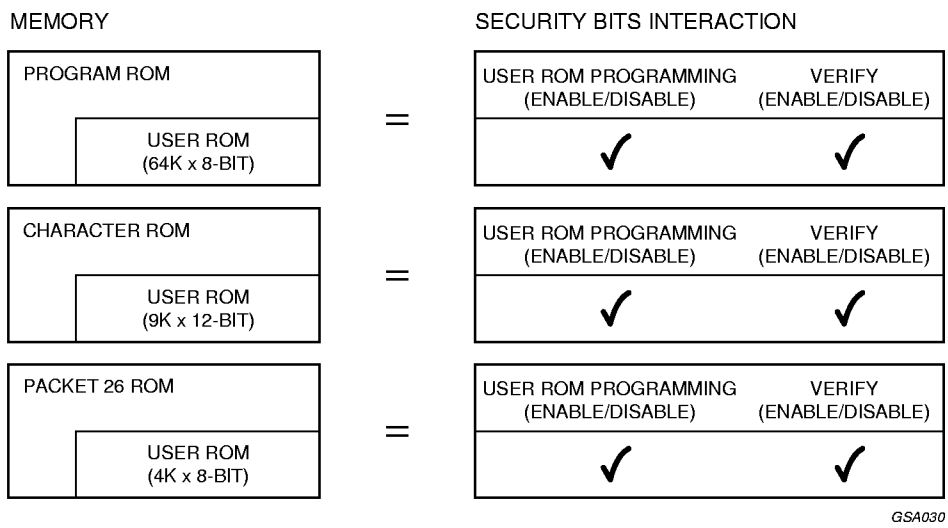


Fig.4 Memory and security bit structures.

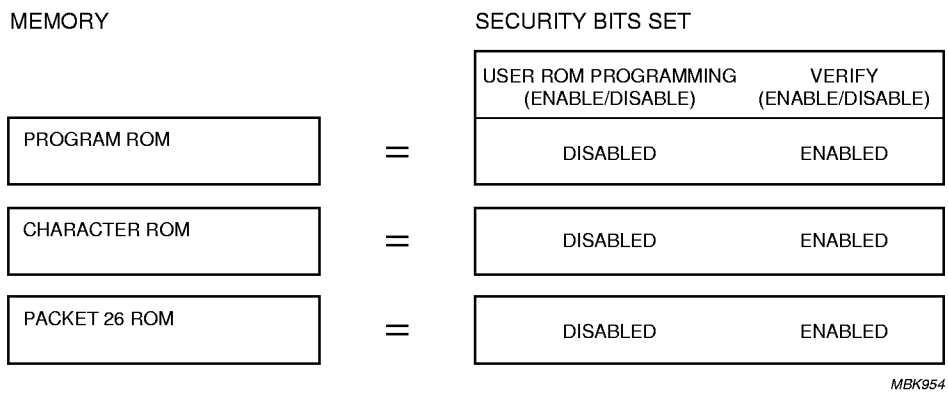


Fig.5 Security bits for production devices.

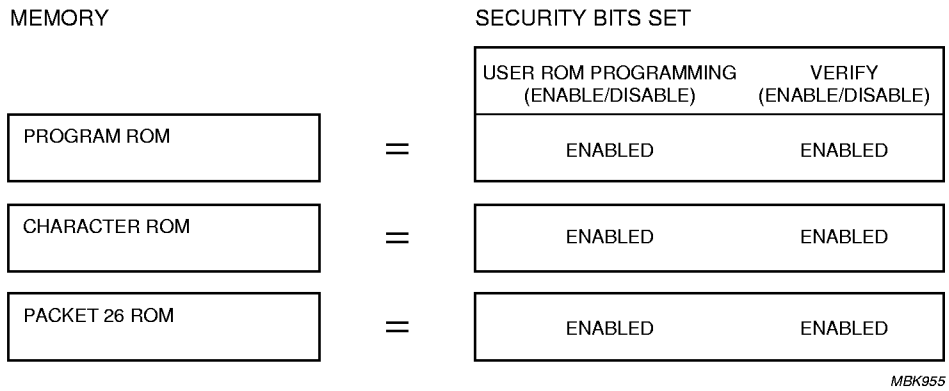


Fig.6 Security bits for production blank devices.

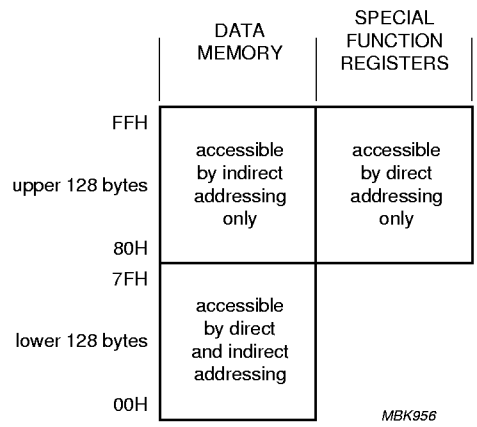


Fig.7 Internal Data memory.

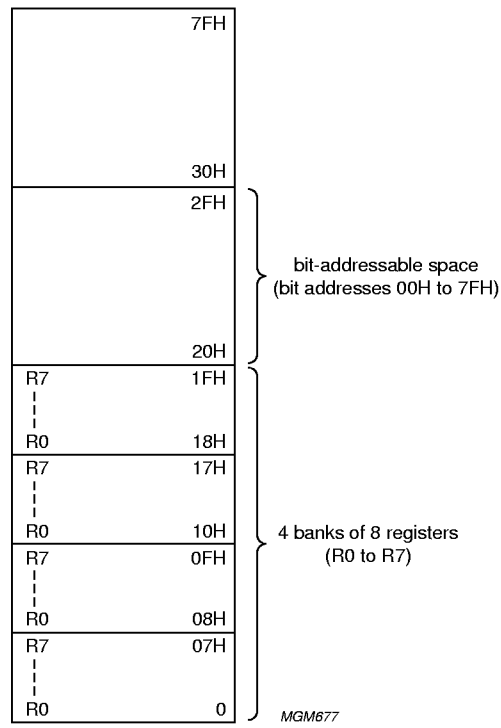


Fig.8 Lower 128 bytes of internal RAM.

8.4 SFR memory

The Special Function Register (SFR) space is used for port latches, timer, peripheral control, acquisition control, display control. These registers can only be accessed by direct addressing. Sixteen of the addresses in the SFR space are both bit and byte addressable. The bit addressable SFRs are those whose address ends in 0H or 8H. A summary of the SFR map in address order is shown in Table 2.

A description of each of the SFR bits is shown in Table 3 which presents the SFRs in alphabetical order.

Table 2 SFR memory map

ADD	R/W	NAMES	7	6	5	4	3	2	1	0	RESET
80H	R/W	P0	P07	P06	P05	P04	P03	P02	P01	P00	FFH
81H	R/W	SP	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	07H
82H	R/W	DPL	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0	00H
83H	R/W	DPH	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0	00H
87H	R/W	PCON	0	ARD	RFI	WLE	GF1	GF0	PD	IDL	00H
88H	R/W	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
89H	R/W	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H
8AH	R/W	TL0	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00	00H
8BH	R/W	TL1	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10	00H
8CH	R/W	TH0	TH07	TH06	TH05	TH04	TH03	TH02	TH01	TH00	00H
8DH	R/W	TH1	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10	00H
90H	R/W	P1	P17	P16	P15	P14	P13	P12	P11	P10	FFH
96H	R/W	P0CFGA	P0CFGA7	P0CFGA6	P0CFGA5	P0CFGA4	P0CFGA3	P0CFGA2	P0CFGA1	P0CFGA0	FFH
97H	R/W	P0CFGB	P0CFGB7	P0CFGB6	P0CFGB5	P0CFGB4	P0CFGB3	P0CFGB2	P0CFGB1	P0CFGB0	00H
98H	R/W	SADB	0	0	0	DC_COMP	SAD3	SAD2	SAD1	SAD0	00H
9EH	R/W	P1CFGA	P1CFGA7	P1CFGA6	P1CFGA5	P1CFGA4	P1CFGA3	P1CFGA2	P1CFGA1	P1CFGA0	FFH
9FH	R/W	P1CFGB	P1CFGB7	P1CFGB6	P1CFGB5	P1CFGB4	P1CFGB3	P1CFGB2	P1CFGB1	P1CFGB0	00H
A0H	R/W	P2	P27	P26	P25	P24	P23	P22	P21	P20	FFH
A6H	R/W	P2CFGA	P2CFGA7	P2CFGA6	P2CFGA5	P2CFGA4	P2CFGA3	P2CFGA2	P2CFGA1	P2CFGA0	FFH
A7H	R/W	P2CFGB	P2CFGB7	P2CFGB6	P2CFGB5	P2CFGB4	P2CFGB3	P2CFGB2	P2CFGB1	P2CFGB0	00H
A8H	R/W	IE	EA	EBUSY	ES2	–	ET1	EX1	ET0	EX0	00H
B0H	R/W	P3	P37	P36	P35	P34	P33	P32	P31	P30	FFH
B2H	R/W	TXT18	NOT3	NOT2	NOT1	NOT0	0	0	BS1	BS0	00H
B3H	R/W	TXT19	TEN	TC2	TC1	TC0	0	0	TS1	TS0	00H
B4H	R/W	TXT20	0	0	0	0	OSD LANG ENABLE	OSD LAN2	OSD LAN1	OSD LAN0	00H

ADD	R/W	NAMES	7	6	5	4	3	2	1	0	RESET
B5H	R/W	TXT21	0	0	0	0	I²C PORT 1	0	I²C PORT 0	0	02H
B6H	R	TXT22	GPF7	GPF6	0	GPF4	GPF3	0	GPF1	GPF0	XXH
B8H	R/W	IP	0	PBUSY	PES2	PCC	PT1	PX1	PT0	PX0	00H
B9H	R/W	TXT17	0	FORCE ACQ1	FORCE ACQ0	FORCE DISP1	FORCE DISP0	SCREEN COL2	SCREEN COL1	SCREEN COL0	00H
BAH	R	WSS1	0	0	0	WSS<3:0> ERROR	WSS3	WSS2	WSS1	WSS0	00H
BBH	R	WSS2	0	0	0	WSS<7:4> ERROR	WSS7	WSS6	WSS5	WSS4	00H
BCH	R	WSS3	WSS<13:11> ERROR	WSS13	WSS12	WSS11	WSS<10:8> ERROR	WSS10	WSS9	WSS8	00H
BEH	R/W	P3CFGA	1	1	1	P3CFGA4	P3CFGA3	P3CFGA2	P3CFGA1	P3CFGA0	FFH
BFH	R/W	P3CFGB	0	0	0	P3CFGB4	P3CFGB3	P3CFGB2	P3CFGB1	P3CFGB0	00H
C0H	R/W	TXT0	X24 POSN	DISPLAY X24	AUTO FRAME	DISABLE HEADER ROLL	DISPLAY STATUS ROW ONLY	DISABLE FRAME	VPS ON	INV ON	00H
C1H	R/W	TXT1	EXT PKT OFF	8-BIT	ACQ OFF	X26 OFF	FULL FIELD	FIELD POLARITY	H POLARITY	V POLARITY	00H
C2H	R/W	TXT2	ACQ BANK	REQ3	REQ2	REQ1	REQ0	SC2	SC1	SC0	00H
C3H	W	TXT3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	00H
C4H	R/W	TXT4	OSD BANK ENABLE	QUAD WIDTH ENABLE	EAST/$\overline{\text{WEST}}$	DISABLE DOUBLE HEIGHT	B MESH ENABLE	C MESH ENABLE	TRANS ENABLE	SHADOW ENABLE	00H
C5H	R/W	TXT5	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03H
C6H	R/W	TXT6	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03H
C7H	R/W	TXT7	STATUS ROW TOP	CURSOR ON	REVEAL	BOTTOM /$\overline{\text{TOP}}$	DOUBLE HEIGHT	BOX ON 24	BOX ON 1 – 23	BOX ON 0	00H
C8H	R/W	TXT8	(reserved) 0	$\overline{\text{FLICKER}}$ $\overline{\text{STOP ON}}$	(reserved) 0	DISABLE SPANISH	PKT 26 RECEIVED	WSS RECEIVED	WSS ON	CVBS1/ $\overline{\text{CVBS0}}$	00H
C9H	R/W	TXT9	CURSOR FREEZE	CLEAR MEMORY	A0	R4	R3	R2	R1	R0	00H
CAH	R/W	TXT10	0	0	C5	C4	C3	C2	C1	C0	00H
CBH	R/W	TXT11	D7	D6	D5	D4	D3	D2	D1	D0	00H

ADD	R/W	NAMES	7	6	5	4	3	2	1	0	RESET
CCH	R	TXT12	525/$\overline{625}$ SYNC	SPANISH	ROM VER3	ROM VER2	ROM VER1	ROM VER0	1	VIDEO SIGNAL QUALITY	XXXX XX1X
CDH	R/W	TXT14	0	0	0	–	PAGE3	PAGE2	PAGE1	PAGE0	00H
CEH	R/W	TXT15	0	0	0	–	BLOCK3	BLOCK2	BLOCK1	BLOCK0	00H
D0H	R/W	PSW	C	AC	F0	RS1	RS0	OV	–	P	00H
D2H	R/W	TDACL	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	00H
D3H	R/W	TDACH	TPWE	1	TD13	TD12	TD11	TD10	TD9	TD8	40H
D4H	R/W	PWM7	PW7E	1	PW7V5	PW7V4	PW7V3	PW7V2	PW7V1	PW7V0	40H
D5H	R/W	PWM0	PW0E	1	PW0V5	PW0V4	PW0V3	PW0V2	PW0V1	PW0V0	40H
D6H	R/W	PWM1	PW1E	1	PW1V5	PW1V4	PW1V3	PW1V2	PW1V1	PW1V0	40H
D8H	R/W	S1CON	CR2	ENSI	STA	STO	SI	AA	CR1	CR0	00H
D9H	R	S1STA	STAT4	STAT3	STAT2	STAT1	STAT0	0	0	0	F8H
DAH	R/W	S1DAT	DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0	00H
DBH	R/W	S1ADR	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	GC	00H
DCH	R/W	PWM3	PW3E	1	PW3V5	PW3V4	PW3V3	PW3V2	PW3V1	PW3V0	40H
DDH	R/W	PWM4	PW4E	1	PW4V5	PW4V4	PW4V3	PW4V2	PW4V1	PW4V0	40H
DEH	R/W	PWM5	PW5E	1	PW5V5	PW5V4	PW5V3	PW5V2	PW5V1	PW5V0	40H
DFH	R/W	PWM6	PW6E	1	PW6V5	PW6V4	PW6V3	PW6V2	PW6V1	PW6V0	40H
E0H	R/W	ACC	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0	00H
E4H	R/W	PWM2	PW2E	1	PW2V5	PW2V4	PW2V3	PW2V2	PW2V1	PW2V0	40H
E8H	R/W	SAD	VHI	CH1	CH0	ST	SAD7	SAD6	SAD5	SAD4	00H
F0H	R/W	B	B7	B6	B5	B4	B3	B2	B1	B0	00H
F8H	R/W	TXT13	VPS RECEIVED	PAGE CLEARING	525 DISPLAY	525 TEXT	625 TEXT	PKT 8/30	FASTEXT	0	XXXX XXX0
FAH	R/W	XRAMP	XRAMP7	XRAMP6	XRAMP5	XRAMP4	XRAMP3	XRAMP2	XRAMP1	XRAMP0	00H
FBH	R/W	ROMBK	STANDBY	0	0	0	0	0	(reserved) 0	(reserved) 0	00H
FEH	W	WDTKEY	WKEY7	WKEY6	WKEY5	WKEY4	WKEY3	WKEY2	WKEY1	WKEY0	00H
FFH	R/W	WDT	WDV7	WDV6	WDV5	WDV4	WDV3	WDV2	WDV1	WDV0	00H

Table 3 SFR bit description

BIT	FUNCTION
Accumulator (ACC)	
ACC7 to ACC0	accumulator value
B Register (B)	
B7 to B0	B register value
Data Pointer High byte (DPH)	
DPH7 to DPH0	data pointer high byte, used with DPL to address auxiliary memory
Data Pointer Low byte (DPL)	
DPL7 to DPL0	data pointer low byte, used with DPH to address auxiliary memory
Interrupt Enable Register (IE)	
EA	disable all interrupts (logic 0), or use individual interrupt enable bits (logic 1)
EBUSY	enable BUSY interrupt
ES2	enable I^2C-bus interrupt
ET1	enable Timer 1 interrupt
EX1	enable external interrupt 1
ET0	enable Timer 0 interrupt
EX0	enable external interrupt 0
Interrupt Priority Register (IP)	
PBUSY	priority EBUSY interrupt
PES2	priority ES2 interrupt
PCC	priority ECC interrupt
PT1	priority Timer 1 interrupt
PX1	priority external interrupt 1
PT0	priority Timer 0 interrupt
PX0	priority external interrupt 0
Port 0 (P0)	
P07 to P00	Port 0 I/O register connected to external pins
Port 1 (P1)	
P17 to P10	Port 1 I/O register connected to external pins
Port 2 (P2)	
P27 to P20	Port 2 I/O register connected to external pins
Port 3 (P3)	
P37 to P30	Port 3 I/O register connected to external pins; P37 to P35 are only available with the LQFP100 package

BIT	FUNCTION
Port 0 Configuration A (P0CFGA) and Port 0 Configuration B (P0CFGB)	
P0CFGA<7:0> and P0CFGB<7:0>	These two registers are used to configure Port 0 pins. For example, the configuration of Port 0 pin 3 is controlled by setting bit 3 in both P0CFGA and P0CFGB. P0CFGB<x>/P0CFGA<x>: 00 = P0.x in open-drain configuration 01 = P0.x in quasi-bidirectional configuration 10 = P0.x in high-impedance configuration 11 = P0.x in push-pull configuration
Port 1 Configuration A (P1CFGA) and Port 1 Configuration B (P1CFGB)	
P1CFGA<7:0> and P1CFGB<7:0>	These two registers are used to configure Port 1 pins. For example, the configuration of Port 1 pin 3 is controlled by setting bit 3 in both P1CFGA and P1CFGB. P1CFGB<x>/P1CFGA<x>: 00 = P1.x in open-drain configuration 01 = P1.x in quasi-bidirectional configuration 10 = P1.x in high-impedance configuration 11 = P1.x in push-pull configuration
Port 2 Configuration A (P2CFGA) and Port 2 Configuration B (P2CFGB)	
P2CFGA<7:0> and P2CFGB<7:0>	These two registers are used to configure Port 2 pins. For example, the configuration of Port 2 pin 3 is controlled by setting bit 3 in both P2CFGA and P2CFGB. P2CFGB<x>/P2CFGA<x>: 00 = P2.x in open-drain configuration 01 = P2.x in quasi-bidirectional configuration 10 = P2.x in high-impedance configuration 11 = P2.x in push-pull configuration
Port 3 Configuration A (P3CFGA) and Port 3 Configuration B (P3CFGB)	
P3CFGA<7:0> and P3CFGB<7:0>	These two registers are used to configure Port 3 pins. For example, the configuration of Port 3 pin 3 is controlled by setting bit 3 in both P3CFGA and P3CFGB. P3CFGB<x>/P3CFGA<x>: 00 = P3.x in open-drain configuration 01 = P3.x in quasi-bidirectional configuration 10 = P3.x in high-impedance configuration 11 = P3.x in push-pull configuration

BIT	FUNCTION
Power Control Register (PCON)	
ARD	auxiliary RAM disable bit, all MOVX instructions access the external data memory
RFI	disable ALE during internal access to reduce radio frequency interference
WLE	Watchdog Timer enable
GF1	general purpose flag 1
GF0	general purpose flag 0
PD	Power-down mode activation bit
IDL	Idle mode activation bit
Program Status Word (PSW)	
C	carry bit
AC	auxiliary carry bit
F0	flag 0
RS1 to RS0	register bank selector bits RS<1:0>: 00 = Bank 0 (00H to 07H) 01 = Bank 1 (08H to 0FH) 10 = Bank 2 (10H to 17H) 11 = Bank 3 (18H to 1FH)
OV	overflow flag
P	parity bit
Pulse Width Modulator 0 Control Register (PWM0)	
PW0E	activate this PWM and take control of respective port pin (logic 1)
PW0V5 to PW0V0	pulse width modulator high time
Pulse Width Modulator 1 Control Register (PWM1)	
PW1E	activate this PWM (logic 1)
PW1V5 to PW1V0	pulse width modulator high time
Pulse Width Modulator 2 Control Register (PWM2)	
PW2E	activate this PWM (logic 1)
PW2V5 to PW2V0	pulse width modulator high time
Pulse Width Modulator 3 Control Register (PWM3)	
PW3E	activate this PWM (logic 1)
PW3V5 to PW3V0	pulse width modulator high time
Pulse Width Modulator 4 Control Register (PWM4)	
PW4E	activate this PWM (logic 1)
PW4V5 to PW4V0	pulse width modulator high time

BIT	FUNCTION
Pulse Width Modulator 5 Control Register (PWM5)	
PW5E	activate this PWM (logic 1)
PW5V5 to PW5V0	pulse width modulator high time
Pulse Width Modulator 6 Control Register (PWM6)	
PW6E	activate this PWM (logic 1)
PW6V5 to PW6V0	pulse width modulator high time
Pulse Width Modulator 7 Control Register (PWM7)	
PW7E	activate this PWM (logic 1)
PW7V5 to PW7V0	pulse width modulator high time
ROM Bank (ROMBK)	
STANDBY	standby activation bit
I^2C-bus Slave Address Register (S1ADR)	
ADR6 to ADR0	I^2C-bus slave address to which the device will respond
GC	enable I^2C-bus general call address (logic 1)
I^2C-bus Control Register (S1CON)	
CR2 to CR0	clock rate bits; CR<2:0>: 000 = 100 kHz bit rate 001 = 3.75 kHz bit rate 010 = 150 kHz bit rate 011 = 200 kHz bit rate 100 = 25 kHz bit rate 101 = 1.875 kHz bit rate 110 = 37.5 kHz bit rate 111 = 50 kHz bit rate
ENSI	enable I^2C-bus interface (logic 1)
STA	**START flag.** When this bit is set in slave mode, the hardware checks the I^2C-bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode it will generate a repeated START condition.
STO	**STOP flag.** If this bit is set in a master mode a STOP condition is generated. A STOP condition detected on the I^2C-bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. In this case no STOP condition is generated to the I^2C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected receiver mode. The STOP flag is cleared by the hardware.

BIT	FUNCTION
SI	**Serial Interrupt flag.** This flag is set and an interrupt request is generated, after any of the following events occur: • A START condition is generated in master mode • The own slave address has been received during AA = 1 • The general call address has been received while S1ADR.GC and AA = 1 • A data byte has been received or transmitted in master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A STOP or START condition is received as selected slave receiver or transmitter. While the SI flag is set, SCL remains LOW and the serial transfer is suspended. SI must be reset by software.
AA	**Assert Acknowledge flag.** When this bit is set, an acknowledge is returned after any one of the following conditions: • Own slave address is received • General call address is received (S1ADR.GC = 1) • A data byte is received, while the device is programmed to be a master receiver • A data byte is received, while the device is selected slave receiver. When the bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.
I^2C-bus Data Register (S1DAT)	
DAT7 to DAT0	I^2C-bus data
I^2C-bus Status Register (S1STA)	
STAT4 to STAT0	I^2C-bus interface status
Software ADC Register (SAD)	
VHI	analog input voltage greater than DAC voltage (logic 1)
CH1 to CH0	ADC input channel select bits; CH<1:0>: 00 = ADC3 01 = ADC0 10 = ADC1 11 = ADC2
ST(1)	initiate voltage comparison between ADC input channel and SAD value
SAD7 to SAD4	4 MSBs of DAC input word
Software ADC Control Register (SADB)	
DC_COMP	enable DC comparator mode (logic 1)
SAD3 to SAD0	4 LSBs of SAD value
Stack Pointer (SP)	
SP7 to SP0	stack pointer value

BIT	FUNCTION
Timer/Counter Control Register (TCON)	
TF1	**Timer 1 overflow flag.** Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	**Timer 1 run control bit.** Set/cleared by software to turn timer/counter on/off.
TF0	**Timer 0 overflow flag.** Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR0	**Timer 0 run control bit.** Set/cleared by software to turn timer/counter on/off.
IE1	**Interrupt 1 Edge flag.** Both edges generate flag. Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt processed.
IT1	**Interrupt 1 type control bit.** Set/cleared by software to specify edge/LOW level triggered external interrupts.
IE0	**Interrupt 0 Edge I flag.** Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt processed.
IT0	**Interrupt 0 type flag.** Set/cleared by software to specify falling edge/LOW level triggered external interrupts.
14-bit PWM MSB Register (TDACH)	
TPWE	activate this 14-bit PWM (logic 1)
TD13 to TD8	6 MSBs of 14-bit number to be output by the 14-bit PWM
14-bit PWM LSB Register (TDACL)	
TD7 to TD0	8 LSBs of 14-bit number to be output by the 14-bit PWM
Timer 0 High byte (TH0)	
TH07 to TH00	8 MSBs of Timer 0 16-bit counter
Timer 1 High byte (TH1)	
TH17 to TH10	8 MSBs of Timer 1 16-bit counter
Timer 0 Low byte (TL0)	
TL07 to TL00	8 LSBs of Timer 0 16-bit counter
Timer 1 Low byte (TL1)	
TL17 to TL10	8 LSBs of Timer 1 16-bit counter
Timer/Counter Mode Control (TMOD)	
GATE	gating control Timer/Counter 1
C/$\overline{T}$	Counter/Timer 1 selector
M1 to M0	mode control bits timer/counter 1; M<1:0>: 00 = 8-bit timer or 8-bit counter with divide-by-32 prescaler 01 = 16-bit time interval or event counter 10 = 8-bit time interval or event counter with automatic reload upon overflow; reload value stored in TH1 11 = stopped
GATE	Gating control Timer/Counter 0
C/$\overline{T}$	Counter/Timer 0 selector

BIT	FUNCTION
M1 to M0	mode control bits timer/counter 0; M<1:0>: 00 = 8-bit timer or 8-bit counter with divide-by-32 prescaler 01 = 16-bit time interval or event counter 10 = 8-bit time interval or event counter with automatic reload upon overflow; reload value stored in TH0 11 = one 8-bit time interval or event counter and one 8-bit time interval counter
Text Register 0 (TXT0)	
X24 POSN	store packet 24 in extension packet memory (logic 0) or page memory (logic 1)
DISPLAY X24	display X24 from page memory (logic 0) or extension packet memory (logic 1)
AUTO FRAME	FRAME output switched off automatically if any video displayed (logic 1)
DISABLE HEADER ROLL	disable writing of rolling headers and time into memory (logic 1)
DISPLAY STATUS ROW ONLY	display row 24 only (logic 1)
DISABLE FRAME	FRAME output always LOW (logic 1)
VPS ON	enable capture of VPS data (logic 1)
INV ON	enable capture of inventory page in block 8 (logic 1)
Text Register 1 (TXT1)	
EXT PKT OFF	disable acquisition of extension packets (logic 1)
8-BIT	disable checking of packets 0 to 24 written into memory (logic 1)
ACQ OFF	disable writing of data into Display memory (logic 1)
X26 OFF	disable automatic processing of X/26 data (logic 1)
FULL FIELD	acquire data on any TV line (logic 1)
FIELD POLARITY	VSYNC pulse in second half of line during even field (logic 1)
H POLARITY	HSYNC reference edge is negative going (logic 1)
V POLARITY	VSYNC reference edge is negative going (logic 1)
Text Register 2 (TXT2)	
ACQ BANK	select acquisition Bank 1 (logic 1)
REQ3 to REQ0	page request
SC2 to SC0	start column of page request
Text Register 3 (TXT3)	
PRD4 to PRD0	page request data
Text Register 4 (TXT4)	
OSD BANK ENABLE	alternate OSD location available via graphic attribute, additional 32 locations (logic 1)
QUAD WIDTH ENABLE	enable display of quadruple width characters (logic 1)
EAST/$\overline{\text{WEST}}$	eastern language selection of character codes A0H to FFH (logic 1)
DISABLE DOUBLE HEIGHT	disable normal decoding of double height characters (logic 1)
B MESH ENABLE	enable meshing of black background (logic 1)
C MESH ENABLE	enable meshing of coloured background (logic 1)
TRANS ENABLE	display black background as video (logic 1)
SHADOW ENABLE	display shadow/fringe (default SE black) (logic 1)

BIT	FUNCTION
Text Register 5 (TXT5)	
BKGND OUT	background colour displayed outside teletext boxes (logic 1)
BKGND IN	background colour displayed inside teletext boxes (logic 1)
$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ active outside teletext and OSD boxes (logic 1)
$\overline{\text{COR}}$ IN	$\overline{\text{COR}}$ active inside teletext and OSD boxes (logic 1)
TEXT OUT	text displayed outside teletext boxes (logic 1)
TEXT IN	text displayed inside teletext boxes (logic 1)
PICTURE ON OUT	video displayed outside teletext boxes (logic 1)
PICTURE ON IN	video displayed inside teletext boxes (logic 1)
Text Register 6 (TXT6)	
BKGND OUT	background colour displayed outside teletext boxes (logic 1)
BKGND IN	background colour displayed inside teletext boxes (logic 1)
$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ active outside teletext and OSD boxes (logic 1)
$\overline{\text{COR}}$ IN	$\overline{\text{COR}}$ active inside teletext and OSD boxes (logic 1)
TEXT OUT	text displayed outside teletext boxes (logic 1)
TEXT IN	text displayed inside teletext boxes (logic 1)
PICTURE ON OUT	video displayed outside teletext boxes (logic 1)
PICTURE ON IN	video displayed inside teletext boxes (logic 1)
Text Register 7 (TXT7)	
STATUS ROW TOP	display memory row 24 information above teletext page (on display row 0) (logic 1)
CURSOR ON	display cursor at position given by TXT9 and TXT10 (logic 1)
REVEAL	display characters in area with conceal attribute set (logic 1)
BOTTOM/$\overline{\text{TOP}}$	display memory rows 12 to 23 when DOUBLE HEIGHT height bit is set (logic 1)
DOUBLE HEIGHT	display each character as twice normal height (logic 1)
BOX ON 24	enable display of teletext boxes in memory row 24 (logic 1)
BOX ON 1 to 23	enable display of teletext boxes in memory row 1 to 23 (logic 1)
BOX ON 0	enable display of teletext boxes in memory row 0 (logic 1)
Text Register 8 (TXT8)	
$\overline{\text{FLICKER STOP ON}}$	disable ‘Flicker Stopper’ circuitry (logic 1)
DISABLE SPANISH	disable special treatment of Spanish packet 26 characters (logic 1)
PKT 26 RECEIVED[2]	packet 26 data has been processed (logic 1)
WSS RECEIVED[2]	WSS data has been processed (logic 1)
WSS ON	enable acquisition of WSS data (logic 1)
CVBS1/$\overline{\text{CVBS0}}$	select CVBS1 as source for device (logic 1)

BIT	FUNCTION
Text Register 9 (TXT9)	
CURSOR FREEZE	lock cursor at current position (logic 1)
CLEAR MEMORY(1)	clear memory block pointed to by TXT15 (logic 1)
A0	access extension packet memory (logic 1)
R4 to R0(3)	current memory row value
Text Register 10 (TXT10)	
C5 to C0(4)	current memory column value
Text Register 11 (TXT11)	
D7 to D0	data value written or read from memory location defined by TXT9, TXT10 and TXT15
Text Register 12 (TXT12)	
625/525 SYNC	525-line CVBS signal is being received (logic 1)
SPANISH	Spanish character set present (logic 1)
ROM VER3 to ROM VER0	mask programmable identification for character set
VIDEO SIGNAL QUALITY	acquisition can be synchronized to CVBS (logic 1)
Text Register 13 (TXT13)	
VPS RECEIVED	VPS data (logic 1)
PAGE CLEARING	software or power-on page clear in progress (logic 1)
525 DISPLAY	525-line synchronisation for display (logic 1)
525 TEXT	525-line WST being received (logic 1)
625 TEXT	625-line WST being received (logic 1)
PKT 8/30	packet 8/30/x(625) or packet 4/30/x(525) data detected (logic 1)
FASTEXT	packet x/27 data detected (logic 1)
Text Register 14 (TXT14)	
PAGE3 to PAGE0	current display page
Text Register 15 (TXT15)	
BLOCK3 to BLOCK0	current micro block to be accessed by TXT9, TXT10 and TXT11
Text Register 17 (TXT17)	
FORCE ACQ1 to FORCE ACQ0	FORCE ACQ<1:0>: 00 = automatic selection 01 = force 525 timing, force 525 teletext standard 10 = force 625 timing, force 625 teletext standard 11 = force 625 timing, force 525 teletext standard
FORCE DISP1 to FORCE DISP0	FORCE DISP<1:0>: 00 = automatic selection 01 = force display to 525 mode (9 lines per row) 10 = force display to 625 mode (10 lines per row) 11 = not valid (default to 625 mode)

BIT	FUNCTION
SCREEN COL2 to SCREEN COL0	Defines colour to be displayed instead of TV picture and black background; these bits are equivalent to the RGB components. SCREEN COL<2:0>: 000 = transparent 001 = CLUT entry 9 010 = CLUT entry 10 011 = CLUT entry 11 100 = CLUT entry 12 101 = CLUT entry 13 110 = CLUT entry 14 111 = CLUT entry 15
Text Register 18 (TXT18)	
NOT3 to NOT0	national option table selection, maximum of 31 when used with EAST/$\overline{\text{WEST}}$ bit
BS1 to BS0	basic character set selection
Text Register 19 (TXT19)	
TEN	enable twist character set (logic 1)
TC2 to TC0	language control bits (C12, C13 and C14) that has twisted character set
TS1 to TS0	twist character set selection
Text Register 20 (TXT20)	
OSD LANG ENABLE	enable use of OSD LAN<2:0> to define language option for display, instead of C12, C13 and C14
OSD LAN2 to OSD LAN0	alternative C12, C13 and C14 bits for use with OSD menus
Text Register 21 (TXT21)	
I^2C PORT 1	enable I^2C-bus Port 1 selection (P1.5/SDA1 and P1.4/SCL1) (logic 1)
I^2C PORT 0	enable I^2C-bus Port 0 selection (P1.7/SDA0 and P1.6/SCL0) (logic 1)
Text Register 22 (TXT22)	
GPF7 to GPF6	reserved
GPF5	standard device (logic 0)
GPF4	10 pages available (logic 1)
GPF3	PWM0, PWM1, PWM2 and PWM3 outputs routed to Port 2.1 to Port 2.4 respectively (logic 1)
GPF2	reserved
GPF1	text acquisition available (logic 1)
GPF0	reserved
Watchdog Timer (WDT)	
WDV7 to WDV0	Watchdog Timer period

BIT	FUNCTION
Watchdog Timer Key (WDTKEY)	
WKEY7 to WKEY0[5]	Watchdog Timer Key
Wide Screen Signalling 1 (WSS1)	
WSS<3:0> ERROR	error in WSS<3:0> (logic 1)
WSS3 to WSS0	signalling bits to define aspect ratio (group 1)
Wide Screen Signalling 2 (WSS2)	
WSS<7:4> ERROR	error in WSS<7:4> (logic 1)
WSS7 to WSS4	signalling bits to define enhanced services (group 2)
Wide Screen Signalling 3 (WSS3)	
WSS<13:11> ERROR	error in WSS<13:11> (logic 1)
WSS13 to WSS11	signalling bits to define reserved elements (group 4)
WSS<10:8> ERROR	error in WSS<10:8> (logic 1)
WSS10 to WSS8	signalling bits to define subtitles (group 3)
XRAMP	
XRAMP7 to XRAMP0	internal RAM access upper byte address

Notes

1. This flag is set by software and reset by hardware.
2. This flag is set by hardware and must be reset by software.
3. Valid range TXT mode 0 to 24.
4. Valid range TXT mode 0 to 39.
5. Must be set to 55H to disable Watchdog Timer when active.

8.5 Character set feature bits

Features available on the SAA55xx devices are reflected in a specific area of the character ROM. These sections of the character ROM are mapped to two Special Function Registers: TXT22 and TXT12. Character ROM address 09FEH is mapped to SFR TXT22 as shown in Table 4. Character ROM address 09FFH is mapped to SFR TXT12 as shown in Table 6.

Table 4 Character ROM - TXT22 mapping

U = used; X = reserved

MAPPED ITEMS	11	10	9	8	7	6	5	4	3	2	1	0
Character ROM address 09FEH	X	X	X	X	X	X	U	U	U	X	U	X
Mapped to TXT22	–	–	–	–	7	6	5	4	3	2	1	0

Table 5 Description of Character ROM address 09FEH bits

BIT NUMBER	FUNCTION
0	reserved; normally set to logic 1
1	1 = Text Acquisition available 0 = Text Acquisition not available
2	reserved
3	1 = PWM0, PWM1, PWM2 and PWM3 output routed to Port 2.1 to Port 2.4 respectively 0 = PWM0, PWM1, PWM2 and PWM3 output routed to Port 3.0 to Port 3.3 respectively
4	1 = 10 page available 0 = 6 page available
5	0 = standard device
6 to 11	reserved; normally set to logic 1

Table 6 Character ROM - TXT12 mapping

U = used; X = reserved

MAPPED ITEMS	11	10	9	8	7	6	5	4	3	2	1	0
Character ROM address 09FFH	X	X	X	X	X	X	X	U	X	X	X	X
Mapped to TXT12	–	–	–	–	–	–	–	6	5	4	3	2

Table 7 Description of Character ROM address 09FFH bits

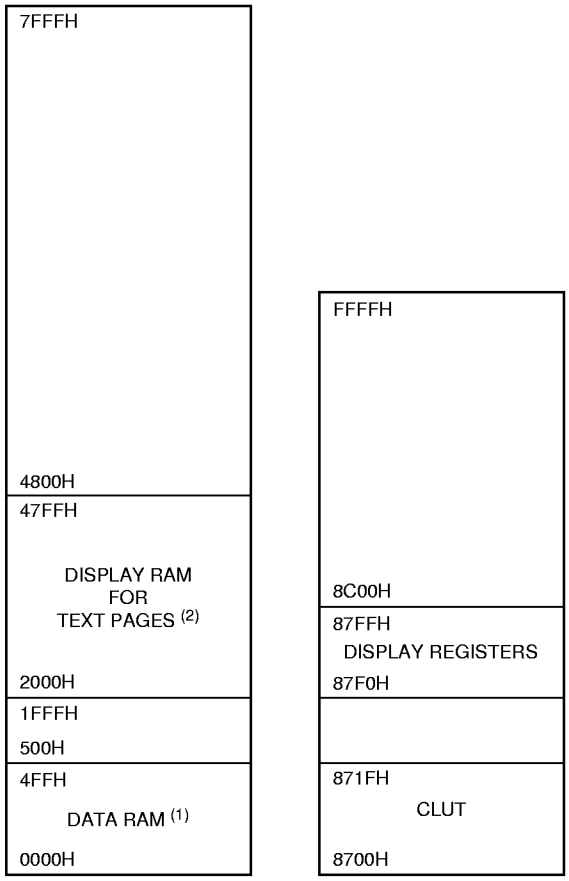
BIT NUMBER	FUNCTION
4	1 = Spanish character set present 0 = no Spanish character set present
0 to 3, 5 to 11	reserved; normally set to logic 1

8.6 External (auxiliary) memory

The normal 80C51 external memory area has been mapped internally to the device, this means that the MOVX instruction accesses memory internal to the device.

8.6.1 AUXILIARY RAM PAGE SELECTION

The Auxiliary RAM page pointer is used to select one of the 256 pages within the Auxiliary RAM, not all pages are allocated, refer to Fig.10 for further detail. A page consists of 256 consecutive bytes.



(1) Amount of Data RAM depends on the device.
(2) Amount of Display RAM depends on the device.

Fig.9 Auxiliary RAM allocation.

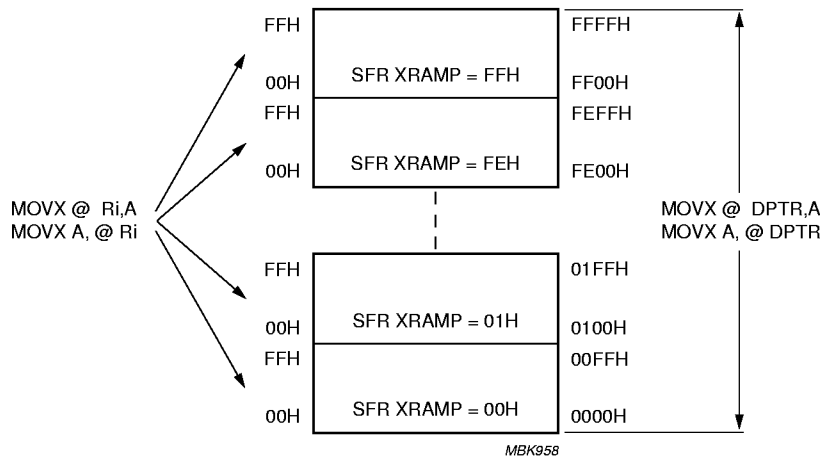


Fig.10 Indirect addressing of Auxiliary RAM.

9 POWER-ON RESET

An automatic reset can be obtained when V_{DD} is turned on by connecting the RESET pin to V_{DDP} through a 10 µF capacitor, providing the V_{DD} rise time does not exceed 1 ms, and the oscillator start-up time does not exceed 10 ms.

To ensure correct initialisation, the RESET pin must be held high long enough for the oscillator to settle following power-up, usually a few ms. Once the oscillator is stable, a further 24 clocks are required to generate the reset (two machine cycles of the microcontroller). Once the above reset condition has been detected an internal reset signal is triggered which remains active for 2048 clock cycles.

10 REDUCED POWER MODES

There are two power saving modes, Idle and Power-down, incorporated into the 10 page devices. There is an additional Standby mode incorporated into the 1 page devices. When utilizing any mode, power to the device (V_{DDP}, V_{DDC} and V_{DDA}) should be maintained, since power saving is achieved by clock gating on a section by section basis.

10.1 Idle mode

During Idle mode, Acquisition, Display and the Central Processing Unit (CPU) sections of the device are disabled. The following functions remain active:

- Memory interface
- I²C-bus interface
- Timer/Counters
- Watchdog Timer
- Pulse Width Modulators.

To enter Idle mode the IDL bit in the PCON register must be set. The Watchdog Timer must be disabled prior to entering the Idle mode to prevent the device being reset. Once in Idle mode, the crystal oscillator continues to run, but the internal clock to the CPU, Acquisition and Display are gated out. However, the clocks to the Memory interface, I²C-bus interface, Timer/Counters, Watchdog Timer and Pulse Width Modulators are maintained. The CPU state is frozen along with the status of all SFRs, internal RAM contents are maintained, as are the device output pin values.

Since the output values on Red Green Blue (RGB) and the Video Data Switch (VDS) are maintained the display output must be disabled before entering this mode.

There are three methods to recover from Idle mode:

- Assertion of an enabled interrupt will cause the IDL bit to be cleared by hardware, thus terminating Idle mode. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Idle mode.
- A second method of exiting the Idle mode is via an interrupt generated by the SAD DC Compare circuit. When the device is configured in this mode, detection of an analog threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into Idle mode.
- The third method of terminating Idle mode is with an external hardware reset. Since the oscillator is running, the hardware reset need only be active for two machine cycles (24 clocks at 12 MHz) to complete the reset operation. Reset defines all SFRs and Display memory to an initialized state, but maintains all other RAM values. Code execution commences with the Program Counter set to '0000'.

10.2 Power-down mode

In Power-down mode the crystal oscillator is stopped. The contents of all SFRs and Data memory are maintained, However, the contents of the Auxiliary/Display memory are lost. The port pins maintain the values defined by their associated SFRs. Since the output values on RGB and VDS are maintained the display output must be made inactive before entering Power-down mode.

The Power-down mode is activated by setting the PD bit in the PCON register. It is advised to disable the Watchdog Timer prior to entering power-down.

There are three methods of exiting power-down:

- An external interrupt provides the first mechanism for waking from power-down. Since the clock is stopped, external interrupts needs to be set level sensitive prior to entering power-down. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Power-down mode.
- A second method of exiting power-down is via an interrupt generated by the SAD DC Compare circuit. When the device is configured in this mode, detection of a certain analog threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into power-down.
- The third method of terminating the Power-down mode is with an external hardware reset. Reset defines all SFRs and Display memory, but maintains all other RAM values. Code execution commences with the Program Counter set to '0000'.

10.3 Standby mode

This mode is only available on 1 page devices. When Standby mode is entered both Acquisition and Display sections are disabled. The following functions remain active:

- 80C51 core
- Memory interface
- I^2C-bus interface
- Timer/Counters
- Watchdog Timer
- Software ADC
- Pulse Width Modulators.

To enter Standby mode, the STANDBY control bit in the ROMBK SFR (bit 7) must be set. It can be used in conjunction with either Idle or Power-down modes to switch between power saving modes. This mode enables the 80C51 core to decode either IR remote commands or receive I^2C-bus commands without the device being fully powered.

The Standby state is maintained upon exit from either the Idle mode or Power-down mode. No wake-up from Standby is necessary as the 80C51 core remains operational.

Since the output values on RGB and VDS are maintained the display output must be disabled before entering this mode.

11 I/O FACILITY

11.1 I/O ports

The SAA55xx devices have 29 I/O lines, each is individually addressable, or form three parallel 8-bit addressable ports which are Port 0, Port 1 and Port 2. Port 3 has 5-bit parallel I/O only.

11.2 Port type

All individual ports can be programmed to function in one of four I/O configurations: open-drain, quasi-bidirectional, high-impedance and push-pull. The I/O configuration is selected using two associated Port Configuration Registers: PnCFGA and PnCFGB (where n = port number 0, 1, 2 or 3); see Table 3.

11.2.1 OPEN-DRAIN

The open-drain configuration can be used for bidirectional operation of a port. It requires an external pull-up resistor, the pull-up voltage has a maximum value of 5.5 V, to allow connection of the device into a 5 V environment.

The I^2C-bus ports (P1.4,P1.5, P1.6 and P1.7) can only be configured as open-drain.

11.2.2 QUASI-BIDIRECTIONAL

The quasi-bidirectional configuration is a combination of open-drain and push-pull. It requires an external pull-up resistor to V_{DDP} (nominally 3.3 V). When a signal transition from LOW-to-HIGH is output from the device, the pad is put into push-pull configuration for one clock cycle (166 ns) after which the pad goes into open-drain configuration. This configuration is used to speed up the edges of signal transitions. This is the default mode of operation of the pads after reset.

11.2.3 HIGH-IMPEDANCE

The high-impedance configuration can be used for input only operation of the port. When using this configuration the two output transistors are turned off.

11.2.4 PUSH-PULL

The push-pull configuration can be used for output only. In this mode the signal is driven to either 0 V or V_{DDP}, which is nominally 3.3 V.

11.3 Port alternate functions

Ports 1, 2 and 3 are shared with alternative functions to enable control of external devices and circuitry.
The alternative functions are enabled by setting the appropriate SFR and also writing a logic 1 to the port bit that the function occupies.

11.4 LED support

Port pins P0.5 and P0.6 have a 8 mA current sinking capability to enable LEDs in series with current limiting resistors to be driven directly, without the need for additional buffering circuitry.

12 INTERRUPT SYSTEM

The device has six interrupt sources, each of which can be enabled or disabled. When enabled each interrupt can be assigned one of two priority levels. There are four interrupts that are common to the 80C51, two of these are external interrupts (EX0 and EX1) and the other two are timer interrupts (ET0 and ET1). In addition to the conventional 80C51 interrupts, one application specific interrupt is incorporated internal to the device which has following functionality:

- **Display Busy interrupt (EBUSY).** An interrupt is generated when the display enters either a Horizontal or Vertical Blanking Period. i.e. Indicates when the microcontroller can update the Display RAM without causing undesired effects on the screen. This interrupt can be configured in one of two modes using the Memory Mapped Register (MMR) Configuration (address 87FFH, bit TXT/V):
  - Text Display Busy. An interrupt is generated on each active horizontal display line when the Horizontal Blanking Period is entered
  - Vertical Display Busy. An interrupt is generated on each vertical display field when the Vertical Blanking Period is entered.

12.1 Interrupt enable structure

Each of the individual interrupts can be enabled or disabled by setting or clearing the relevant bit in the Interrupt Enable Register (IE). All interrupt sources can also be globally disabled by clearing the EA bit (IE.7).

12.2 Interrupt enable priority

Each interrupt source can be assigned one of two priority levels. The interrupt priorities are defined by the Interrupt Priority Register (IP). A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt can not be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request with the highest priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level there is a second priority structure determined by the polling sequence as defined in Table 8.

Table 8 Interrupt priority (within same level)

SOURCE	PRIORITY WITHIN LEVEL	INTERRUPT VECTOR
EX0	highest	0003H
ET0	–	000BH
EX1	–	0013H
ET1	–	001BH
ES2	–	002BH
EBUSY	lowest	0033H

12.3 Interrupt vector address

The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate servicing routine. The interrupt vector addresses for each source are shown in Table 8.

12.4 Level/edge interrupt

The external interrupt can be programmed to be either level-activated or transition-activated by setting or clearing the IT0/IT1 bits in the Timer Control SFR (TCON).

Table 9 External interrupt activation

ITx	LEVEL	EDGE
0	active LOW	–
1	–	INT0 = negative edge
		INTI = positive and negative edge

The external interrupt INT1 differs from the standard 80C51 interrupt in that it is activated on both edges when in edge sensitive mode. This is to allow software pulse width measurement for handling remote control inputs.

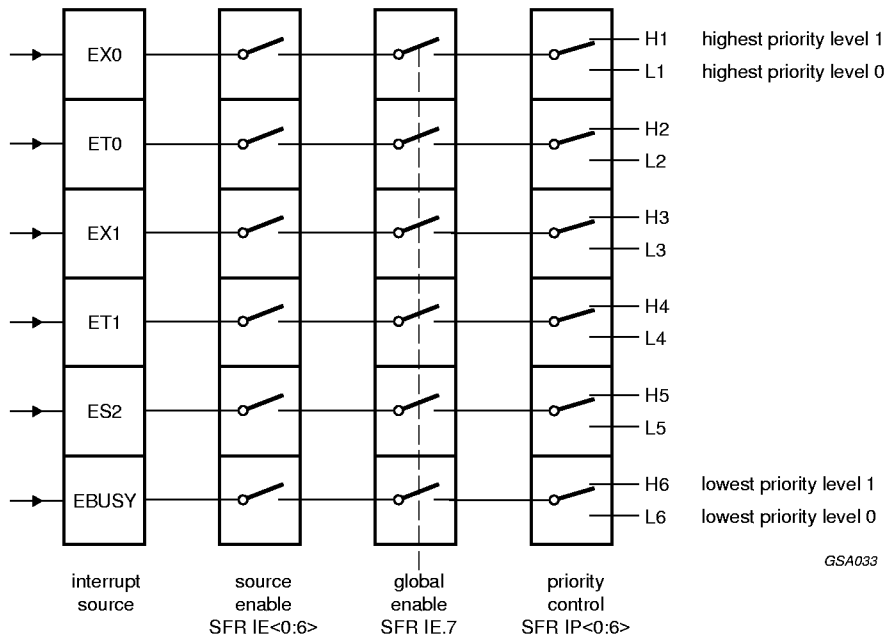


Fig.11 Interrupt structure.

13 TIMER/COUNTER

Two 16-bit timers/counters are incorporated Timer 0 and Timer 1. Both can be configured to operate as either timers or event counters.

In Timer mode, the register is incremented on every machine cycle. It is therefore counting machine cycles. Since the machine cycle consists of twelve oscillator periods, the count rate is $^1/_{12}f_{osc}$ = 1 MHz.

In Counter mode, the register is incremented in response to a negative transition at its corresponding external pin T0 or T1. Since the pins T0 and T1 are sampled once per machine cycle, it takes two machine cycles to recognise a transition, this gives a maximum count rate of $^1/_{24}f_{osc}$ = 0.5 MHz.

There are six Special Function Registers used to control the timers/counters. These are: TCON, TMOD, TL0, TH0, TL1 and TH1.

The timer/counter function is selected by control bits C/$\overline{T}$ in the Timer Mode SFR (TMOD). These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1 and M0) in TMOD. Detail of the modes of operation is given in *"Handbook IC20, 80C51-Based 8-bit Microcontrollers"*.

TL0 and TH0 are the actual Timer/Counter registers for Timer 0. TL0 is the low byte and TH0 is the high byte. TL1 and TH1 are the actual Timer/Counter registers for Timer 1. TL1 is the low byte and TH1 is the high byte.

14 WATCHDOG TIMER

The Watchdog Timer is a counter that once in an overflow state forces the microcontroller into a reset condition. The purpose of the Watchdog Timer is to reset the microcontroller if it enters an erroneous processor state (possibly caused by electrical noise or RFI) within a reasonable period of time. When enabled, the Watchdog circuitry will generate a system reset if the user program fails to reload the Watchdog Timer within a specified length of time known as the Watchdog Interval (WI).

The Watchdog Timer consists of an 8-bit counter with an 11-bit prescaler. The prescaler is fed with a signal whose frequency is $^1/_{12}f_{osc}$ (1 MHz for 12 MHz oscillator).

The 8-bit timer is incremented every 't' seconds where:

$$t = 12 \times 2048 \times \frac{1}{f_{osc}} = 12 \times 2048 \times \frac{1}{12 \times 10^6} = 2.048 \text{ ms}$$

14.1 Watchdog Timer operation

The Watchdog operation is activated when the WLE bit in the Power Control SFR (PCON) is set. The Watchdog can be disabled by software by loading the value 55H into the Watchdog Key SFR (WDTKEY). This must be performed before entering Idle or Power-down mode to prevent exiting the mode prematurely.

Once activated the Watchdog Timer SFR (WDT) must be reloaded before the timer overflows. The WLE bit must be set to enable loading of the WDT SFR, once loaded the WLE bit is reset by hardware, this is to prevent erroneous software from loading the WDT SFR.

The value loaded into the WDT defines the Watchdog Interval (WI).

$$WI = (256 - WDT) \times t = (256 - WDT) \times 2.048 \text{ ms}$$

The range of intervals is from WDT = 00H which gives 524 ms to WDT = FFH which gives 2.048 ms.

15 PULSE WIDTH MODULATORS

The device has eight 6-bit Pulse Width Modulated (PWM) outputs for analog control of e.g. volume, balance, bass, treble, brightness, contrast, hue and saturation. The PWM outputs generate pulse patterns with a repetition rate of 21.33 μs, with the high time equal to the PWM SFR value multiplied by 0.33 μs. The analog value is determined by the ratio of the high time to the repetition time, a DC voltage proportional to the PWM setting is obtained by means of an external integration network (low-pass filter).

15.1 PWM control

The relevant PWM is enabled by setting the PWM enable bit PWxE in the PWMx Control Register (where x = 0 to 7). The high time is defined by the value PWxV<5:0>.

15.2 Tuning Pulse Width Modulator (TPWM)

The device has a single 14-bit PWM that can be used for Voltage Synthesis Tuning. The method of operation is similar to the normal PWM except the repetition period is 42.66 μs.

15.2.1 TPWM CONTROL

Two SFRs are used to control the TPWM, they are TDACL and TDACH. The TPWM is enabled by setting the TPWE bit in the TDACH SFR. The most significant bits TD<13:7> alter the high period between 0 and 42.33 μs. The 7 least significant bits TD<6:0> extend certain pulses by a further 0.33 μs, e.g. if TD<6:0> = 01H then 1 in 128 periods will be extended by 0.33 μs, if TD<6:0> = 02H then 2 in 128 periods will be extended.

The TPWM will not start to output a new value until TDACH has been written to. Therefore, if the value is to be changed, TDACL should be written before TDACH.

15.3 Software ADC (SAD)

Four successive approximation Analog-to-Digital Converters can be implemented in software by making use of the on-board 8-bit Digital-to-Analog Converter and Analog Comparator.

15.3.1 SAD CONTROL

The control of the required analog input is done using the channel select bits CH<1:0> in the SAD SFR, this selects the required analog input to be passed to one of the inputs of the comparator. The second comparator input is generated by the DAC whose value is set by the bits SAD<7:0> in the SAD and SADB SFRs. A comparison between the two inputs is made when the start compare bit ST in the SAD SFR is set, this must be at least one instruction cycle after the SAD<7:0> value has been set. The result of the comparison is given on VHI one instruction cycle after the setting of ST.

15.3.2 SAD INPUT VOLTAGE

The external analog voltage that is used for comparison with the internally generated DAC voltage does not have the same voltage range. The DAC has a lower reference level of V_{SSA} and an upper reference level of V_{SSP}.

The resolution of the DAC voltage with a nominal value is $^{3.3}/_{256} \approx 13$ mV. The external analog voltage has a lower value equivalent to V_{SSA} and an upper value equivalent to $V_{DDP} - V_{tn}$, where V_{tn} is the threshold voltage for an N type Metal Oxide Semiconductor transistor. The reason for this is that the input pins for the analog signals (P3.0 to P3.3) are 5 V tolerant for normal port operations, i.e. when not used as analog input. To protect the analog multiplexer and comparator circuitry from the 5 V, a series transistor is used to limit the voltage. This limiting introduces a voltage drop equivalent to V_{tn} (≈0.6 V) on the input voltage. Therefore, for an input voltage in the range V_{DDP} to $V_{DDP} - V_{tn}$ the SAD returns the same comparison value.

15.3.3 SAD DC COMPARATOR MODE

The SAD module incorporates a DC Comparator mode which is selected using the DC_COMP control bit in the SADB SFR. This mode enables the microcontroller to detect a threshold crossing at the input to the selected analog input pin (P3.0/ADC0, P3.1/ADC1, P3.2/ADC2 or P3.3/ADC3) of the Software ADC. A level sensitive interrupt is generated when the analog input voltage level at the pin falls below the analog output level of the SAD DAC.

This mode is intended to provide the device with a wake-up mechanism from Power-down or Idle mode when a key-press on the front panel of the TV is detected.

The following software sequence should be used when utilizing this mode for Power-down or Idle:

1. Disable INT1 using the IE SFR.
2. Set INT1 to level sensitive using the TCON SFR.
3. Set the DAC digital input level to the desired threshold level using SAD/SADB SFRs and select the required input pin (P3.0/ADC0, P3.1/ADC1, P3.2/ADC2 or P3.3/ADC3) using CH<1:0> in the SAD SFR.
4. Enter DC Compare mode by setting the DC_COMP enable bit in the SADB SFR.
5. Enable INT1 using the IE SFR.
6. Enter Power-down or Idle mode. Upon wake-up the SAD should be restored to its conventional operating mode by disabling the DC_COMP control bit.

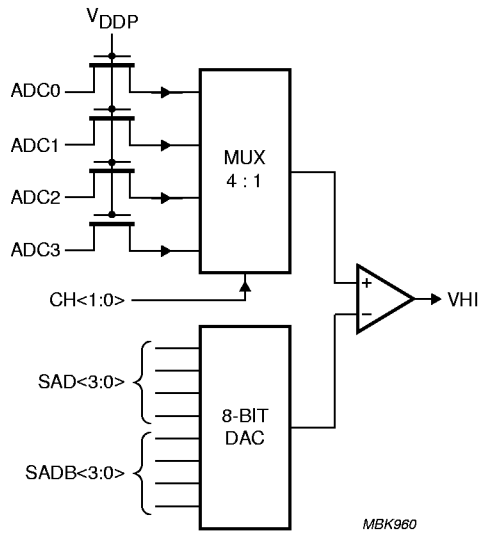


Fig.12 SAD block diagram.

16 I²C-BUS SERIAL I/O

The I²C-bus consists of a serial data (SDA) line and a serial clock (SCL) line. The definition of the I²C-bus protocol can be found in the document *"The I²C-bus and how to use it (including specification)"*. This document may be ordered using the code 9398 393 40011.

The device operates in four modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

The microcontroller peripheral is controlled by the Serial Control SFR (S1CON) and its status is indicated by the Status SFR (S1STA). Information is transmitted/received to/from the I²C-bus using the Data SFR (S1DAT) and the Slave Address SFR (S1ADR) is used to configure the slave address of the peripheral.

The byte level I²C-bus serial port is identical to the I²C-bus serial port on the P8xCE558, except for the clock rate selection bits CR<2:0> in S1CON. The operation of the subsystem is described in detail in the *"P8xCE558 data sheet"*.

16.1 I²C-bus port selection

Two I²C-bus ports are available SCL0/SDA0 and SCL1/SDA1. The selection of the port is done using TXT21.I²C PORT 0 and TXT21.I²C PORT 1. When the port is enabled, any information transmitted from the device goes onto the enabled port. Any information transmitted to the device can only be acted on if the port is enabled.

If both ports are enabled then data transmitted from the device is seen on both ports, however data transmitted to the device on one port can not be seen on the other port.

17 MEMORY INTERFACE

The memory interface controls access to the embedded Dynamic Random Access Memory (DRAM), refreshing of the DRAM and page clearing. The DRAM is shared between Data Capture, display and microcontroller sections. The Data Capture section uses the DRAM to store acquired information that has been requested. The display reads from the DRAM information and converts it into RGB values. The microcontroller uses the DRAM as embedded auxiliary RAM.

17.1 Memory structure

The memory is partitioned into two distinct areas, the dedicated Auxiliary RAM area, and the Display RAM area. The Display RAM area when not being used for Data Capture or display, can be used as an extension to the auxiliary RAM area.

17.1.1 AUXILIARY RAM

The Auxiliary RAM is not initialised at power-up. The contents of the Auxiliary RAM are maintained during Idle mode, but are lost if Power-down mode is entered.

17.1.2 DISPLAY RAM

The Display RAM is initialised on power-up to a value of 20H throughout. The contents of the Display RAM are maintained when entering Idle mode. If Idle mode is exited using an interrupt then the contents are unchanged, if Idle mode is exited using a reset then the contents are initialised to 20H.

17.2 Memory mapping

The dedicated Auxiliary RAM area occupies a maximum of 8 kbytes, with an address range from 0000H to 1FFFH. The Display RAM occupies a maximum of 10 kbytes with an address range from 2000H to 47FFH for TXT mode (see Fig.13).

17.3 Addressing memory

The memory can be addressed by the microcontroller in two ways, either directly using a MOVX command, or via Special Function Registers depending on what address is required.

The Display memory in the range 2000H to 47FFH can either be directly accessed using the MOVX, or via the Special Function Registers.

17.3.1 TXT DISPLAY MEMORY SFR ACCESS

The Display memory when in TXT mode (see Fig.14) is configured as 40 columns wide by 25 rows and occupies 1K × 8 bits of memory. There can be a maximum of 10 display pages. Using TXT15.BLOCK<3:0>, the required display page can be selected to be written to. The row and column within that block is selected using TXT9.R<4:0> and TXT10.C<5:0>. The data at the selected position can be read or written using TXT11.D<7:0>.

Whenever a read or write is performed on TXT11, the row values stored in TXT9 and column value stored in TXT10 are automatically incremented. For rows 0 to 24 the column value is incremented up to a maximum of 39, at which point it resets to '0' and increments the row counter value. When row 25 column 23 is reached the values of the row and column are both reset to zero.

Writing values outside of the valid range for TXT9 or TXT10 will cause undetermined operation of the auto-incrementing function for accesses to TXT11.

17.3.2 TXT Display memory MOVX access

It is important for the generation of OSD displays, that use this mode of access, to understand the mapping of the MOVX address onto the display row and column value. This mapping of row and column onto address is shown in Table 10. The values shown are added onto a base address for the required memory block (see Fig.13) to give a 16-bit address.

17.4 Page clearing

Page clearing is performed on request from either the Data Capture block, or the microcontroller under the control of the embedded software.

At power-on and reset the whole of the page memory is cleared. The TXT13.PAGE CLEARING bit will be set while this takes place.

17.4.1 Data Capture page clear

When a page header is acquired for the first time after a new page request or a page header is acquired with the erase (C4) bit set the page memory is 'cleared' to spaces before the rest of the page arrives.

When this occurs, the space code (20H) is written into every location of rows 1 to 23 of the basic page memory, the appropriate packet 27 row of the extension packet memory and the row where teletext packet 24 is written. This last row is either row 24 of the basic page memory, if the TXT0.X24 POSN bit is set, or row 0 of the extension packet memory, if the bit is not set. Page clearing takes place before the end of the TV line in which the header arrived which initiated the page clear.

This means that the 1 field gap between the page header and the rest of the page which is necessary for many teletext decoders is not required.

17.4.2 Software page clear

The software can also initiate a page clear, by setting the TXT9.CLEAR MEMORY bit. When it does so, every location in the memory block pointed to by TXT15.BLOCK<3:0> is cleared to a space code (20H). The CLEAR MEMORY bit is not latched so the software does not have to reset it after it has been set.

Only one page can be cleared in a TV line so if the software requests a page clear it will be carried out on the next TV line on which the Data Capture hardware does not force the page to be cleared. A flag, TXT13.PAGE CLEARING, is provided to indicate that a software requested page clear is being carried out. The flag is set when a logic 1 is written into the TXT9.CLEAR MEMORY bit and is reset when the page clear has been completed.

If TXT0.INV ON bit = 1 and a page clear is initiated on Block 8 all locations are cleared to 00H.

Table 10 Column and row to MOVX address (lower 10 bits of address)

ROW	COL. 0	.....	COL. 23	.....	COL. 31	COL. 32	.....	COL. 39
Row 0	000H	.....	017H	.....	01FH	3F8H	.....	3FFH
Row 1	020H	.....	037H	.....	03FH	3F0H	.....	3F7H
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
Row 23	2E0H	.....	3F7H	.....	2FFH	340H	.....	347H
Row 24	300H	.....	317H	.....	31FH	338H	.....	33FH
Row 25	320H	.....	337H	.....	.....	.....	.....	:

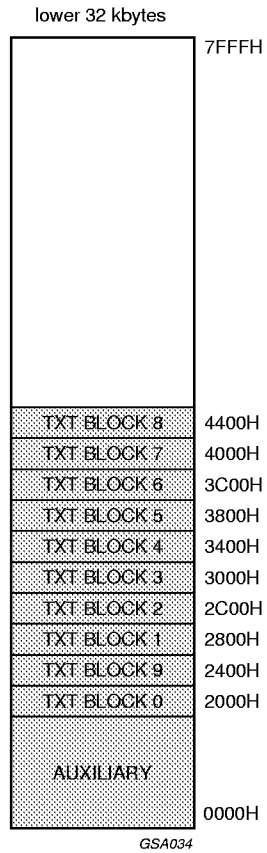


Fig.13 DRAM memory mapping.

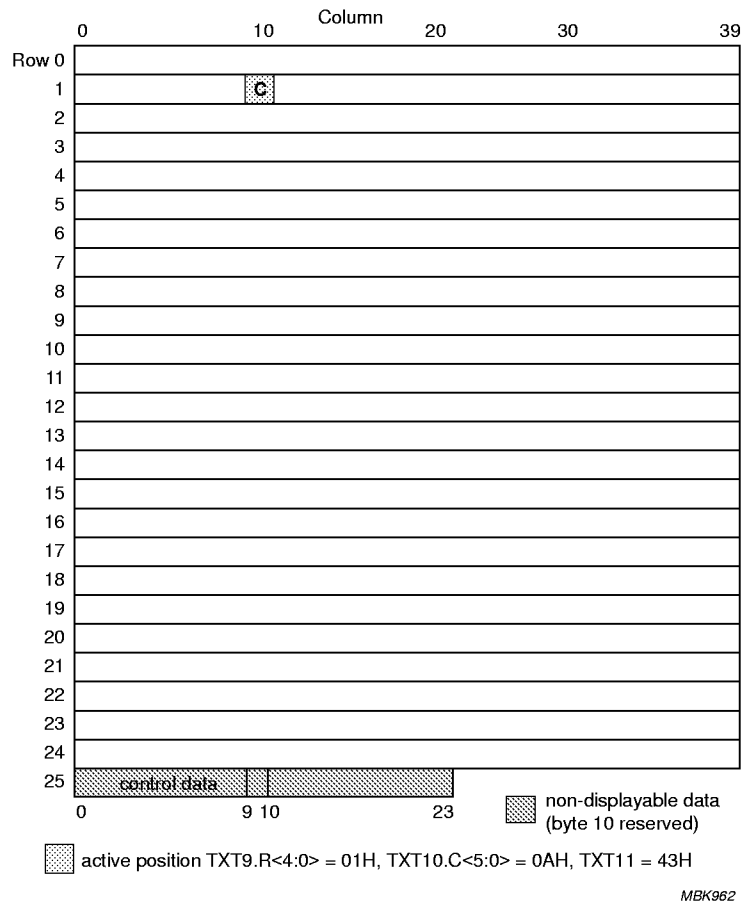


Fig.14 TXT memory map.

18 DATA CAPTURE

The Data Capture section takes in the analog Composite Video and Blanking Signal (CVBS), and from this extracts the required data, which is then decoded and stored in memory.

The extraction of the data is performed in the digital domain. The first stage is to convert the analog CVBS signal into a digital form. This is done using an ADC sampling at 12 MHz. The data and clock recovery is then performed by a Multi-Rate Video Input Processor (MulVIP). From the recovered data and clock the following data types are extracted: WST Teletext (625/525), VPS and WSS. The extracted data is stored in either memory (DRAM) via the Memory interface or in SFR locations.

18.1 Data Capture features

- Two CVBS inputs
- Video Signal Quality detector
- Data Capture for 625-line WST
- Data Capture for 525-line WST
- Data Capture for VPS data (Programme Delivery Control (PDC) system A)
- Data Capture for Wide Screen Signalling (WSS) bit decoding
- Automatic selection between 525 WST/625 WST
- Automatic selection between 625 WST/VPS on line 16 of Vertical Blanking Interval (VBI)
- Real-time capture and decoding for WST Teletext in hardware, to enable optimized microprocessor throughput
- Up to 10 pages stored on-chip
- Inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT)
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine in hardware for processing accented, G2 and G3 characters
- Signal quality detector for WST/VPS data types
- Comprehensive Teletext language coverage
- Full Field and Vertical Blanking Interval (VBI) data capture of WST data.

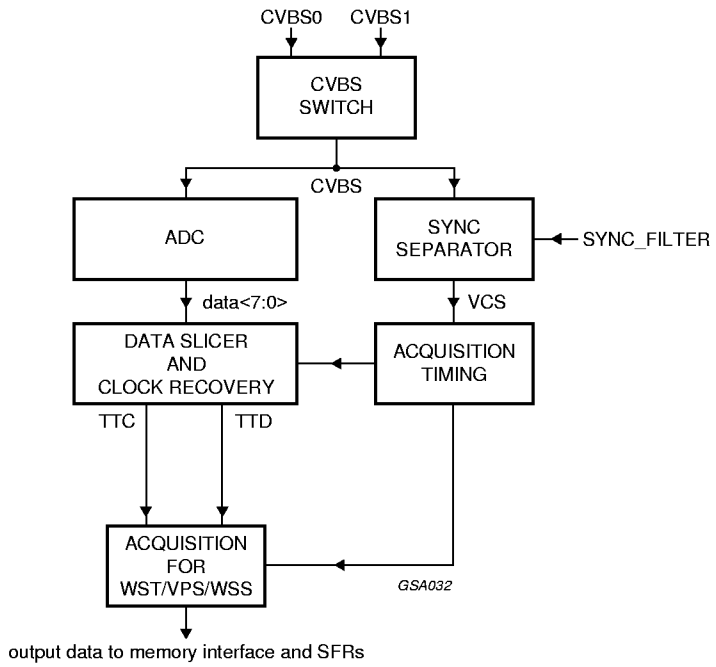


Fig.15 Data capture block diagram.

18.1.1 CVBS SWITCH

The CVBS switch is used to select the required analog input depending on the value of TXT8.CVBS1/$\overline{\text{CVBS0}}$.

18.1.2 ANALOG-TO-DIGITAL CONVERTER

The output of the CVBS switch is passed to a differential-to-single-ended converter, although in this device it is used in single-ended configuration with a reference. The analog output of the differential amplifier is converted into a digital representation by a full flash ADC with a sampling rate of 12 MHz.

18.1.3 MULTI-RATE VIDEO INPUT PROCESSOR

The multi-rate video input processor is a Digital Signal Processor designed to extract the data and recover the clock from a digitised CVBS signal.

18.1.4 DATA STANDARDS

The data and clock standards that can be recovered are shown in Table 11.

Table 11 Data slicing standards

DATA STANDARD	CLOCK RATE (MHz)
625 WST	6.9375
525 WST	5.7272
VPS	5.0
WSS	5.0

18.1.5 DATA CAPTURE TIMING

The Data Capture timing section uses the synchronisation information extracted from the CVBS signal to generate the required horizontal and vertical reference timings.

The timing section automatically recognises and selects the appropriate timings for either 625 (50 Hz) synchronisation or 525 (60 Hz) synchronisation. A flag TXT12.VIDEO SIGNAL QUALITY is set when the timing section is locked correctly to the incoming CVBS signal. When TXT12.VIDEO SIGNAL QUALITY is set another flag TXT12.525/$\overline{625}$ SYNC can be used to identify the standard.

18.1.6 ACQUISITION

The acquisition sections extracts the relevant information from the serial stream of data from the MulVIP and stores it in memory.

18.1.6.1 Making a page request

A page is requested by writing a series of bytes into the TXT3.PRD<4:0> SFR which corresponds to the number of the page required. The bytes written into TXT3 are stored in a RAM with an auto-incrementing address. The start address for the RAM is set using the TXT2.SC<2:0> to define which part of the page request is being written, and TXT2.REQ<3:0> is used to define which of the 10 page requests is being modified. If TXT2.REQ<3:0> is greater than 09H, then data being written to TXT3 is ignored. Table 12 shows the contents of the page request RAM.

Up to 10 pages of teletext can be acquired on the 10 page device, when TXT1.EXT PKT OFF is set to logic 1, and up to 9 pages can be acquired when this bit is set to logic 0. For a 20 page device the 10 page acquisition channels are banked, the bank being selected using TXT2.ACQ BANK.

If the 'DO CARE' bit for part of the page number is set to logic 0 then that part of the page number is ignored when the teletext decoder is deciding whether a page being received off air should be stored or not. For example, if the 'DO CARE' bits for the four subcode digits are all set to logic 0 then every subcode version of the page will be captured.

Table 12 The contents of the Page request RAM

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE Page Tens	PT3	PT2	PT1	PT0
2	DO CARE Page Units	PU3	PU2	PU1	PU0
3	DO CARE Hour Tens	X	X	HT1	HT0
4	DO CARE Hours Units	HU3	HU2	HU1	HU0
5	DO CARE Minutes Tens	X	MT2	MT1	MT0
6	DO CARE Minutes Units	MU3	MU2	MU1	MU0
7	X	X	X	E1	E0

When the HOLD bit is set to a logic 0 the teletext decoder will not recognise any page as having the correct page number and no pages will be captured. In addition to providing the user requested hold function this bit should be used to prevent the inadvertent capture of an unwanted page when a new page request is being made.
For example, if the previous page request was for page 100 and this was being changed to page 234, it would be possible to capture page 200 if this arrived after only the requested magazine number had been changed.

The E1 and E0 bits control the error checking which should be carried out on packets 1 to 23 when the page being requested is captured. This is described in more detail in Section 18.1.6.3.

For a multi-page device, each packet can only be written into one place in the teletext RAM so if a page matches more than one of the page requests the data is written into the area of memory corresponding to the lowest numbered matching page request.

At power-up each page request defaults to any page, hold on and error check Mode 0.

18.1.6.2 Rolling headers and time

When a new page has been requested it is conventional for the decoder to turn the header row of the display green and to display each page header as it arrives until the correct page has been found.

When a page request is changed (i.e. when the TXT3 SFR is written to) a flag (PBLF) is written into bit 5, column 9, row 25 of the corresponding block of the page memory. The state of the flag for each block is updated every TV line, if it is set for the current display block, the acquisition section writes all valid page headers which arrive into the display block and automatically writes an alphanumeric green character into column 7 of row 0 of the display block every TV line.

When a requested page header is acquired for the first time, rows 1 to 23 of the relevant memory block are cleared to space, i.e. have 20H written into every column, before the rest of the page arrives. Row 24 is also cleared if the TXT0.X24 POSN bit is set. If the TXT1.EXT PKT OFF bit is set the extension packets corresponding to the page are also cleared.

The last 8 characters of the page header are used to provide a time display and are always extracted from every valid page header as it arrives and written into the display block.

The TXT0.DISABLE HEADER ROLL bit prevents any data being written into row 0 of the page memory except when a page is acquired off air i.e. rolling headers and time are not written into the memory. The TXT1.ACQ OFF bit prevents any data being written into the memory by the teletext acquisition section.

When a parallel magazine mode transmission is being received only headers in the magazine of the page requested are considered valid for the purposes of rolling headers and time. Only one magazine is used even if don't care magazine is requested. When a serial magazine mode transmission is being received all page headers are considered to be valid.

18.1.6.3 Error checking

Before teletext packets are written into the page memory they are error checked. The error checking carried out depends on the packet number, the byte number, the error check mode bits in the page request data and the TXT1.8-BIT bit.

If an uncorrectable error occurs in one of the Hamming checked addressing and control bytes in the page header or in the Hamming checked bytes in packet 8/30, bit 4 of the byte written into the memory is set, to act as an error flag to the software. If uncorrectable errors are detected in any other Hamming checked data the byte is not written into the memory.

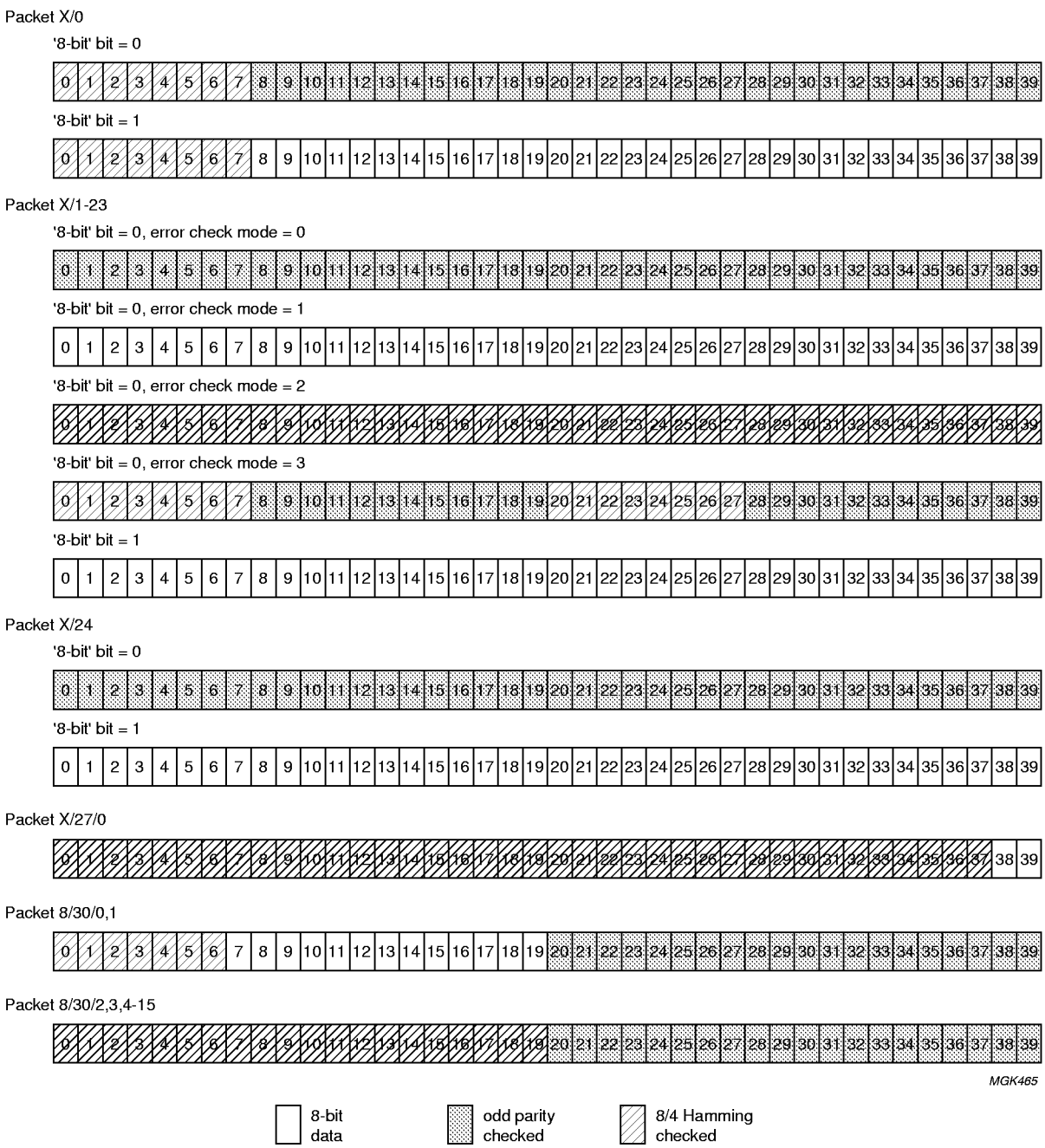
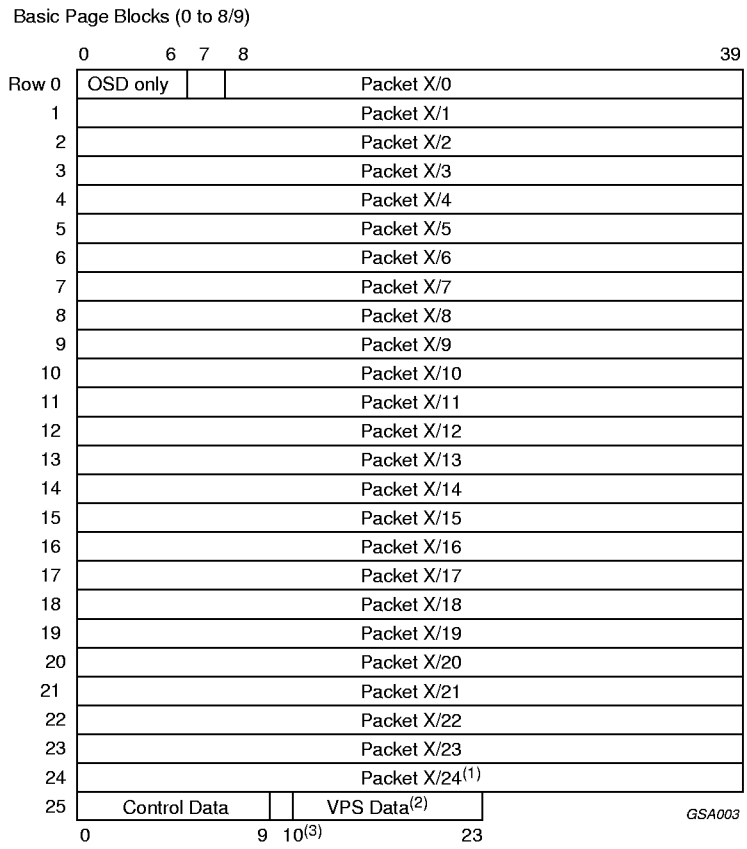


Fig.16 Error checking.



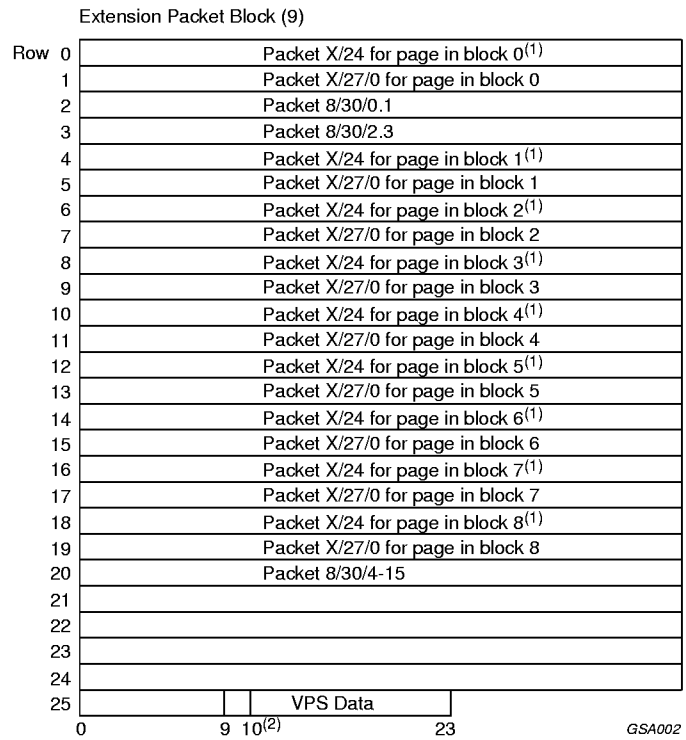
(1) If 'X24 POSN' bit = 1.
(2) VPS data block 9, unused in blocks 0 to 8.
(3) Byte 10 reserved.

Fig.17 Packet storage locations.

18.1.6.4 Teletext memory organisation

The teletext memory is divided into 2 banks of 10 blocks. Normally, when the TXT1.EXT PKT OFF bit is logic 0, each of blocks 0 to 8 contains a teletext page arranged in the same way as the basic page memory of the page device and block 9 contains extension packets. When the TXT1.EXT PKT OFF bit is logic 1, no extension packets are captured and block 9 of the memory is used to store another page. The number of the memory block into which a page is written corresponds to the page request number which resulted in the capture of the page.

Packet 0, the page header, is split into two parts when it is written into the text memory. The first 8 bytes of the header contain control and addressing information. They are Hamming decoded and written into columns 0 to 7 of row 25. Row 25 also contains the magazine number of the acquired page and the PLBF flag but the last 14 bytes are unused and may be used by the software, if necessary.



(1) If 'X24 POSN' bit = 0.
(2) Byte 10 reserved.

Fig.18 Extension packet storage locations.

18.1.6.5 Row 25 data contents

The Hamming error flags are set if the on-board 8/4 Hamming checker detects that there has been an uncorrectable (2-bit) error in the associated byte. It is possible for the page to still be acquired if some of the page address information contains uncorrectable errors if that part of the page request was a 'don't care'. There is no error flag for the magazine number as an uncorrectable error in this information prevents the page being acquired.

The interrupt sequence (C9) bit is automatically dealt with by the acquisition section so that rolling headers do not contain a discontinuity in the page number sequence.

The magazine serial (C11) bit indicates whether the transmission is a serial or a parallel magazine transmission. This affects the way the acquisition section operates and is dealt with automatically.

The newsflash (C5), subtitle (C6), suppress header (C7), inhibit display (C10) and language control (C12 to 14) bits are dealt with automatically by the display section.

The update (C8) bit has no effect on the hardware.
The remaining 32 bytes of the page header are parity checked and written into columns 8 to 39 of row 0. Bytes which pass the parity check have the MSB set to a logic 0 and are written into page memory. Bytes with parity errors are not written into the memory.

Table 13 The data in row 25 of the basic page memory

COL	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	Hamming error	PU3	PU2	PU1	PU0
1	0	0	0	Hamming error	PT3	PT2	PT1	PT0
2	0	0	0	Hamming error	MU3	MU2	MU1	MU0
3	0	0	0	Hamming error	C4	MT2	MT1	MT0
4	0	0	0	Hamming error	HU3	HU2	HU1	HU0
5	0	0	0	Hamming error	C6	C5	HT1	HT0
6	0	0	0	Hamming error	C10	C9	C8	C7
7	0	0	0	Hamming error	C14	C13	C12	C11
8	0	0	0	$\overline{\text{FOUND}}$	0	MAG2	MAG1	MAG0
9	0	0	PBLF	0	0	0	0	0
10 to 23	–	–	–	unused	–	–	–	–

18.1.6.6 Inventory page

If the TXT0.INV ON bit is a logic 1, memory block 8 is used as an inventory page.The inventory page consists of two tables: the Transmitted Page Table (TPT) and the Subtitle Page Table (SPT).

In each table, every possible combination of the page tens and units digit, 00H to FFH, is represented by a byte.

Each bit of these bytes corresponds to a magazine number so each page number, from 100H to 8FFH, is represented by a bit in the table.

The bit for a particular page in the TPT is set when a page header is received for that page. The bit in the SPT is set when a page header for the page is received which has the 'subtitle' page header control bit (C6) set. The bit for a particular page in the TPT is set when a page header is received for that page. The bit in the SPT is set when a page header for the page is received which has the 'subtitle' page header control bit (C6) set.

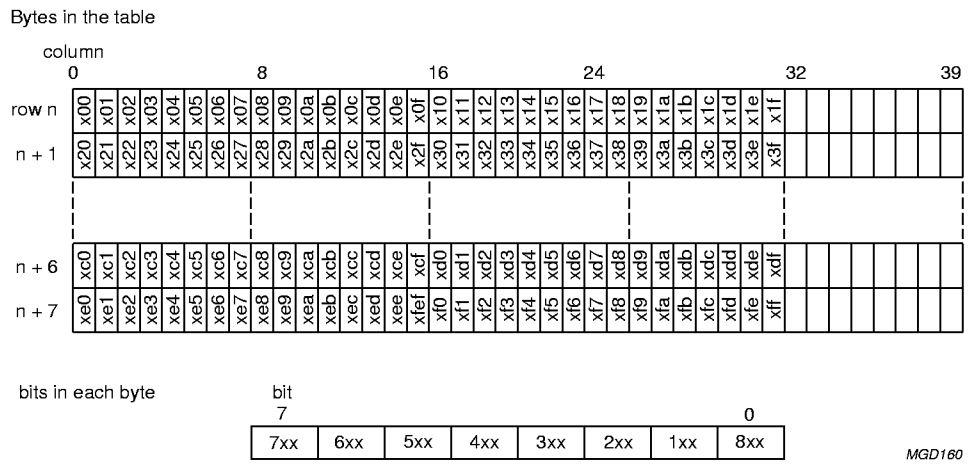


Fig.19 Transmitted/subtitle page organisation.

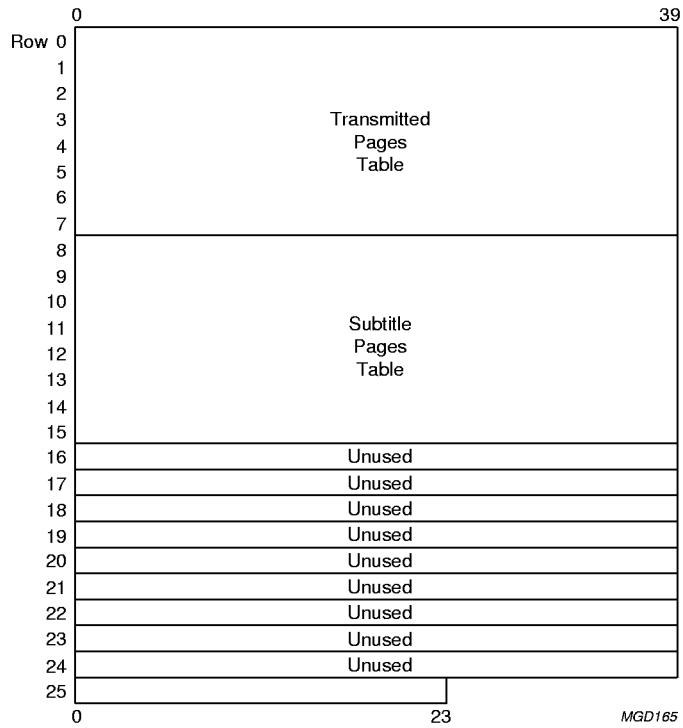


Fig.20 Inventory page organisation.

18.1.6.7 Packet 26 processing

One of the uses of packet 26 is to transmit characters which are not in the basic teletext character set. The family automatically decodes packet 26 data and, if a character corresponding to that being transmitted is available in the character set, automatically writes the appropriate character code into the correct location in the teletext memory. This is not a full implementation of the packet 26 specification allowed for in level 2 teletext, and so is often referred to as level 1.5.

By convention, the packets 26 for a page are transmitted before the normal packets. To prevent the default character data overwriting the packet 26 data the device incorporates a mechanism which prevents packet 26 data from being overwritten. The mechanism is disabled when the Spanish national option is detected as the Spanish transmission system sends even parity (i.e. incorrect) characters in the basic page locations corresponding to the characters sent via packet 26 and these will not overwrite the packet 26 characters anyway. The special treatment of Spanish national option is prevented if TXT12.ROM VER3 is logic 0 or if the TXT8.DISABLE SPANISH is set.

Packet 26 data is processed regardless of the TXT1.EXT PKT OFF bit, but setting theTXT1.X26 OFF disables packet 26 processing.

The TXT8.PKT26 RECEIVED bit is set by the hardware whenever a character is written into the page memory by the packet 26 decoding hardware. The flag can be reset by writing a logic 0 into the SFR bit.

18.1.7 WST ACQUISITION

The family is capable of acquiring Level 1.5 625-line and 525-line World System Teletext.

18.2 Broadcast service data detection

When a packet 8/30 is detected, or a packet 4/30 when the device is receiving a 525 line transmission, the TXT13. PKT 8/30 flag is set. The flag can be reset by writing a 0 into the SFR bit.

18.3 VPS acquisition

When the TXT0.VPS ON bit is set, any VPS data present on line 16, field 0 of the CVBS signal at the input of the teletext decoder is error checked and stored in row 25, block 9 of the basic page memory. The device automatically detects whether teletext or VPS is being transmitted on this line and decodes the data appropriately.

Each VPS byte in the memory consists of 4 biphase decoded data bits (bits 0 to 3), a biphase error flag (bit 4) and three logic 0s (bits 5 to 7).

The TXT13.VPS RECEIVED bit is set by the hardware whenever VPS data is acquired.

Full details of the VPS system can be found in the *"Specification of the Domestic Video Programme Delivery Control System (PDC); EBU Tech. 3262-E"*.

18.4 WSS acquisition

The Wide Screen Signalling data transmitted on line 23 gives information on the aspect ratio and display position of the transmitted picture, the position of subtitles and on the camera/film mode. Some additional bits are reserved for future use. A total of 14 data bits are transmitted.

All of the available data bits transmitted by the Wide Screen Signalling signal are captured and stored in SFRs WSS1, WSS2 and WSS3. The bits are stored as groups of related bits, and an error flag is provided for each group to indicate when a transmission error has been detected in one or more of the bits in the group.

Wide screen signalling data is only acquired when the TXT8.WSS ON bit is set.

The TXT8.WSS RECEIVED bit is set by the hardware whenever wide screen signalling data is acquired. The flag can be reset by writing a logic 0 into the SFR bit.

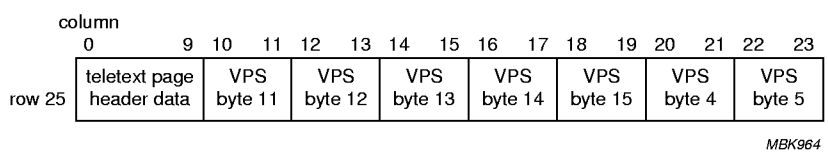


Fig.21 VPS data storage.

19 DISPLAY

The display section is based on the requirements for a Level 1.5 WST Teletext. There are some enhancements for use with locally generated OSDs.

The display section reads the contents of the Display memory and interprets the control/character codes. From this information and other global settings, the display produces the required RGB signals and Video/Data (Fast Blanking) signal for a TV signal processing device.

The display is synchronised to the TV signal processing device by way of horizontal and vertical sync signals provided by external circuits (Slave Sync mode). From these signals all display timings are derived.

19.1 Display features

- Teletext and Enhanced On-Screen Display (OSD) modes
- Level 1.5 WST features
- Single/Double/Quadruple Width and Height for characters
- Variable flash rate controlled by software
- Fixed character matrix (H × V) 12 × 10
- Soft colours using Colour Look Up Table (CLUT) with 4096 colour palette
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- 1 WST Character set (G0/G2) in single device (e.g. Latin or Cyrillic or Greek or Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters.

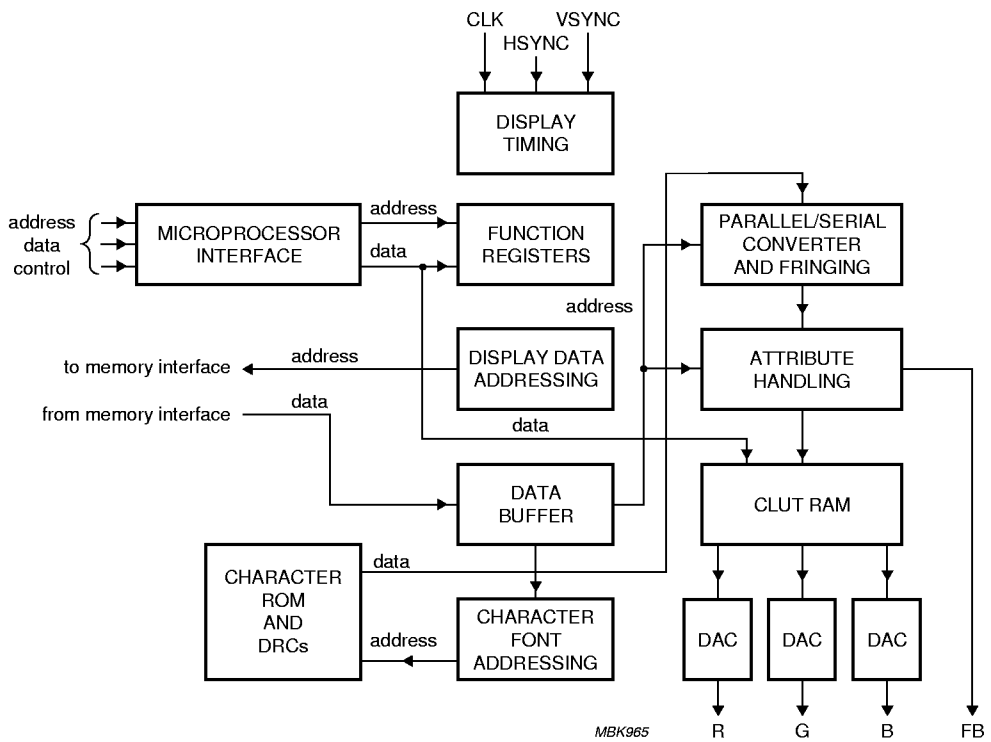


Fig.22 Display block diagram.

19.2 Display mode

The display is configured as WST with additional serial and global attributes. The display is configured as a fixed 25 rows with 40 characters per row.

19.3 Display feature descriptions

19.3.1 FLASH

Flashing causes the foreground colour pixel to be displayed as the background pixels.The flash frequency is controlled by software setting and resetting the MMR Status (see Table 24) at the appropriate interval.

This attribute is set by the control character 'flash' (08H) (see Fig.26) and remains valid until the end of the row or until reset by the control character 'steady' (09H).

19.3.2 BOXES

Two types of boxes exist, the Teletext box and the OSD box. The Teletext box is activated by the 'start box' control character (0BH), two start box characters are required to begin a Teletext box, with the box starting between the two characters. The box ends at the end of the line or after a 'end box' control character.

OSD boxes are started using size implying OSD control characters (BCH, BDH, BEH and BFH). The box starts after the control character ('set after') and ends either at the end of the row or at the next size implying OSD character ('set at'). The attributes flash, Teletext box, conceal, separate graphics, twist and hold graphics are all reset at the start of an OSD box, as they are at the start of the row. OSD boxes are only valid in TV mode which is defined by TXT5 = 03H and TXT6 = 03H.

19.3.3 SIZE

The size of the characters can be modified in both the horizontal and vertical directions.

Three horizontal sizes are available normal (×1), double (×2), quadruple (×4). The control characters 'normal size' (0CH/BCH) enables normal size, the 'double width' or 'double size' (0EH/BEH/0FH/BFH) enables double width characters.

Any two consecutive combination of 'double width' or 'double size' (0EH/BEH/0FH/BFH) activates quadruple width characters, provided quadruple width characters are enabled by TXT4.QUAD WIDTH ENABLE.

Three vertical sizes are available normal (×1), double (×2), quadruple (×4). The control characters 'normal size' (0CH/BCH) enable normal size, the 'double height' or 'double size' (0DH/BDH/0FH/BFH) enable double height characters. Quadruple height characters are achieved by using double height characters and setting the global attributes TXT7.DOUBLE HEIGHT (expand) and TXT7.BOTTOM/$\overline{\text{TOP}}$.

If double height characters are used in Teletext mode, single height characters in the lower row of the double height character are automatically disabled.

19.3.4 COLOURS

19.3.4.1 Colour Look Up Table (CLUT)

A CLUT with 16 colour entries is provided. The colours are programmable out of a palette of 4096 (4 bits per R, G and B). The CLUT is defined by writing data to a RAM that resides in the MOVX address space of the 80C51.

Table 14 CLUT colour values

RED<3:0> (B11 TO B8)	GRN<3:0> (B7 TO B4)	BLUE<3:0> (B3 TO B0)	COLOUR ENTRY
0000	0000	0000	0
0000	0000	1111	1
...	...	...	...
1111	1111	0000	14
1111	1111	1111	15

19.3.5 FOREGROUND COLOUR

The foreground colour is selected via a control character (see Fig.26). The colour control characters take effect at the start of the next character (set-after) and remain valid until the end of the row, or until modified by a control character. Only 8 foreground colours are available.

The TEXT foreground control characters map to the CLUT entries as shown in Table 15.

Table 15 Foreground CLUT mapping

CONTROL CODE	DEFINED COLOUR	CLUT ENTRY
00H	black	0
01H	red	1
02H	green	2
03H	yellow	3
04H	blue	4
05H	magenta	5
06H	cyan	6
07H	white	7

19.3.6 Background colour

The control character new background (1DH) is used to change the background colour to the current foreground colour. The selection is immediate (set at) and remains valid until the end of the row or until otherwise modified.

The TEXT background control characters map to the CLUT entries as shown in Table 16.

Table 16 Background CLUT mapping

CONTROL CODE	DEFINED COLOUR	CLUT ENTRY
00H + 1DH	black	8
01H + 1DH	red	9
02H + 1DH	green	10
03H + 1DH	yellow	11
04H + 1DH	blue	12
05H + 1DH	magenta	13
06H + 1DH	cyan	14
07H + 1DH	white	15

19.3.7 Fringing

The display of fringing is controlled by the TXT4.SHADOW bit.

When set all the alphanumeric characters being displayed are shadowed, graphics characters are not shadowed.

19.3.8 Meshing

The attribute effects the background colour being displayed. Alternate pixels are displayed as the background colour or video. The structure is offset by 1 pixel from scan line to scan line, thus achieving a checker board display of the background colour and video.

TXT: There are two meshing attributes one that only affects black background colours TXT4.B MESH ENABLE and a second that only affects backgrounds other than black TXT4.C MESH ENABLE. A black background is defined as CLUT entry 8, a non-black background is defined as CLUT entry 9 to 15.

19.3.9 Cursor

The cursor operates by reversing the background and foreground colours in the character position pointed to by the active cursor position. The cursor is enabled using TXT7.CURSOR ON. When active, the row the cursor appears on is defined by TXT9.R<4:0> and the column is defined by TXT10.C<5:0>. The position of the cursor can be fixed using TXT9.CURSOR FREEZE.

The valid range for row positioning is 0 to 24. The valid range for column is 0 to 39.

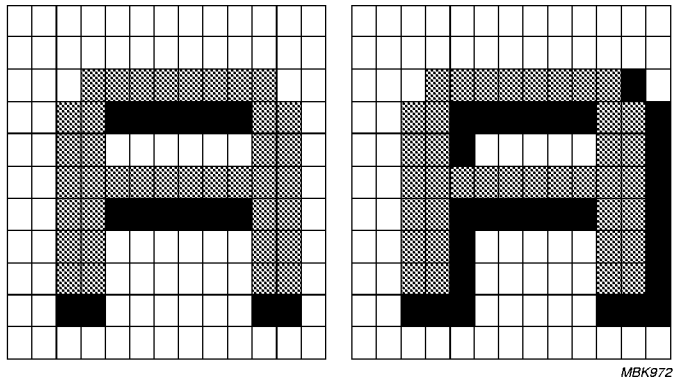


Fig.23 South and south-west fringing.

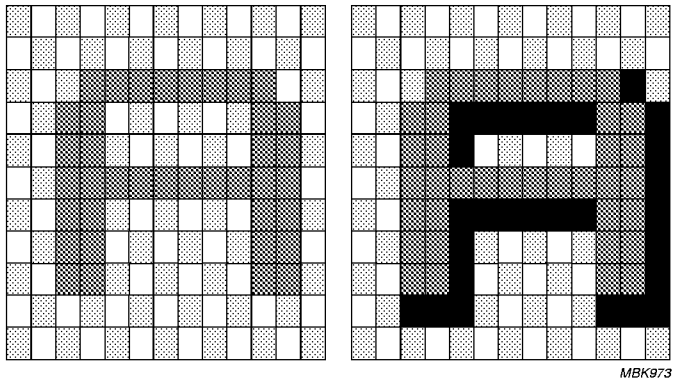


Fig.24 Meshing and meshing/fringing (south + west).

Fig.25 Cursor display.

19.4 Character and attribute coding

The character coding is in a serial format, with only one attribute being changed at any single location. The serial attributes take effect either at the position of the attribute (set at), or at the following location (set after). The attribute remains effective until either modified by new serial attributes or until the end of the row.

The default settings at the start of a row is:

- Foreground colour white (CLUT address 7)
- Background colour black (CLUT address 8)
- Horizontal size ×1, vertical size ×1 (normal size)
- Alphanumeric on
- Contiguous Mosaic Graphics
- Release Mosaics
- Flash off
- Box off
- Conceal off
- Twist off.

The attributes have individual codes which are defined in the basic character table (see Fig.26).

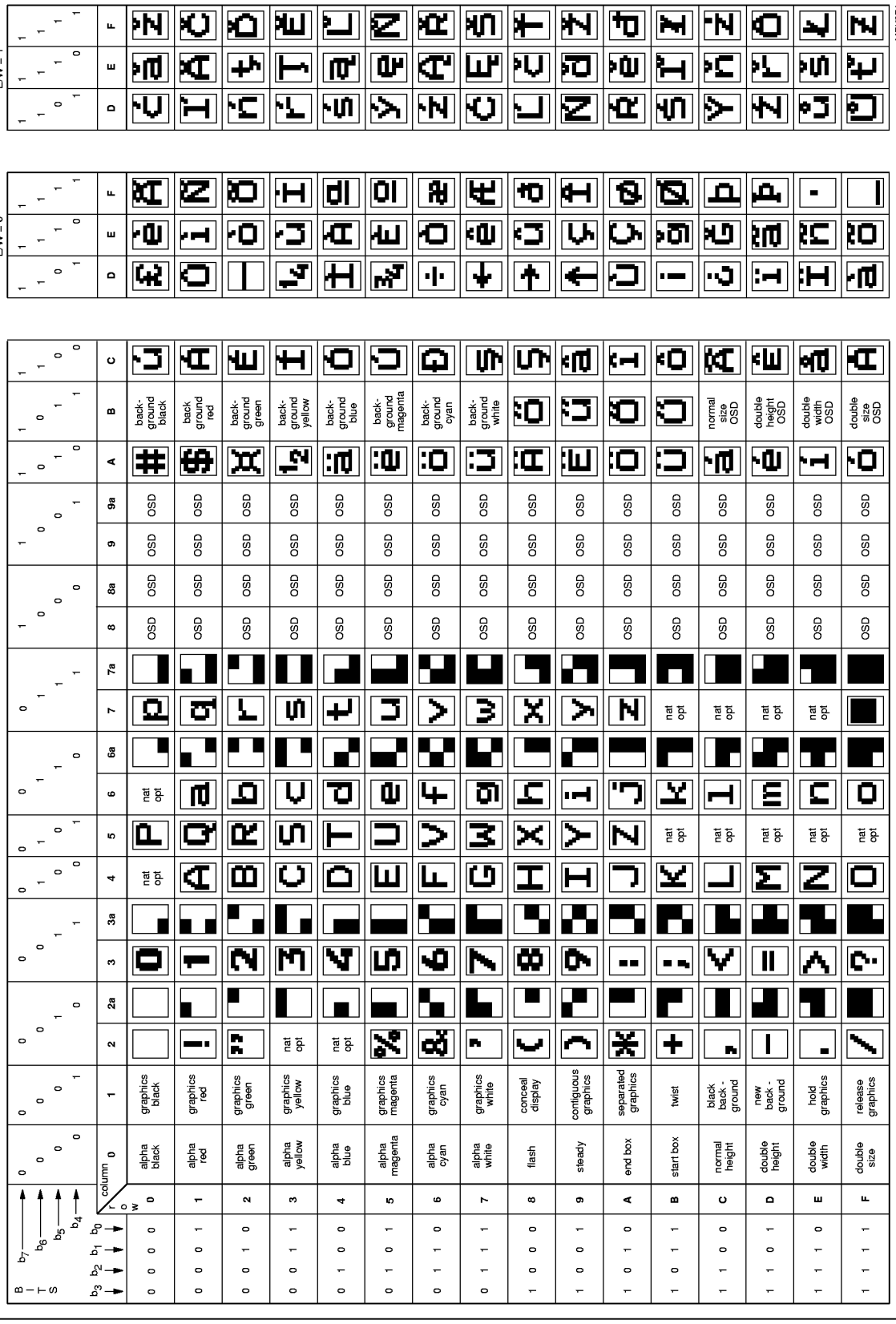


Fig.26 TXT basic character set (Pan-European).

19.5 Screen and global controls

A number of attributes are available that affect the whole display region, and cannot be applied selectively to regions of the display.

19.5.1 Display Modes

The display mode is controlled by the bits in the TXT5 and TXT6. There are three control functions: Text on, Background on and Picture on. Separate sets of bits are used inside and outside teletext boxes so that different display modes can be invoked. TXT6 is used if the newsflash (C5) or subtitle (C6) bits in row 25 of the basic page memory are set, otherwise TXT5 is used. This allows the software to set up the type of display required on newsflash and subtitle pages (e.g. text inside boxes, TV picture outside) this will be invoked without any further software intervention when such a page is acquired.

When teletext box control characters are present in the display page memory, the appropriate box control bit must be set, TXT7.BOX ON 0, TXT7.BOX ON 1 – 23 or TXT7.BOX ON 24. This allows the display mode to be different inside the Teletext box compared to outside. These bits are present to allow boxes in certain areas of the screen to be disabled.

The use of teletext boxes for OSD messages has been superseded in this device by the OSD box concept, but these bits remain to allow teletext boxes to be used, if required.

19.6 Screen colour

Screen colour is displayed from 10.5 to 62.5 ms after the active edge of the HSYNC input and on TV lines 23 to 310 inclusive, for a 625-line display, and lines 17 to 260 inclusive for a 525-line display.

The register bits TXT17.SCREEN COL<2:0> can be used to define a colour to be displayed in place of TV picture and the black background colour. If the bits are all set to zero, the screen colour is defined as ‘transparent’ and TV picture and background colour are displayed as normal. Otherwise the bits define CLUT entries 9 to 15.

19.7 Text display control

The display is organised as a fixed size of 25 rows (0 to 24) of 40 columns (0 to 39), This is the standard size for teletext transmissions. The control data in row 25 is not displayed but is used to configure the display page correctly.

Table 17 TXT display control bits

PICTURE ON	TEXT ON	BACKGROUND ON	EFFECT
0	0	X	Text mode, black screen
0	1	0	Text mode, background always black
0	1	1	Text mode
1	0	X	Video mode
1	1	0	Mixed text and TV mode
1	1	1	Text mode, TV picture outside text area

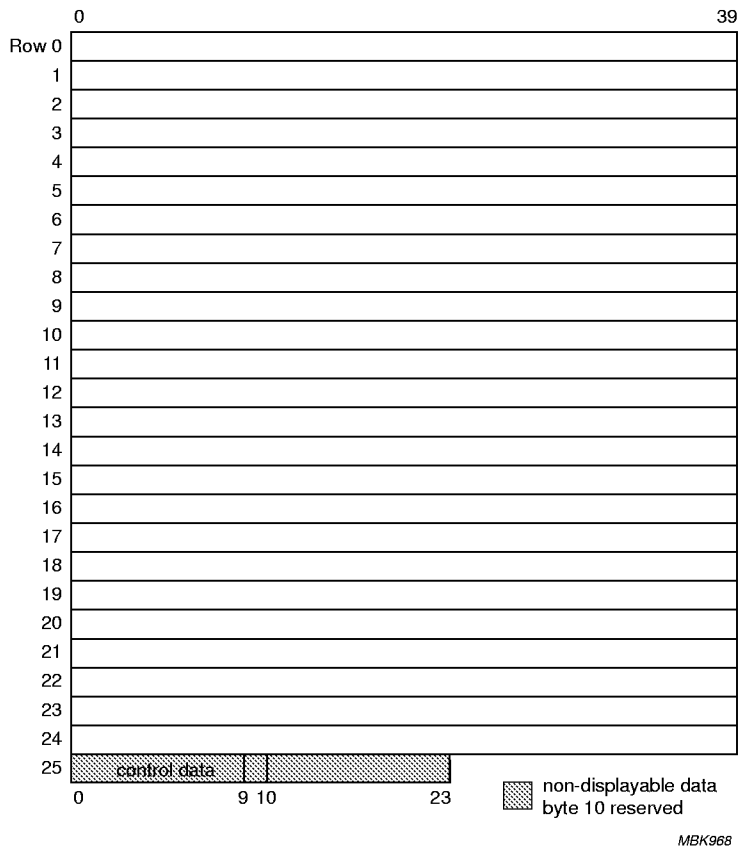


Fig.27 TXT text area.

19.8 Display positioning

The display consists of the screen colour covering the whole screen and the text area that is placed within the visible screen area.

The screen colour extends over a large vertical and horizontal range so that no offset is needed. The text area is offset in both directions relative to the vertical and horizontal sync pulses.

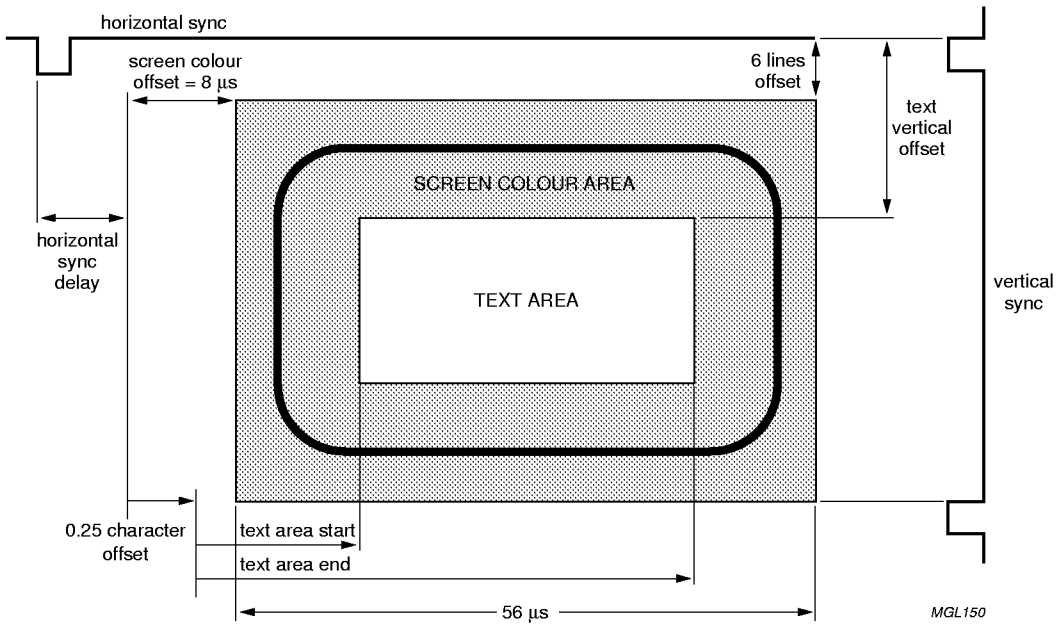


Fig.28 Display area positioning.

19.8.1 SCREEN COLOUR DISPLAY AREA

This area is covered by the screen colour. The screen colour display area starts with a fixed offset of 8 µs from the leading edge of the horizontal sync pulse in the horizontal direction. A vertical offset is not necessary.

Table 18 Screen colour display area

VECTOR	DESCRIPTION
Horizontal	Start at 8 µs after leading edge of horizontal sync for 56 µs.
Vertical	Line 9, field 1 (321, field 2) to leading edge of vertical sync (line numbering using 625 standard).

19.8.2 TEXT DISPLAY AREA

The text area can be defined to start with an offset in both the horizontal and vertical direction.

Table 19 Text display area

VECTOR	DESCRIPTION
Horizontal	Up to 40 full sized characters per row. Start position setting from 8 to 64 characters from the leading edge of horizontal sync. Fine adjustment in quarter characters.
Vertical	256 lines (nominal 41 to 297). Start position setting from leading edge of vertical sync, legal values are 4 to 64 lines. (line numbering using 625 standard).

The horizontal offset is set in the MMR Text Area Start. The offset is done in full width characters using TAS<5:0> and quarter characters using HOP<1:0> for fine setting. The values 00H to 08H for TAS<5:0> will result in a corrupted display.

The width of the text area is defined in the MMR Text Area End by setting the end character value TAE<5:0>. This number determines where the background colour of the text area will end if set to extend to the end of the row. It will also terminate the character fetch process thus eliminating the necessity of a row end attribute. This entails however writing to all positions.

The vertical offset is set in the MMR Text Position Vertical Register. The offset value VOL<5:0> is done in number of TV scan lines.

Note that the Text Position Vertical Register should not be set to 00H as the Display Busy interrupt is not generated in these circumstances.

19.9 Character set

A set can consist of alphanumeric characters as required by WST Teletext or customer definable OSD characters.

Two character sets can be displayed at once. These are the basic G0 set or the alternate G2 set (Twist Set). The basic set is selected using TXT18.BS<1:0>. The alternate/twist character set is defined by TXT19.TS<1:0>. Since the alternate character set is an option it can be enabled or disabled using TXT19.TEN, and the language code that is defined for the alternate set is defined by TXT19.TC<2:0>.

19.10 Display synchronization

The horizontal and vertical synchronizing signals from the TV deflection are used as inputs. Both signals can be inverted before being delivered to the Phase Selector section.

SFRs bits TXT1.HPOLARITY and TXT1.VPOLARITY control the polarity.

A line locked 12 MHz clock is derived from the 12 MHz free running oscillator by the Phase Selector. This line locked clock is used to clock the whole of the Display block.

The horizontal and vertical sync signals are synchronized with the 12 MHz clock before being used in the Display section.

19.11 Video/data switch (fast blanking) polarity

The polarity of the Video/data (fast blanking) signal can be inverted. The polarity is set with the VDSPOL bit in the MMR RGB Brightness.

Table 20 Fast blanking signal polarity

VDSPOL	VDS	CONDITION
0	1	RGB display
0	0	Video display
1	0	RGB display
1	1	Video display

19.12 Video/data switch adjustment

To take into account the delay between the RGB values and the VDS signal due to external buffering, the VDS signal can be moved in relation to the RGB signals. The VDS signal can be set to be either a clock cycle before or after the RGB signal, or coincident with the RGB signal. This is done using VDEL<2:0> in the MMR Configuration.

19.13 RGB brightness control

A brightness control is provided to allow the RGB upper output voltage level to be modified. The nominal value is 1 V into a 15 Ω resistor, but can be varied between 0.7 and 1.2 V.

The brightness is set in the RGB Brightness Register.

Table 21 RGB brightness

BRI3 TO BRI0	RGB BRIGHTNESS
0000	lowest value
...	...
1111	highest value

19.14 Contrast reduction

The $\overline{COR}$ bits in SFRs TXT5 and TXT6 control when the $\overline{COR}$ output of the device is activated (i.e. pulled LOW). This output is intended to act on the TVs display circuits to reduce contrast of the video when it is active. The result of contrast reduction is to improve the readability of the text in a mixed teletext and video display.

The bits in the TXT5 and TXT6 SFRs allow the display to be set up so that, for example, the areas inside teletext boxes will be contrast reduced when a subtitle is being displayed but that the rest of the screen will be displayed as normal video.

20 MEMORY MAPPED REGISTERS (MMR)

The memory mapped registers are used to control the display. The registers are mapped into the microcontroller MOVX address space, starting at address 87F0H and extending to 87FFH.

Table 22 MMR address summary

REGISTER NO.	MEMORY ADDRESS	FUNCTION
1	87F1H	Text Position Vertical
2	87F2H	Text Area Start
3	87F3H	Fringing Control
4	87F4H	Text Area End
7	87F7H	RGB Brightness
8	87F8H	Status
12	87FCH	HSYNC Delay
13	87FDH	VSYNC Delay
15	87FFH	Configuration

Table 23 MMR map

ADD	R/W	NAME	7	6	5	4	3	2	1	0	RESET
87F1	R/W	Text Position Vertical	–	–	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	00H
87F2	R/W	Text Area Start	HOP1	HOP0	TAS5	TAS4	TAS3	TAS2	TAS1	TAS0	00H
87F3	R/W	Fringing Control	FRC3	FRC2	FRC1	FRC0	FRDN	FRDE	FRDS	FRDW	00H
87F4	R/W	Text Area End	–	–	TAE5	TAE4	TAE3	TAE2	TAE1	TAE0	00H
87F7	R/W	RGB Brightness	VDSPOL	–	–	–	BRI3	BRI2	BRI1	BRI0	00H
87F8	R	Status	BUSY	FIELD	–	FLR	–	–	–	–	00H
	W		–	–	–	FLR	–	–	–	–	00H
87FC	R/W	HSYNC Delay	–	HSD6	HSD5	HSD4	HSD3	HSD3	HSD1	HSD0	00H
87FD	R/W	VSYNC Delay	–	VSD6	VSD5	VSD4	VSD3	VSD2	VSD1	VSD0	00H
87FF	R/W	Configuration	–	VDEL2	VDEL1	VDEL0	TXT/V	–	–	–	00H

Table 24 MMR bit definition

REGISTER	FUNCTION
Text Position Vertical	
VOL5 to VOL0	display start vertical offset from VSYNC (lines)
Text Area Start	
HOP1 to HOP0	fine horizontal offset in quarter of characters
TAS5 to TAS0	text area start
Fringing Control	
FRC3 to FRC0	fringing colour, value address of CLUT
FRDN	fringe in north direction (logic 1)
FRDE	fringe in east direction (logic 1)
FRDS	fringe in south direction (logic 1)
FRDW	fringe in west direction (logic 1)
Text Area End	
TAE5 to TAE0	text area end, in full characters
RGB Brightness	
VDSPOL	VDS polarity 0 = RGB (1), Video (0) 1 = RGB (0), Video (1)
BRI3 to BRI0	RGB brightness control

REGISTER	FUNCTION
Status read	
BUSY	access to display memory could cause display problems (logic 1)
FIELD	even field (logic 1)
FLR	active flash region background only displayed (logic 1)
Status write	
FLR	active flash region background colour only displayed (logic 1)
HSYNC Delay	
HSD6 to HSD0	HSYNC delay, in full size characters
VSYNC Delay	
VSD6 to VSD0	VSYNC delay in number of 8-bit 12 MHz clock cycles
Configuration	
VDEL2 to VDEL0	pixel delay between VDS and RGB output 000 = VDS switched to video, not active 001 = VDS active one pixel earlier then RGB 010 = VDS synchronous to RGB 100 = VDS active one pixel after RGB
TXT/V	BUSY signal switch; horizontal (logic 1)

21 LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDX}	supply voltage (all supplies)		−0.5	+4.0	V
V_I	input voltage (any input)	note 1	−0.5	V_{DD} + 0.5 or 4.1	V
V_O	output voltage (any output)	note 1	−0.5	V_{DD} + 0.5	V
I_O	output current (each output)		–	±10	mA
I_{IOK}	DC input or output diode current		–	±20	mA
T_{amb}	operating ambient temperature		−20	+70	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. This maximum value refers to 5 V tolerant I/Os and may be 6 V maximum but only when V_{DD} is present.

22 CHARACTERISTICS

V_{DD} = 3.3 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDX}	any supply voltage (V_{DD} to V_{SS})		3.0	3.3	3.6	V
I_{DDP}	periphery supply current	note 1	1	–	–	mA
I_{DDC}	core supply current		–	15	18	mA
$I_{DDC(id)}$	Idle mode core supply current		–	4.6	6	mA
$I_{DDC(pd)}$	Power-down mode core supply current		–	0.76	1	mA
$I_{DDC(stb)}$	Standby mode core supply current		–	5.11	6.50	mA
I_{DDA}	analog supply current		–	45	48	mA
$I_{DDA(id)}$	Idle mode analog supply current		–	0.87	1	mA
$I_{DDA(pd)}$	Power-down mode analog supply current		–	0.45	0.7	mA
$I_{DDA(stb)}$	Standby mode analog supply current		–	0.95	1.20	mA
Digital inputs						
RESET						
V_{IL}	LOW-level input voltage		–	–	1.34	V
V_{IH}	HIGH-level input voltage		1.49	–	5.5	V
V_{hys}	hysteresis voltage of Schmitt trigger input		0.44	–	0.58	V
I_{LI}	input leakage current	V_I = 0	–	–	0.17	µA
R_{pd}	equivalent pull-down resistance	$V_I = V_{DD}$	55.73	70.71	92.45	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HSYNC, VSYNC						
V_{IL}	LOW-level input voltage		–	–	1.31	V
V_{IH}	HIGH-level input voltage		1.44	–	5.5	V
V_{hys}	hysteresis voltage of Schmitt trigger input		0.40	–	0.56	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.00	µA
Digital outputs						
FRAME, VDS						
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.13	V
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	2.84	–	–	V
t_r	output rise time	10% to 90%; C_L = 70 pF	7.50	8.85	10.90	ns
t_f	output fall time	10% to 90%; C_L = 70 pF	6.70	7.97	10.00	ns
$\overline{COR}$ (OPEN-DRAIN OUTPUT)						
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.14	V
V_{OH}	HIGH-level pull-up output voltage	I_{OL} = –3 mA; push-pull	2.84	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.00	V
V_{IH}	HIGH-level input voltage		0.00	–	5.50	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.12	µA
t_r	output rise time	10% to 90%; C_L = 70 pF	7.20	8.64	11.10	ns
t_f	output fall time	10% to 90%; C_L = 70 pF	4.90	7.34	9.40	ns
Digital input/outputs						
P0.0 TO P0.4, P0.7, P1.0 TO P1.1, P2.1 TO P2.7, P3.0 TO P3.7						
V_{IL}	LOW-level input voltage		–	–	1.28	V
V_{IH}	HIGH-level input voltage		1.43	–	5.50	V
V_{hys}	hysteresis voltage of Schmitt trigger input		0.41	–	0.55	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.01	µA
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.18	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA; push-pull	2.81	–	5.50	V
t_r	output rise time	10% to 90%; C_L = 70 pF push-pull	6.50	8.47	10.70	ns
t_f	output fall time	10% to 90%; C_L = 70 pF	5.70	7.56	10.00	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P1.2, P1.3 AND P2.0						
V_{IL}	LOW-level input voltage		–	–	1.29	V
V_{IH}	HIGH-level input voltage		1.45	–	5.50	V
V_{hys}	hysteresis voltage of Schmitt trigger input		0.42	–	0.56	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.02	µA
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.17	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; push-pull	2.81	–	5.50	V
t_r	output rise time	10% to 90%; C_L = 70 pF; push-pull	7.00	8.47	10.50	ns
t_f	output fall time	10% to 90%; C_L = 70 pF	5.40	7.36	9.30	ns
P0.5 AND P0.6						
V_{IL}	LOW-level input voltage		–	–	1.28	V
V_{IH}	HIGH-level input voltage		1.43	–	5.50	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.11	µA
V_{hys}	hysteresis voltage of Schmitt trigger input		0.42	–	0.58	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	–	–	0.20	V
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; push-pull	2.76	–	5.50	V
t_r	output rise time	10% to 90%; C_L = 70 pF; push-pull	7.40	8.22	8.80	ns
t_f	output fall time	10% to 90%; C_L = 70 pF	4.20	4.57	5.20	ns
P1.4 TO P1.7 (OPEN-DRAIN)						
V_{IL}	LOW-level input voltage		–	–	1.45	V
V_{IH}	HIGH-level input voltage		1.62	–	5.50	V
V_{hys}	hysteresis voltage of Schmitt trigger input		0.49	–	0.60	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.13	µA
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	–	–	0.35	V
t_f	output fall time	10% to 90%; C_L = 70 pF	69.70	83.67	103.30	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
CVBS0 AND CVBS1						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
Z_{source}	source impedance		0	–	250	Ω
V_{IH}	HIGH-level input voltage		3.0	–	V_{DDA} + 0.3	V
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground	resistor tolerance 2%	–	24	–	kΩ
ADC0 TO ADC3						
V_{IH}	HIGH-level input voltage		–	–	V_{DDA}	V
C_I	input capacitance		–	–	10	pF
VPE						
V_{IH}	HIGH-level input voltage		–	–	9.0	V
Analog outputs						
R, G AND B						
I_{OL}	output current (black Level)	V_{DDA} = 3.3 V	−10	–	+10	μA
I_{OH}	output current (maximum Intensity)	V_{DDA} = 3.3 V Intensity level code = 15 dec	6.0	6.67	7.3	mA
	output current (70% of full Intensity)	V_{DDA} = 3.3 V Intensity level code = 0 dec	4.2	4.7	5.1	mA
R_{load}	load resistor to V_{SSA}	resistor tolerance 5%	–	150	–	Ω
C_L	load capacitance		–	–	15	pF
Analog input/output						
SYNC_FILTER						
C_{sync}	storage capacitor to ground		–	100	–	nF
V_{sync}	sync filter level voltage for nominal sync amplitude		0.35	0.55	0.75	V
Crystal oscillator						
XTALIN						
V_{IL}	LOW-level input voltage		V_{SSA}	–	–	V
V_{IH}	HIGH-level input voltage		–	–	V_{DDA}	V
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
XTALOUT						
C_O	output capacitance		–	–	10	pF
Crystal specification; notes 2 and 3						
f_{xtal}	nominal frequency	fundamental mode	–	12	–	MHz
C_L	crystal load capacitance		–	-	30	pF
C_1	crystal motional capacitance	T_{amb} = 25 °C	–	–	20	fF
R_r	resonance resistance	T_{amb} = 25 °C	–	–	60	Ω
C_{osc}	capacitors at XTALIN, XTALOUT	T_{amb} = 25 °C	–	note 4	–	pF
C_0	crystal holder capacitance	T_{amb} = 25 °C	–	–	note 5	pF
T_{xtal}	temperature range		−20	+25	+85	°C
X_j	adjustment tolerance	T_{amb} = 25 °C	–	–	$\pm 50 \times 10^{-6}$	
X_d	drift		–	–	$\pm 100 \times 10^{-6}$	

Notes

1. Peripheral current is dependent on external components and voltage levels on I/Os.
2. Crystal order number 4322 143 05561.
3. If the 4322 143 05561 crystal is not used, then the formulae in the crystal specification should be used. Where C_{IO} = 7 pF, the mean of the capacitances due to the chip at XTALIN and at XTALOUT. C_{ext} is a value for the mean of the stray capacitances due to the external circuit at XTALIN and XTALOUT. The maximum value for the crystal holder capacitance is to ensure start-up, C_{osc} may need to be reduced from the initially selected value.
4. $C_{osc(typ)} = 2C_L - C_{IO} - C_{ext}$
5. $C_{0(max)} = 35 - \frac{1}{2}(C_{osc} + C_{IO} + C_{ext})$

22.1 I²C-bus characteristics

Table 25 I²C-bus characteristics

SYMBOL	PARAMETER	FAST-MODE I²C-bus		UNIT
		MIN.	MAX.	
f_{SCL}	SCL clock frequency	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition	1.3	–	µs
$t_{HD;STA}$	hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock	0.6	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition	0.6	–	µs
$t_{HD;DAT}$	data hold time; notes 1 and 2	0	0.9	µs
$t_{SU;DAT}$	data set-up time, note 3	100	–	ns
t_r	rise time of both SDA and SCL signals	20	300	ns
t_f	fall time of both SDA and SCL signals	20	300	ns
$t_{SU;STO}$	set-up time for STOP condition	0.6	–	µs
C_b	capacitive load for each bus line	–	400	pF

Notes

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IL(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
2. The maximum $f_{HD;DAT}$ has only to be met if the device does not stretch the LOW period t_{LOW} of the SCL signal.
3. A fast-mode I²C-bus device can be used in a standard mode I²C-bus system but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 + 1250$ ns (according to the standard mode I²C-bus specification) before the SCL line is released.

23 QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*. The principal requirements are shown in Tables 26 to 29.

23.1 Group A

Table 26 Acceptance tests per lot

TEST	REQUIREMENTS(1)
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <100 ppm

Note

1. ppm = fraction of defective devices, in parts per million.

23.2 Group B

Table 27 Processability tests (by package family)

TEST	REQUIREMENTS
Solderability	0/16 on all lots
Mechanical	0/15 on all lots
Solder heat resistance	0/15 on all lots

23.3 Group C

Table 28 Reliability tests (by process family)

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	<1000 FPM at T_j = 150 °C
Humidity life	temperature, humidity, bias 1000 hours, 85 °C, 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Note

1. FPM = fraction of devices failing at test condition, in Failures Per Million.

Table 29 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD Human body model 100 pF, 1.5 kΩ	2000 V
	ESD Machine model 200 pF, 0 Ω	200 V
	latch-up	100 mA, 1.5 × V_{DD} (absolute maximum)

24 APPLICATION INFORMATION

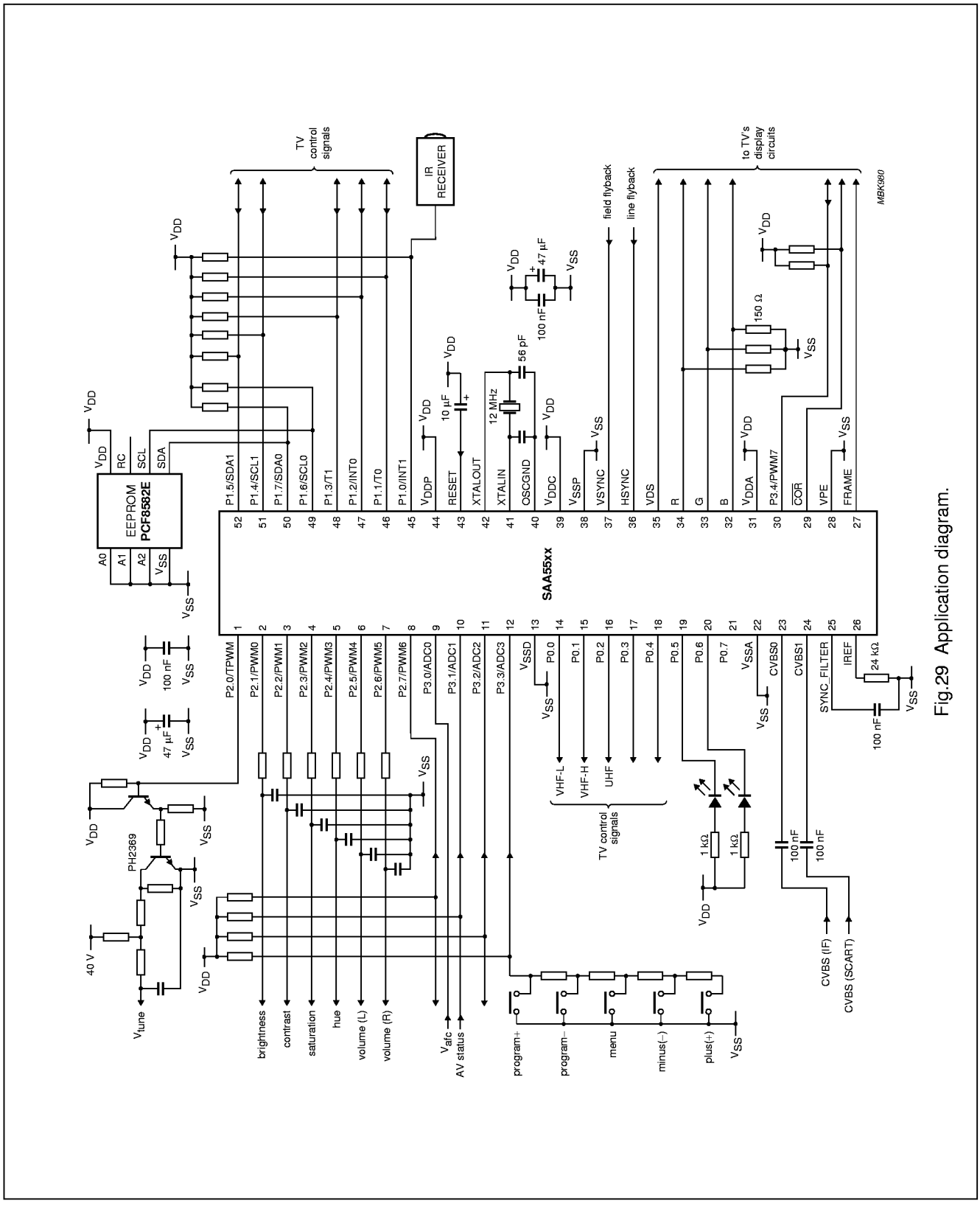


Fig.29 Application diagram.

25 ELECTROMAGNETIC COMPATIBILITY (EMC) GUIDELINES

Optimization of circuit return paths and minimisation of common mode emission will be assisted by using a double sided Printed-Circuit Board (PCB) with low inductance ground plane.

On a single sided printed-circuit board a local ground plane under the whole Integrated Circuit (IC) should be present as shown in Fig.30. This should be connected by the widest possible connection back to the printed-circuit board ground connection, and bulk electrolytic decoupling capacitor. It should preferably not connect to other grounds on the way, and no wire links should be present in this connect. The use of wire links increases ground bounce by introducing inductance into the ground.

The supply pins can be decoupled at the pin to the ground plane under the IC. This is easily accomplished using surface mount capacitors, which are more effective than leaded components at high frequency.

Using a device socket will unfortunately add to the area and inductance of the external bypass loop.

A ferrite bead or inductor with resistive characteristics at high frequencies may be utilised in the supply line close to the decoupling capacitor to provide a high impedance. To prevent pollution by conduction onto the signal lines (which may then radiate) signals connected to the V_{DD} supply via a pull-up resistor should not be connected to the IC side of this ferrite component.

OSCGND should be connected only to the crystal load capacitors and not to the local or circuit ground.

Physical connection distances to associated active devices should be short.

Output traces should be routed with close proximity to mutually coupled ground return paths.

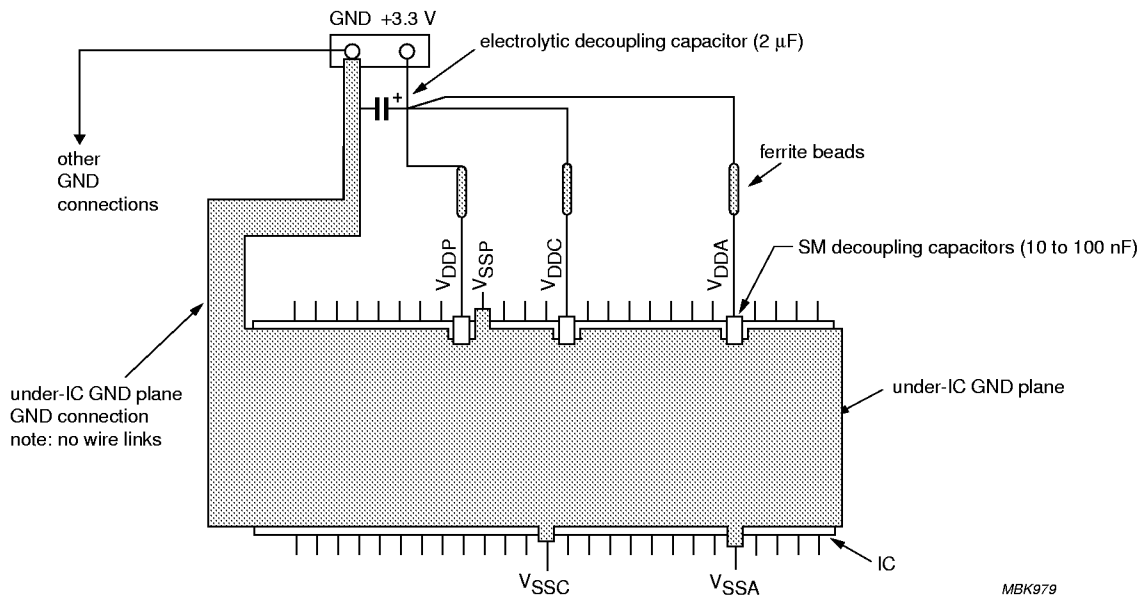
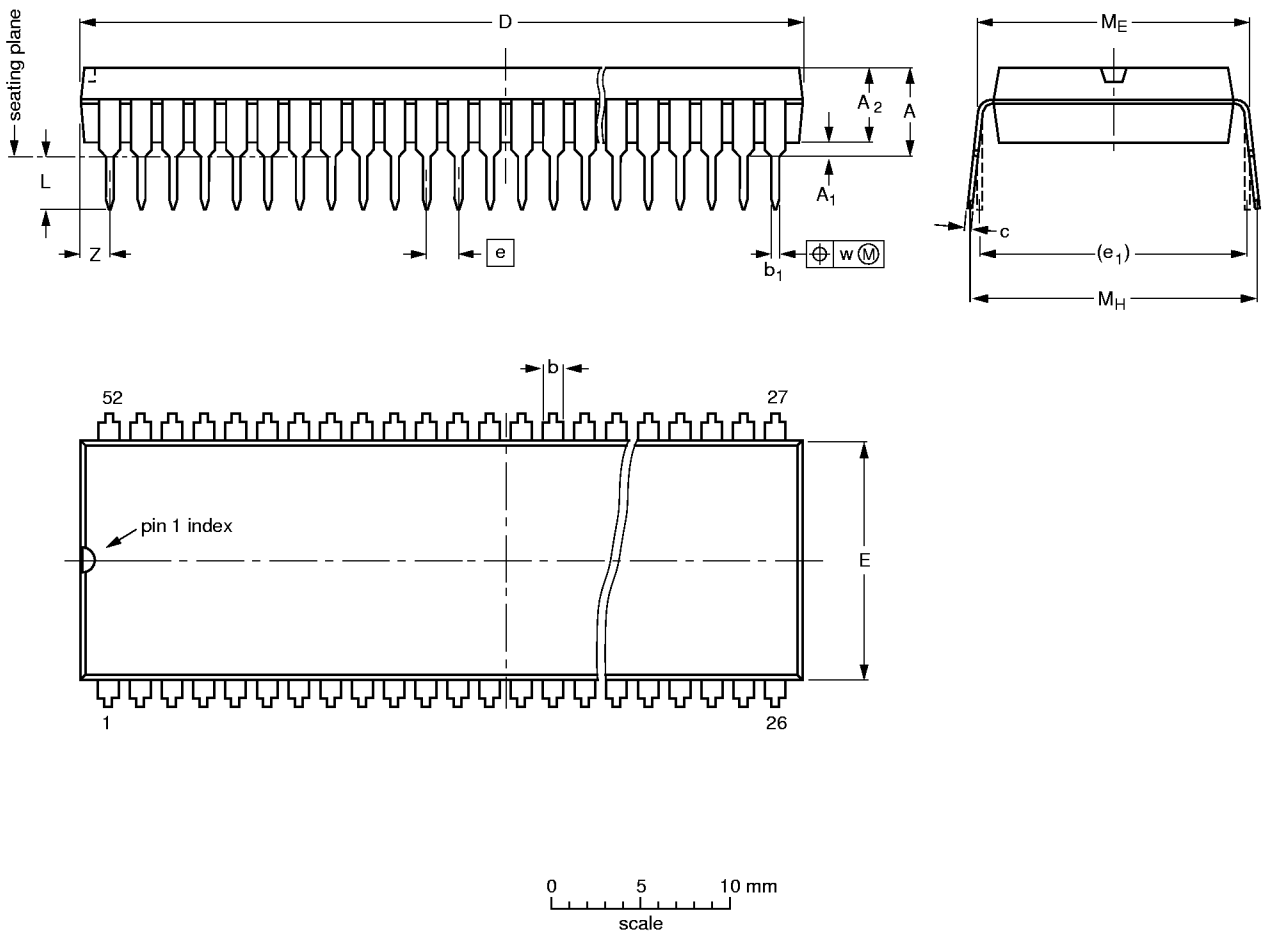


Fig.30 Power supply connections for EMC.

26 PACKAGE OUTLINES

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

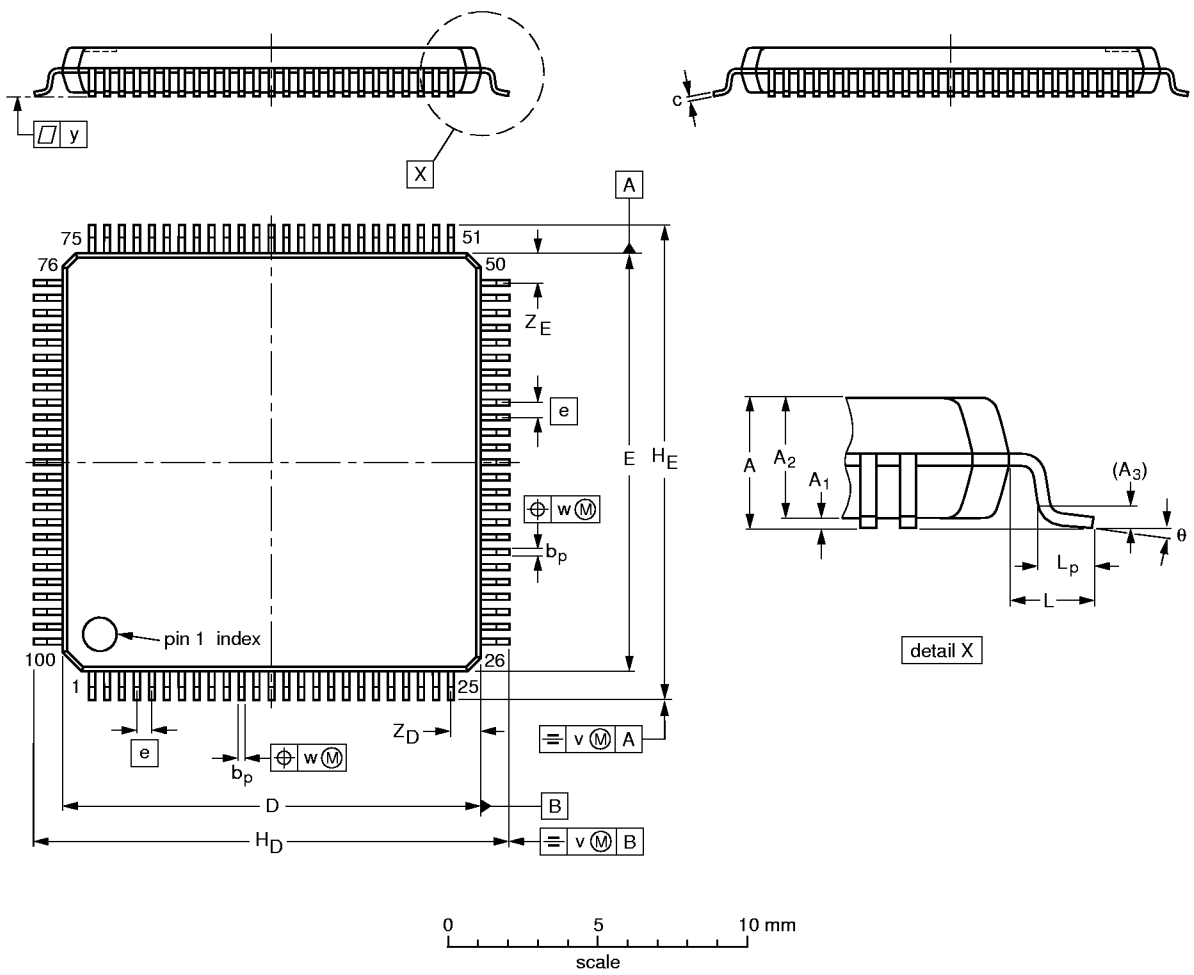
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

27 SOLDERING

27.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

27.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

27.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

27.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.