M28335

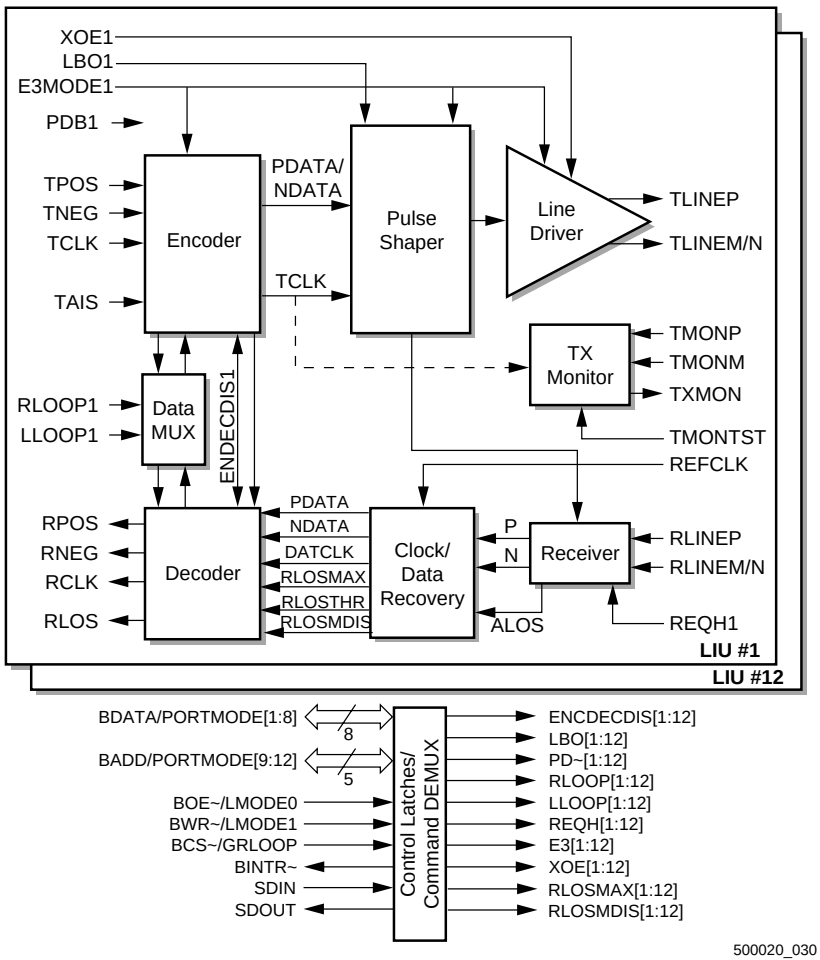
Twelve Port T3/E3/STS-1 Line Interface Unit

The M28335 is a 12-channel, T3/E3/STS-1 Line Interface Unit (LIU). It can be configured via Parallel, Serial (SPI) microprocessor interface or through hardware control pins. Each channel includes an independent receive equalizer that requires no user configuration. Additionally, each channel has a programmable transmit pulse shaper that can be set to ensure that the transmit pulse meets the pulse mask requirement for the digital cross-connect. The M28335 achieves a typical reach of 1275 feet when working at DS3/E3 rates, allowing designers greater margin and flexibility in the design of high performance system solutions.

The M28335 provides the user new economies of scale in Metro-optical Access Switch applications where 12 DS3 or STS-1 channels are aggregated into an OC12/OC48 connection on a single line card. Significant elimination of external components is achieved by including twelve independent transceivers in one package.

The line interface is reduced to 1:1 coupling transformers, termination resistors, and supply bypass capacitors.

Functional Block Diagram



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Distinguishing Features

- Programmable pulse shaper to meet cross-connect pulse masks (*ANSI T1.102-1993*)
- SRAM-like 8-bit parallel microprocessor interface
- Serial Peripheral Interface (SPI) support
- Meets jitter tolerance and jitter generation specifications of *Bellcore GR499*, *GR253*, and *ETSI TBR24*
- Alarms for coding violation and loss of signal
- Full diagnostic loopback capability
- Uses a minimum of external components
- Compliant with *ITU-T G.703* and *ETSI TBR24*
- Independent power-down mode per channel
- Easily interfaced to the T3/E3 framer ICs (CX28342/3/4/6/8 and CX28365)
- Selectable B3ZS/HDB3 encoding/decoding
- Superior input receiver sensitivity (<25 mV peak)
- Transmit monitor inputs for a faulty transmit or shorted output
- Programmable RLOS threshold

Physical Characteristics

- 580-ball, 35 mm TBGA package
- Single 3.3 V power supply
- –40 °C to +85 °C temperature range
- 5 V-tolerant pins
- TTL digital pins

Applications

- Digital cross-connect systems
- High-end routers
- Multi-service ATM switches
- Optical add-drop multiplexers
- Metro-optical Access Switches

Ordering Information

Model Number	Package	Description	Operating Temperature
Direct: M28335-13 Distributors: M28335EBGC	580-pin 35 mm TBGA	Twelve Port T3/E3/STS-1 LIU	–40 °C to +85 °C

Revision History

Revision	Level	Date	Description
A	Advance	February 2001	Initial release.
B	Advance	May 2001	Changed document number from 101487B to 500020B. Added pin number information in M28335 Pin Definitions table. Misc. updates.
C	Advance	October 2001	Updated register map and RLOS information.
D	Advance	December 2001	Added SPI definition.
E	Preliminary	May 2002	Incorporated Errata document number 500297C. Improved description of the device. Added new diagrams. General corrections.
F	Preliminary	May 2002	Corrected diagrams; minor updates.
G	Preliminary	August 2002	Corrected BMODE settings in Table 1-1 pin descriptions. Updated electrical characteristics. Corrected LBO distance setting in Section 3.3. Removed multidevice transmit monitor connection diagram. General corrections.
B	Released	February 2003	- Corrected transmit AIS operation during loopback. - Fixed E3 transmit pulse mask, Figure 2-7. - Added requirement that a hard reset be performed after power-up in bus and serial modes. - Added DS3/E3 and STS-1 electrical characteristics tables. - Updated PCB design considerations. - Added power sequencing requirements between VGG and VDD. - General corrections. - Assigned new document number and released as 28335-DSH-001-B.

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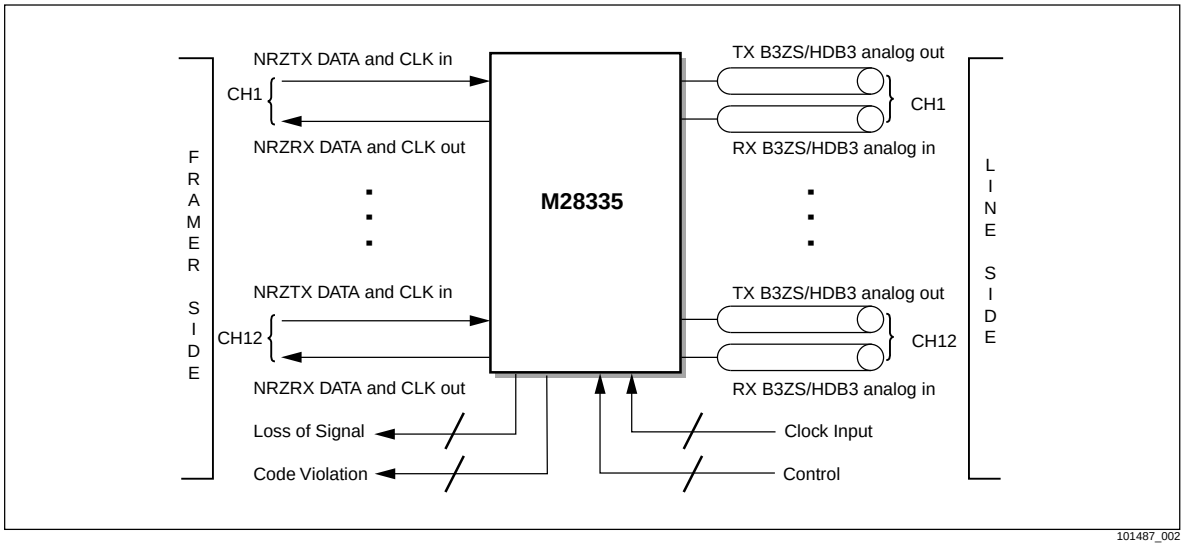
NRZTX DATA and CLK in
CH1
NRZRX DATA and CLK out
NRZTX DATA and CLK in
CH12
NRZRX DATA and CLK out
Loss of Signal
Code Violation
M28335
TX B3ZS/HDB3 analog out
CH1
RX B3ZS/HDB3 analog in
TX B3ZS/HDB3 analog out
CH12
RX B3ZS/HDB3 analog in
Clock Input
Control
FRAMER SIDE
LINE SIDE
101487_002

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1.0 Pin Description

1.1 Pin Assignments

The M28335 is packaged in a 580-ball TBGA package. Figure 1-1 illustrates the complete view of the ballout, as seen from the bottom.

Figure 1-1. Bottom View of the M28335

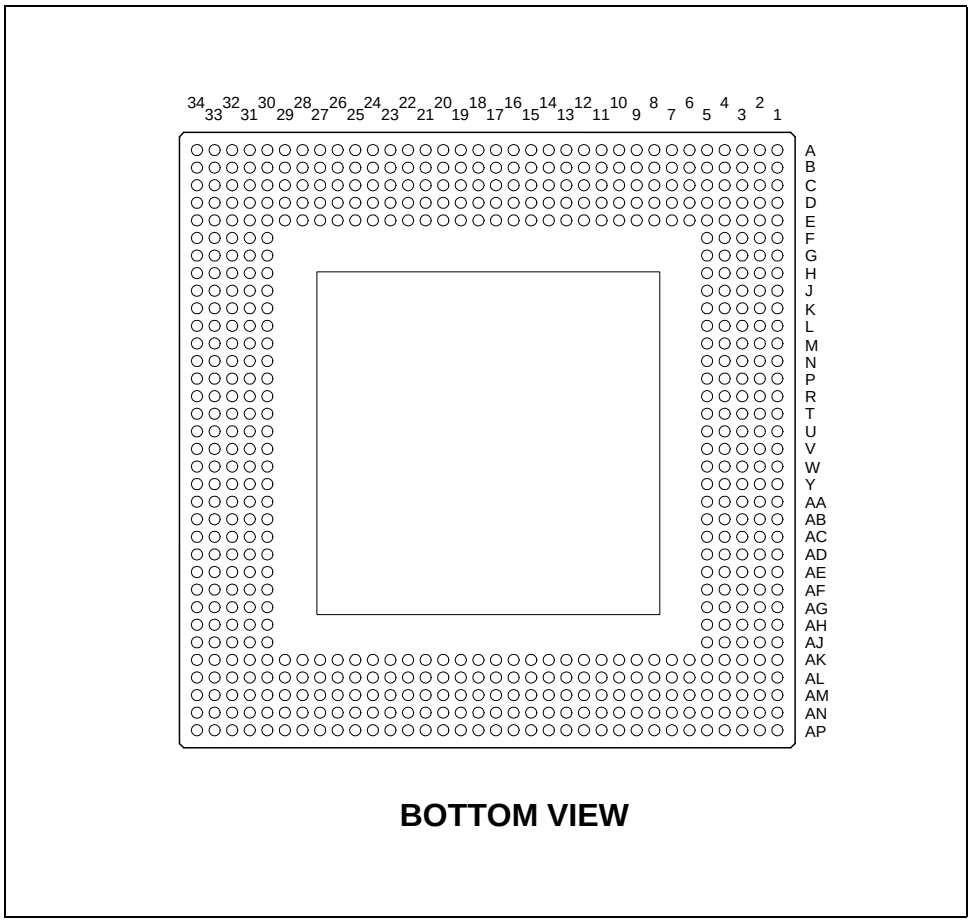


Table 1-1 lists the M28335 pin descriptions. The Input/Output (I/O) column is coded as follows:

I = Input

O = Output

I/O = Bidirectional

P = Power

NOTE: All digital inputs and outputs contain 75 kΩ pull-down resistors.

When a channel is disabled, all receive and transmit analog circuitry powers down. Analog inputs (RLINE) are ignored and analog outputs (TLINE) are high impedance. Digital inputs of a powered-down channel are still active, but ignored. Overall noise on the device can be lowered by not driving the digital inputs of a powered-down channel.

NOTE: When a channel is reverted from power-down to normal operation, TLINE pins are low impedance to ground if driven by more than one forward-bias diode voltage (0.7 V) below ground. Additionally, driving TLINE, a forward-bias diode voltage above the VGG pin, creates a low impedance path from the TLINE pin to the VGG pin. Otherwise, the TLINE pins are high impedance.

Table 1-1. M28335 Pin Definitions (1 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
Coaxial Line Pins				
H33	RLINE1P	Ch 1 positive receive data	I	Differential inputs for each channel from its respective receive coax line. The RX expects balanced differential inputs, usually achieved using a 1:1 transformer. The inputs are internally DC biased to 1.9 V.
H34	RLINE1M	Ch 1 negative receive data	I	
M33	RLINE2P	Ch 2 positive receive data	I	
M34	RLINE2M	Ch 2 negative receive data	I	
R33	RLINE3P	Ch 3 positive receive data	I	
R34	RLINE3M	Ch 3 negative receive data	I	
J3	RLINE4P	Ch 4 positive receive data	I	
J2	RLINE4M	Ch 4 negative receive data	I	
M2	RLINE5P	Ch 5 positive receive data	I	
M1	RLINE5M	Ch 5 negative receive data	I	
T4	RLINE6P	Ch 6 positive receive data	I	
T3	RLINE6M	Ch 6 negative receive data	I	
AF33	RLINE7P	Ch 7 positive receive data	I	
AF34	RLINE7M	Ch 7 negative receive data	I	
AC32	RLINE8P	Ch 8 positive receive data	I	
AC33	RLINE8M	Ch 8 negative receive data	I	
Y33	RLINE9P	Ch 9 positive receive data	I	
Y34	RLINE9M	Ch 9 negative receive data	I	
AF4	RLINE10P	Ch 10 positive receive data	I	
AF3	RLINE10M	Ch 10 negative receive data	I	
AC4	RLINE11P	Ch 11 positive receive data	I	
AC3	RLINE11M	Ch 11 negative receive data	I	
Y3	RLINE12P	Ch 12 positive receive data	I	
Y2	RLINE12M	Ch 12 negative receive data	I	

Table 1-1. M28335 Pin Definitions (2 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
F33	TLINE1P	Ch 1 positive transmit data	O	Differential, coax-driver balanced outputs for pulse-shaped AMI B3ZS/HDB3 encoded waveforms for each channel. These pins should be connected to the primary side of the 1:1 transformer through two backmatch resistors.
F34	TLINE1M	Ch 1 negative transmit data	O	
K32	TLINE2P	Ch 2 positive transmit data	O	
K31	TLINE2M	Ch 2 negative transmit data	O	
P31	TLINE3P	Ch 3 positive transmit data	O	
P32	TLINE3M	Ch 3 negative transmit data	O	
G4	TLINE4P	Ch 4 positive transmit data	O	
G3	TLINE4M	Ch 4 negative transmit data	O	
L4	TLINE5P	Ch 5 positive transmit data	O	
L3	TLINE5M	Ch 5 negative transmit data	O	
P2	TLINE6P	Ch 6 positive transmit data	O	
P1	TLINE6M	Ch 6 negative transmit data	O	
AG31	TLINE7P	Ch 7 positive transmit data	O	
AG32	TLINE7M	Ch 7 negative transmit data	O	
AD31	TLINE8P	Ch 8 positive transmit data	O	
AD32	TLINE8M	Ch 8 negative transmit data	O	
AA31	TLINE9P	Ch 9 positive transmit data	O	
AA32	TLINE9M	Ch 9 negative transmit data	O	
AH4	TLINE10P	Ch 10 positive transmit data	O	
AH3	TLINE10M	Ch 10 negative transmit data	O	
AE3	TLINE11P	Ch 11 positive transmit data	O	
AE1	TLINE11M	Ch 11 negative transmit data	O	
AA4	TLINE12P	Ch 12 positive transmit data	O	
AA3	TLINE12M	Ch 12 negative transmit data	O	

Table 1-1. M28335 Pin Definitions (3 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
Digital Data Pins				
C27	RPOS1/RNRZ1	Ch 1 receive positive rail or NRZ data	O	Resynchronized receive data intended to be strobed out by the corresponding RCLK. When ENDECDIS = 1, these outputs are positive and negative AMI data (RPOS and RNEG). When ENDECDIS = 0, these outputs are decoded NRZ data (RNRZ) and line code violation (RLCV). A line code violation is indicated when RLCV = 1. See notes on the ENDECDIS pin in Section 2.3.1.
D27	RNEG1/RLCV1	Ch 1 receive negative rail or line code violation	O	
B24	RPOS2/RNRZ2	Ch 2 receive positive rail or NRZ data	O	
C24	RNEG2/RLCV2	Ch 2 receive negative rail or line code violation	O	
B21	RPOS3/RNRZ3	Ch 3 receive positive rail or NRZ data	O	
C21	RNEG3/RLCV3	Ch 3 receive negative rail or line code violation	O	
A7	RPOS4/RNRZ4	Ch 4 receive positive rail or NRZ data	O	
C7	RNEG4/RLCV4	Ch 4 receive negative rail or line code violation	O	
D11	RPOS5/RNRZ5	Ch 5 receive positive rail or NRZ data	O	
A10	RNEG5/RLCV5	Ch 5 receive negative rail or line code violation	O	
B14	RPOS6/RNRZ6	Ch 6 receive positive rail or NRZ data	O	
C14	RNEG6/RLCV6	Ch 6 receive negative rail or line code violation	O	
AN27	RPOS7/RNRZ7	Ch 7 receive positive rail or NRZ data	O	
AM27	RNEG7/RLCV7	Ch 7 receive negative rail or line code violation	O	
AL23	RPOS8/RNRZ8	Ch 8 receive positive rail or NRZ data	O	
AP24	RNEG8/RLCV8	Ch 8 receive negative rail or line code violation	O	
AN20	RPOS9/RNRZ9	Ch 9 receive positive rail or NRZ data	O	
AM20	RNEG9/RLCV9	Ch 9 receive negative rail or line code violation	O	
AM7	RPOS10/RNRZ10	Ch 10 receive positive rail or NRZ data	O	
AL7	RNEG10/RLCV10	Ch 10 receive negative rail or line code violation	O	
AM10	RPOS11/RNRZ11	Ch 11 receive positive rail or NRZ data	O	
AL10	RNEG11/RLCV11	Ch 11 receive negative rail or line code violation	O	
AM14	RPOS12/RNRZ12	Ch 12 receive positive rail or NRZ data	O	
AL14	RNEG12/RLCV12	Ch 12 receive negative rail or line code violation	O	
B27	RCLK1	Receive Clock Ch1	O	Recovered clock for each channel receiver, intended for strobing the corresponding RDAT into the following framer or logic.
A24	RCLK2	Receive Clock Ch2	O	
A21	RCLK3	Receive Clock Ch3	O	
D8	RCLK4	Receive Clock Ch4	O	
C11	RCLK5	Receive Clock Ch5	O	
A14	RCLK6	Receive Clock Ch6	O	
AP27	RCLK7	Receive Clock Ch7	O	
AM23	RCLK8	Receive Clock Ch8	O	
AP20	RCLK9	Receive Clock Ch9	O	
AP7	RCLK10	Receive Clock Ch10	O	
AP10	RCLK11	Receive Clock Ch11	O	
AN14	RCLK12	Receive Clock Ch12	O	

Table 1-1. M28335 Pin Definitions (4 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
D25	TPOS1	Ch 1 transmit Positive rail or NRZ data	I	Synchronized transmit data intended to be strobed in by the corresponding TCLK. When ENDECDIS = 1, these inputs are expected to be positive and negative AMI data (TPOS and TNEG). When ENDECDIS = 0, these inputs are expected to be uncoded NRZ data (TNRZ) and no connects (NC). See notes on the ENDECDIS pin in Section 2.3.1.
A26	TNEG1/NC1	Ch 1 transmit negative rail or no connect data	I	
D22	TPOS2	Ch 2 transmit Positive rail or NRZ data	I	
A23	TNEG2/NC2	Ch 2 transmit negative rail or no connect data	I	
C19	TPOS3	Ch 3 transmit Positive rail or NRZ data	I	
A20	TNEG3/NC3	Ch 3 transmit negative rail or no connect data	I	
B9	TPOS4	Ch 4 transmit Positive rail or NRZ data	I	
C9	TNEG4/NC4	Ch 4 transmit negative rail or no connect data	I	
D13	TPOS5	Ch 5 transmit Positive rail or NRZ data	I	
A12	TNEG5/NC5	Ch 5 transmit negative rail or no connect data	I	
C16	TPOS6	Ch 6 transmit Positive rail or NRZ data	I	
D16	TNEG6/NC6	Ch 6 transmit negative rail or no connect data	I	
AP25	TPOS7	Ch 7 transmit Positive rail or NRZ data	I	
AM25	TNEG7/NC7	Ch 7 transmit negative rail or no connect data	I	
AL21	TPOS8	Ch 8 transmit Positive rail or NRZ data	I	
AP22	TNEG8/NC8	Ch 8 transmit negative rail or no connect data	I	
AN18	TPOS9	Ch 9 transmit Positive rail or NRZ data	I	
AM18	TNEG9/NC9	Ch 9 transmit negative rail or no connect data	I	
AL9	TPOS10	Ch 10 transmit Positive rail or NRZ data	I	
AP8	TNEG10/NC10	Ch 10 transmit negative rail or no connect data	I	
AP12	TPOS11	Ch 11 transmit Positive rail or NRZ data	I	
AN12	TNEG11/NC11	Ch 11 transmit negative rail or no connect data	I	
AL16	TPOS12	Ch 12 transmit Positive rail or NRZ data	I	
AM16	TNEG12/NC12	Ch 12 transmit negative rail or no connect data	I	
C25	TCLK1	Transmit Clock Ch 1	I	Transmit bit clock input for strobing with transmit data into the M28335.
C22	TCLK2	Transmit Clock Ch 2	I	
A19	TCLK3	Transmit Clock Ch 3	I	
A9	TCLK4	Transmit Clock Ch 4	I	
C13	TCLK5	Transmit Clock Ch 5	I	
A16	TCLK6	Transmit Clock Ch 6	I	
AL24	TCLK7	Transmit Clock Ch 7	I	
AM21	TCLK8	Transmit Clock Ch 8	I	
AP18	TCLK9	Transmit Clock Ch 9	I	
AM9	TCLK10	Transmit Clock Ch 10	I	
AL13	TCLK11	Transmit Clock Ch 11	I	
AP16	TCLK12	Transmit Clock Ch 12	I	

Table 1-1. M28335 Pin Definitions (5 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
A27	RLOS1	Loss of Signal Ch 1	0	Loss Of Signal (LOS) indication for each channel, as determined by insufficient pulse density. Signal loss detected when RLOS = 1. Loss of signal will be asserted and deasserted under the conditions discussed in Section 2.4.5.
D23	RLOS2	Loss of Signal Ch 2	0	
D20	RLOS3	Loss of Signal Ch 3	0	
C8	RLOS4	Loss of Signal Ch 4	0	
A11	RLOS5	Loss of Signal Ch 5	0	
C15	RLOS6	Loss of Signal Ch 6	0	
AM26	RLOS7	Loss of Signal Ch 7	0	
AN23	RLOS8	Loss of Signal Ch 8	0	
AL19	RLOS9	Loss of Signal Ch 9	0	
AL8	RLOS10	Loss of Signal Ch 10	0	
AM11	RLOS11	Loss of Signal Ch 11	0	
AL15	RLOS12	Loss of Signal Ch 12	0	
Control Signal				
A25	TAIS1	Transmit Ch 1 AIS mode enable	I	Transmission of Alarm Indication Signal (AIS) for a given channel. Replace transmit data with AIS signal. The AMI form of AIS supported is alternating 1s. (+1, –1, +1, –1, +1, ...) Transmit AIS overwrites data during local loopback. 1 = AIS mode enabled 0 = AIS mode disabled
D21	TAIS2	Transmit Ch 2 AIS mode enable	I	
B18	TAIS3	Transmit Ch 3 AIS mode enable	I	
D10	TAIS4	Transmit Ch 4 AIS mode enable	I	
D14	TAIS5	Transmit Ch 5 AIS mode enable	I	
A17	TAIS6	Transmit Ch 6 AIS mode enable	I	
AN24	TAIS7	Transmit Ch 7 AIS mode enable	I	
AP21	TAIS8	Transmit Ch 8 AIS mode enable	I	
AP17	TAIS9	Transmit Ch 9 AIS mode enable	I	
AN9	TAIS10	Transmit Ch 10 AIS mode enable	I	
AP13	TAIS11	Transmit Ch 11 AIS mode enable	I	
AL17	TAIS12	Transmit Ch 12 AIS mode enable	I	

Table 1-1. M28335 Pin Definitions (6 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
Bus Mode/Hardware Mode/Serial Mode Control Signals				
U3	BDATA0 /PORTMODE1 /SDOUT	Data 0/PORTMODE1/SDOUT	I/O	In Hardware mode (Pins BMODE[1:0] = 00), the pins are defined as PORTMODE[8:1], which select configurations for Port[8:1]. In Bus mode (Pins BMODE[1:0] = 10), the pins are defined as an eight bit bidirectional bus used for transferring data to and from the internal registers which set the configurations of the 12 ports. In Serial mode (Pins BMODE[1:0] = 11), SDIN is the serial data input from the Serial Master device. In Serial mode (Pins BMODE[1:0] = 11), SDOUT is the serial data output to the Serial Master device.
U4	BDATA1 /PORTMODE2 /SDIN	Data 1/PORTMODE2/SDIN	I/O	
U2	BDATA2 /PORTMODE3	Data 2/PORTMODE3	I/O	
U1	BDATA3 /PORTMODE4	Data 3/PORTMODE4	I/O	
V1	BDATA4 /PORTMODE5	Data 4/PORTMODE5	I/O	
V2	BDATA5 /PORTMODE6	Data 5/PORTMODE6	I/O	
V4	BDATA6 /PORTMODE7	Data 6/PORTMODE7	I/O	
V3	BDATA7 /PORTMODE8	Data 7/PORTMODE8	I/O	
T32	BADD0 /PORTMODE9	Address 0/PORTMODE9	I	In Hardware mode (Pins BMODE[1:0] = 00), the pins are defined as PORTMODE[12:9] which select configurations for Port[12:9]. In Bus mode (Pins BMODE[1:0] = 10), the pins are defined as four address lines to identify the internal register for a read/write data transfer cycle.
T34	BADD1 /PORTMODE10	Address 1/PORTMODE10	I	
U32	BADD2 /PORTMODE11	Address 2/PORTMODE11	I	
U31	BADD3 /PORTMODE12	Address 3/PORTMODE12	I	
V31	BADDR4 /TMONTST	Address 4/TX Monitor Test pin	I	In Hardware mode (Pins BMODE[1:0] = 00), it is defined as Tx monitor test pin which, when driven high, asserts all TLOS outputs. This is used to test board level functionality downstream from the TLOS outputs. In Bus mode (Pins BMODE[1:0] = 10), the pin is defined as address bit 4 for internal register access.
U34	BWR~/LMODE1	Data Bus Write Strobe /LMODE1	I	In Hardware mode (Pins BMODE[1:0] = 00), it is defined as one of the two pins LMODE0 and LMODE1 which are common control lines together with the PORTMODEx lines to control the configuration of the individual ports. In Bus mode (Pins BMODE[1:0] = 10), the pin indicates a write cycle when it is low.

Table 1-1. M28335 Pin Definitions (7 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
W1	BOE~/LMODE0 /SCLK	Data Bus Output Enable /LMODE0	I	In Hardware mode (Pins BMODE[1:0] = 00), it is defined as one of the two pins LMODE0 and LMODE1 which are common control lines together with the PORTMODEx lines to control the configuration of the individual ports. In Bus mode (Pins BMODE[1:0] = 10), the pin enables BDATA output during a read operation when active low. When high, the BDATA[7:0] is in high impedance state. In serial mode (Pins BMODE[1:0] = 11), SCLK is the serial clock input from the serial master device.
U33	BCS~/GRLOOP	Chip select /GRLOOP	I	In Hardware mode (Pins BMODE[1:0] = 00), it is defined as GRLOOP (global remote loopback). All twelve ports are placed in remote loopback when this pin is tied high. For normal operations, the GRLOOP should be tied low. In Bus mode (Pins BMODE[1:0] = 10), the pin serves as chip select. It enables a read/write operation when active low. When high, it ends the current read/write cycle and returns the BDATA[7:0] in high impedance state.
V33	BMODE0	Mode select 0	I	The two Mode Select pins control the device configuration mode as follows: BMODE1 BMODE0 Mode of Operation 0 0 Hardware Mode 0 1 Reserved (for factory test) 1 0 Bus Mode 1 1 Serial Mode In the Hardware mode (Pins BMODE[1:0] = 00), the control bus signals are redefined and the configuration of each channel is determined by its associated dedicated PORTMODE pins. In Bus mode (pins BMODE[1:0] = 10), the internal registers that control the operation of each port can be accessed through an SRAM-like parallel port. In Serial mode (pins BMODE[1:0] = 11), the Control Bus signals are redefined to support the SPI.
V34	BMODE1	Mode select 1	I	
W3	BINTR~	Interrupt	O/ OD	Open drain active low output signifies one or more pending alarm condition is detected and the INTEN bit (bit 1 address 0) is set.

Table 1-1. M28335 Pin Definitions (8 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
Miscellaneous				
D26	REFCLK1	Reference Clock for Ch 1	I	Reference clock from off-chip. The clock should be set to one of the following with all rates ±20 ppm tolerance: • E3 rate (34.368 MHz) • DS3 rate (44.736 MHz) • STS-1 rate (51.84 MHz) The clock rate should correspond to the mode of operation chosen for the channel.
C23	REFCLK2	Reference Clock for Ch 2	I	
C20	REFCLK3	Reference Clock for Ch 3	I	
B8	REFCLK4	Reference Clock for Ch 4	I	
D12	REFCLK5	Reference Clock for Ch 5	I	
B15	REFCLK6	Reference Clock for Ch 6	I	
AN26	REFCLK7	Reference Clock for Ch 7	I	
AL22	REFCLK8	Reference Clock for Ch 8	I	
AM19	REFCLK9	Reference Clock for Ch 9	I	
AM8	REFCLK10	Reference Clock for Ch 10	I	
AN11	REFCLK11	Reference Clock for Ch 11	I	
AM15	REFCLK12	Reference Clock for Ch 12	I	
C29	RBIASA	Bias Resistor A	O	Four 12.1 kΩ ± 1% resistors tied from each of these pins to ground to provide the current reference.(2)
D6	RBIASB	Bias Resistor B	O	
AN29	RBIASC	Bias Resistor C	O	
AL6	RBIASD	Bias Resistor D	O	
W34	RESET	Reset	I	Asynchronous reset (reset entire device).
V32	GPD	Global Power Down	I	Power down (Static Idd testing). 0 = Power down disable 1 = Power down active

Table 1-1. M28335 Pin Definitions (9 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
E34	TMON1P	Ch 1 transmit monitor positive input	I	Transmit monitor input pins are normally tied to their respective transmit line outputs, i.e., (TMON1P ⇒TLINE1P and TMON1M ⇒TLINE1M). Loss of signal outputs are active high when the monitor inputs detect no signal for 32 TCLK periods. The TX monitor test pin asserts all TLOS outputs when TMONTST is high. This is used to test board level functionality downstream from the TLOS outputs.
H32	TMON1M	Ch 1 transmit monitor negative input	I	
J33	TMON2P	Ch 2 transmit monitor positive input	I	
L32	TMON2M	Ch 2 transmit monitor negative input	I	
N34	TMON3P	Ch 3 transmit monitor positive input	I	
P34	TMON3M	Ch 3 transmit monitor negative input	I	
F2	TMON4P	Ch 4 transmit monitor positive input	I	
H2	TMON4M	Ch 4 transmit monitor negative input	I	
K3	TMON5P	Ch 5 transmit monitor positive input	I	
L1	TMON5M	Ch 5 transmit monitor negative input	I	
P4	TMON6P	Ch 6 transmit monitor positive input	I	
R3	TMON6M	Ch 6 transmit monitor negative input	I	
AH32	TMON7P	Ch 7 transmit monitor positive input	I	
AG33	TMON7M	Ch 7 transmit monitor negative input	I	
AE34	TMON8P	Ch 8 transmit monitor positive input	I	
AD33	TMON8M	Ch 8 transmit monitor negative input	I	
AB32	TMON9P	Ch 9 transmit monitor positive input	I	
AA34	TMON9M	Ch 9 transmit monitor negative input	I	
AJ1	TMON10P	Ch 10 transmit monitor positive input	I	
AG4	TMON10M	Ch 10 transmit monitor negative input	I	
AE4	TMON11P	Ch 11 transmit monitor positive input	I	
AD3	TMON11M	Ch 11 transmit monitor negative input	I	
AB3	TMON12P	Ch 12 transmit monitor positive input	I	
AA2	TMON12M	Ch 12 transmit monitor negative input	I	
B26	TLOS1	TX loss of signal Ch 1 output	O	
B23	TLOS2	TX loss of signal Ch 2 output	O	
B20	TLOS3	TX loss of signal Ch 3 output	O	
D9	TLOS4	TX loss of signal Ch 4 output	O	
B12	TLOS5	TX loss of signal Ch 5 output	O	
A15	TLOS6	TX loss of signal Ch 6 output	O	
AL25	TLOS7	TX loss of signal Ch 7 output	O	
AM22	TLOS8	TX loss of signal Ch 8 output	O	
AL18	TLOS9	TX loss of signal Ch 9 output	O	
AN8	TLOS10	TX loss of signal Ch 10 output	O	
AM12	TLOS11	TX loss of signal Ch 11 output	O	
AP15	TLOS12	TX loss of signal Ch 12 output	O	

Table 1-1. M28335 Pin Definitions (10 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
C28, A6, AP28, AN6, D28, D7, AL27, AP6,	FAC_TEST	Test pins.	NC	For factory test, leave unconnected.
Power/Ground				
G31	TVDD1	TX Power Ch 1	P	Power pins for transmit circuitry per channel (3.3 V).
L34	TVDD2	TX Power Ch 2	P	
R31	TVDD3	TX Power Ch 3	P	
H1	TVDD4	TX Power Ch 4	P	
M4	TVDD5	TX Power Ch 5	P	
R2	TVDD6	TX Power Ch 6	P	
AF31	TVDD7	TX Power Ch 7	P	
AD34	TVDD8	TX Power Ch 8	P	
Y31	TVDD9	TX Power Ch 9	P	
AG3	TVDD10	TX Power Ch 10	P	
AD2	TVDD11	TX Power Ch 11	P	
AA1	TVDD12	TX Power Ch 12	P	
F31	TVSS1	TX Ground Ch 1	P	Ground pins for transmit circuitry per channel.
J32	TVSS2	TX Ground Ch 2	P	
N32	TVSS3	TX Ground Ch 3	P	
F3	TVSS4	TX Ground Ch 4	P	
K4	TVSS5	TX Ground Ch 5	P	
N1	TVSS6	TX Ground Ch 6	P	
AH31	TVSS7	TX Ground Ch 7	P	
AE32	TVSS8	TX Ground Ch 8	P	
AB31	TVSS9	TX Ground Ch 9	P	
AJ2	TVSS10	TX Ground Ch 10	P	
AF1	TVSS11	TX Ground Ch 11	P	
AB4	TVSS12	TX Ground Ch 12	P	

Table 1-1. M28335 Pin Definitions (11 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
H31	RVDD1	RX Power Ch 1	P	Power pins for receive circuitry per channel (3.3 V). Connect to 3.3 V power.
M32	RVDD2	RX Power Ch 2	P	
R32	RVDD3	RX Power Ch 3	P	
J4	RVDD4	RX Power Ch 4	P	
M3	RVDD5	RX Power Ch 5	P	
R1	RVDD6	RX Power Ch 6	P	
AF32	RVDD7	RX Power Ch 7	P	
AC31	RVDD8	RX Power Ch 8	P	
Y32	RVDD9	RX Power Ch 9	P	
AG2	RVDD10	RX Power Ch 10	P	
AD1	RVDD11	RX Power Ch 11	P	
Y4	RVDD12	RX Power Ch 12	P	
J31	RVSS1	RX Ground Ch 1	P	Ground pins for receive circuitry per channel. Connect to ground.
N31	RVSS2	RX Ground Ch 2	P	
T31	RVSS3	RX Ground Ch 3	P	
J1	RVSS4	RX Ground Ch 4	P	
N3	RVSS5	RX Ground Ch 5	P	
T1	RVSS6	RX Ground Ch 6	P	
AE31	RVSS7	RX Ground Ch 7	P	
AC34	RVSS8	RX Ground Ch 8	P	
W32	RVSS9	RX Ground Ch 9	P	
AF2	RVSS10	RX Ground Ch 10	P	
AC1	RVSS11	RX Ground Ch 11	P	
W4	RVSS12	RX Ground Ch 12	P	
A29	VGGA	5 V/3.3 V ESD pin[(1)]	P	5 V supply for 5 V-tolerant, digital pad ESD diodes. No static power is drawn from pin.
B6	VGGB	5 V/3.3 V ESD pin[(1)]	P	
AM6	VGGC	5 V/3.3 V ESD pin[(1)]	P	
AM28	VGGD	5 V/3.3 V ESD pin[(1)]	P	

Table 1-1. M28335 Pin Definitions (12 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
E6, E10, E14, E18, E22, E26, F30, J5, K30, N5, P30, U5, V30, AA5, AB30, AE5, AF30, AJ5, AK4, AK9, AK13, AK17, AK21, AK25, AK29, AL30	DVDD	Power	P	Connect to 3.3 V power.

Table 1-1. M28335 Pin Definitions (13 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
A1, A2, A3, A4, A5, A8, A13, A18, A22, A28, A30, A31, A32, A33, A34, B1, B2, B3, B4, B5, B7, B10, B11, B13, B16, B17, B19, B22, B25, B28, B29, B30, B31, B32, B33, B34, C1, C2, C3, C4, C5, C6, C10, C12, C17, C18, C26, C30, C31, C32, C33, C34, D1, D2, D3, D4, D5, D15, D17, D18, D19, D24, D29, D30, D31, D32, D33, D34, E1, E2, E3, E4, E5, E7, E8, E9, E11, E12, E13, E15, E16, E17, E19, E20, E21, E23, E24, E25, E27, E28, E29, E30, E31, E32, E33, F1, F4, F5, F32, G1, G2, G5, G30, G32, G33, G34, H3,	GND	Ground	P	Connect to ground. (List continued on next page.)

Table 1-1. M28335 Pin Definitions (14 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
H4, H5, H30, J30, J34, K1, K2, K5, K33, K34, L2, L5, L30, L31, L33, M5, M30, M31, N2, N4, N30, N33, P3, P5, P33, R4, R5, R30, T2, T5, T30, T33, U30, V5, W2, W5, W30, W31, W33, Y1, Y5, Y30, AA30, AA33, AB1, AB2, AB5, AB33, AB34, AC2, AC5, AC30, AD4, AD5, AD30, AE2, AE30, AE33, AF5, AG1, AG5, AG30, AG34, AH1, AH2, AH5, AH30, AH33, AH34, AJ3, AJ4, AJ30, AJ31, AJ32, AJ33, AJ34, AK1, AK2, AK3,	GND	Ground	P	Connect to ground. (List continued on next page.)

Table 1-1. M28335 Pin Definitions (15 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
AK5, AK6, AK7, AK8, AK10, AK11, AK12, AK14, AK15, AK16, AK18, AK19, AK20, AK22, AK23, AK24, AK26, AK27, AK28, AK30, AK31, AK32, AK33, AK34, AL1, AL2, AL3, AL4, AL5, AL11, AL12, AL20, AL26, AL28, AL29, AL31, AL32, AL33, AL34, AM1, AM2, AM3, AM4, AM5, AM13, AM17, AM24, AM29, AM30, AM31, AM32, AM33, AM34, AN1, AN2, AN3, AN4, AN5, AN7, AN10, AN13,	GND	Ground	P	Connect to ground. (List continued on next page.)

Table 1-1. M28335 Pin Definitions (16 of 16)

Pin #	Signal Name	Description	I/O/P	Notes
AN15, AN16, AN17, AN19, AN21, AN22, AN25, AN28, AN30, AN31, AN32, AN33, AN34, AP1, AP2, AP3, AP4, AP5, AP9, AP11, AP14, AP19, AP23, AP26, AP29, AP30, AP31, AP32, AP33, AP34	GND	Ground	P	Connect to ground.

NOTES:

1. This pin should be connected to 3.3 V in an all-3.3 V design.
2. Placing a capacitor from this pin to ground may result in instabilities.

GENERAL NOTE: All digital input pins contain a 75 kΩ pull-down resistor from input to GND.

1.2 Logic Diagrams

Figure 1-2. Hardware Mode Logic Diagram

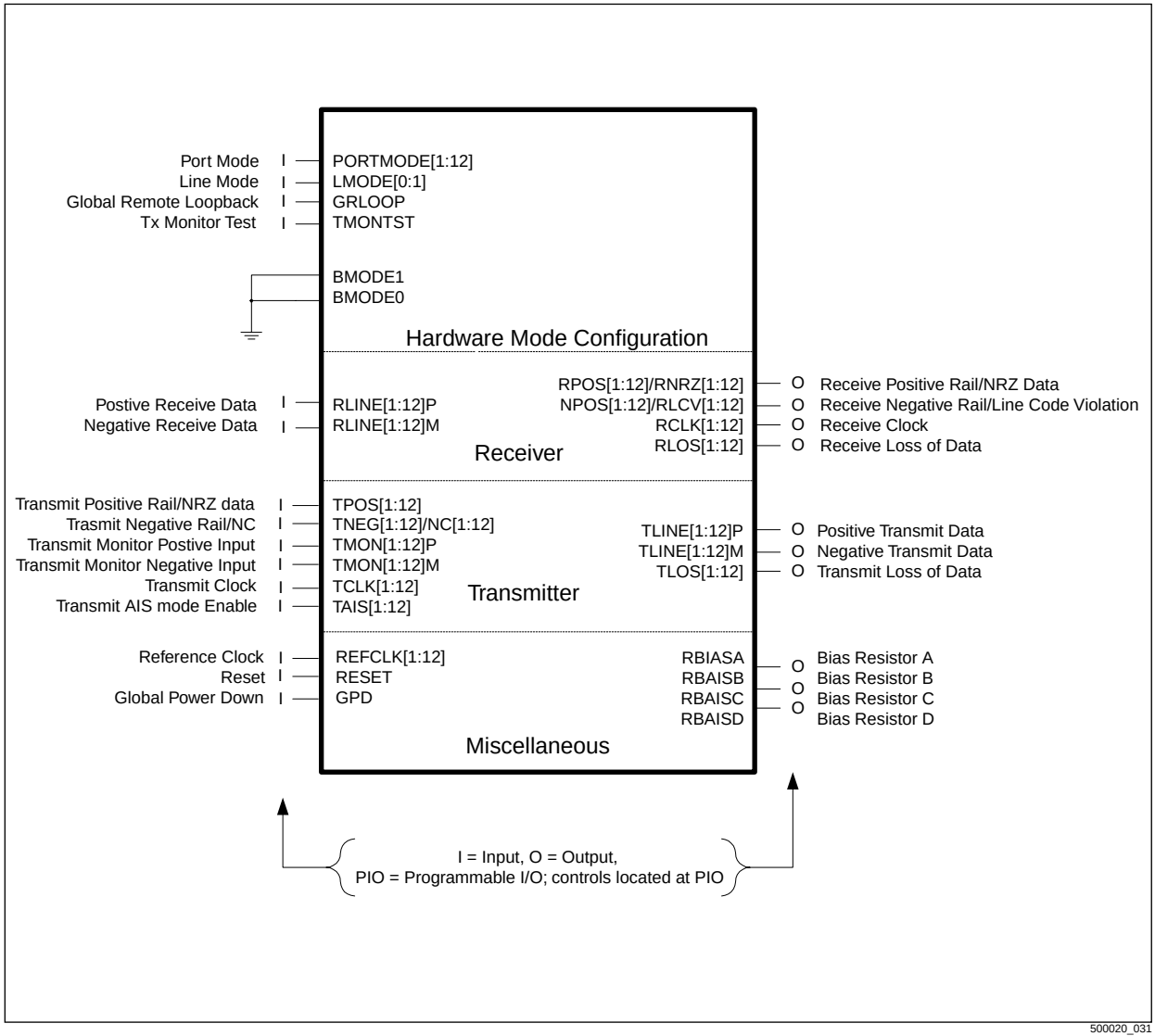


Figure 1-3. Bus Mode Logic Diagram

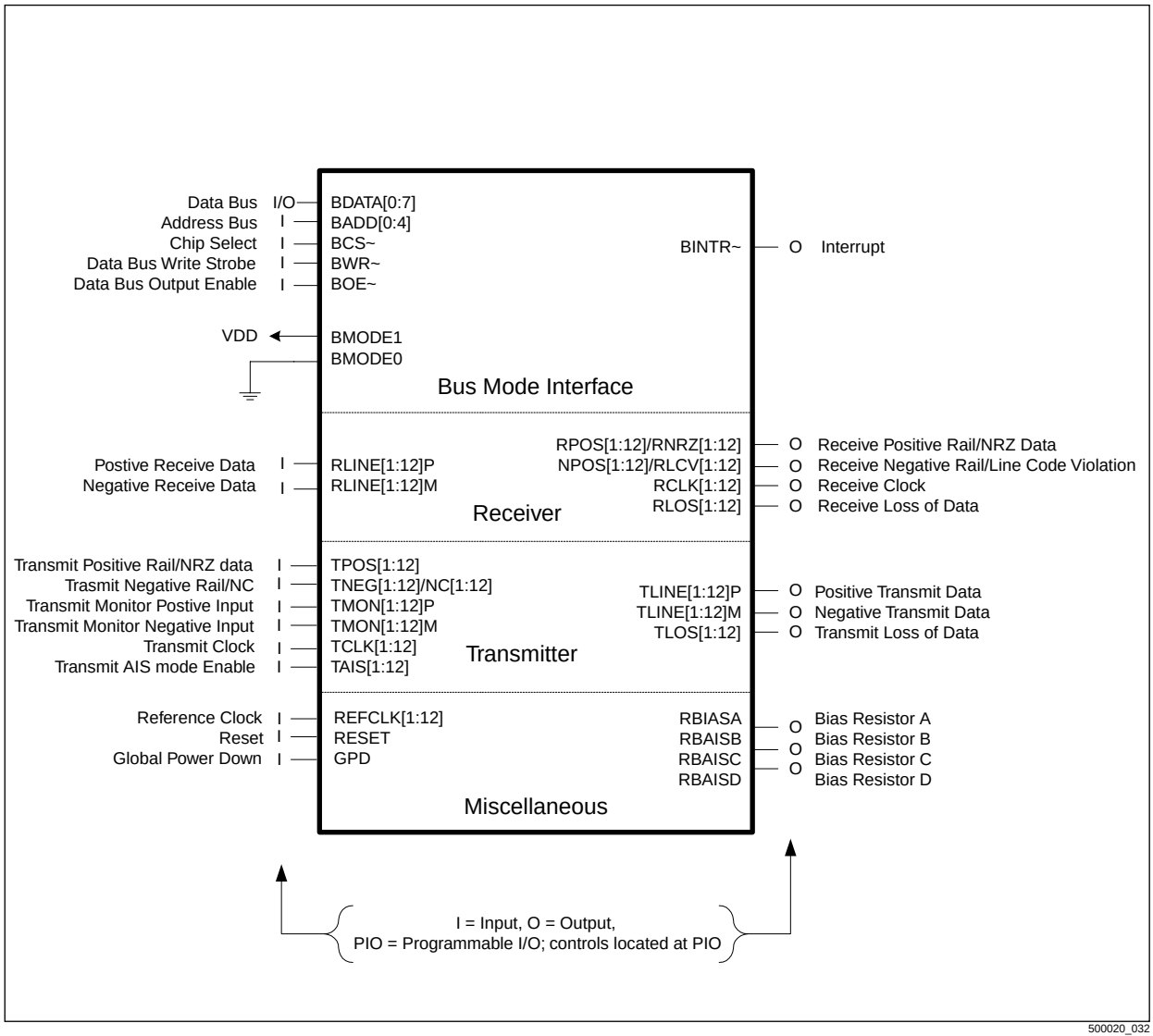
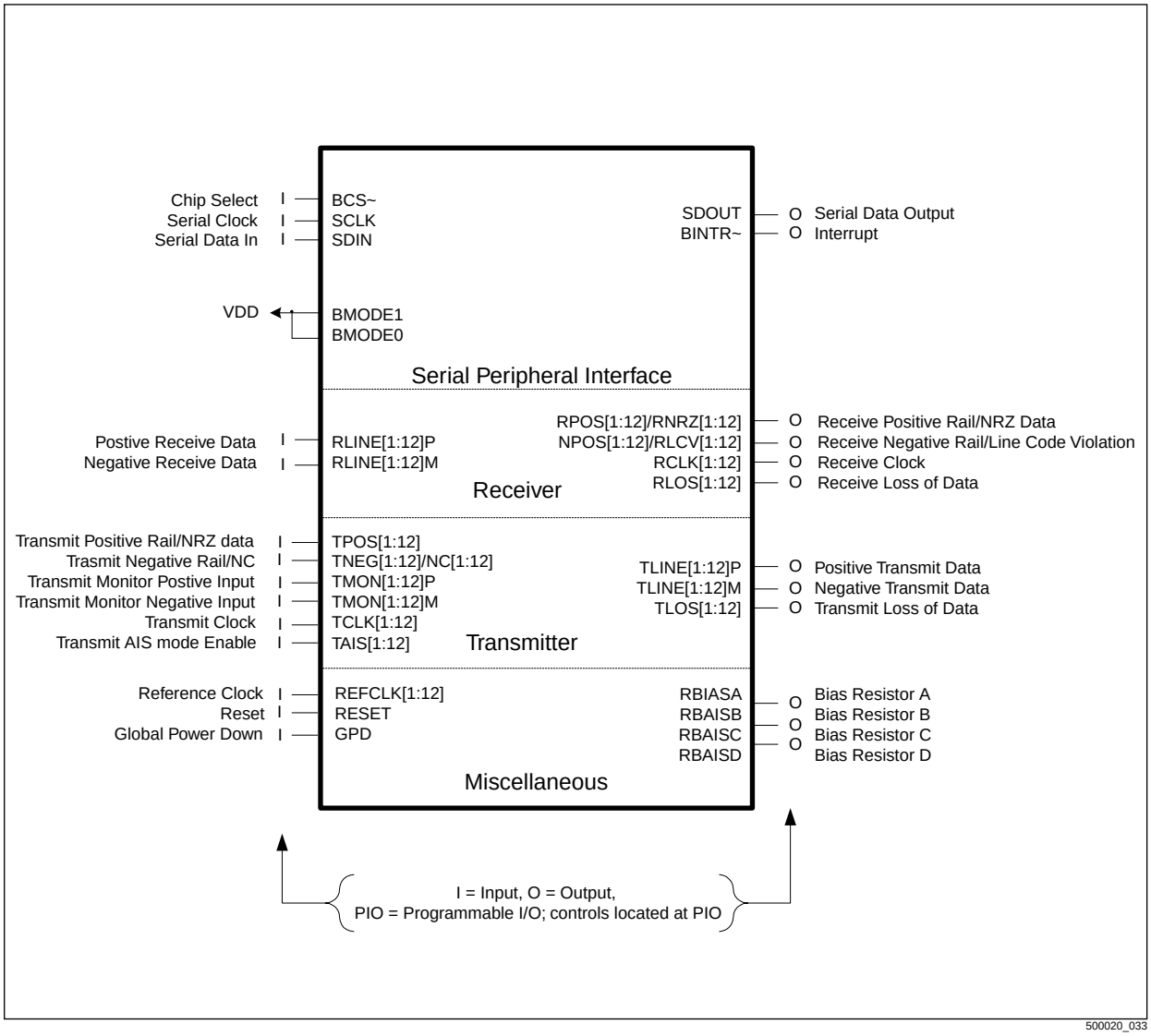


Figure 1-4. Serial Mode Logic Diagram



2.0 Functional Description

2.1 Overview

The M28335 is a 12-port E3/DS3/STS-1 Line Interface Unit (LIU). It is the physical layer interface between the data framer (or other terminal-side equipment) and the electrical cable used for data transmission.

The M28335 LIU consists of 12 independent data transceivers that can operate over type 734/728 coaxial cable at the rates of 34.368 Mbps (E3), 44.736 Mbps (DS3), and 51.84 Mbps (STS-1). The transmit side takes an NRZ or already-encoded dual rail input and encodes it into AMI B3ZS (for DS3/STS-1) or HDB3 (for E3) analog waveforms to be transmitted over the coaxial cable. The receiver side takes in the attenuated and distorted analog receive signal and equalizes, slices, and resynchronizes the signal before decoding it to the NRZ output or sending out a non-decoded dual rail.

The architecture of the M28335 includes the following internal functions for each channel:

Transmitter:

- AMI B3ZS/HDB3 encoder
- pulse shaper
- line driver
- Alarm Indication Signal (AIS) insertion
- transmit monitor

Receiver:

- receive sensitivity
- Automatic Gain Control (AGC)
- receive equalizer
- Clock Recovery circuit
- Loss Of Signal (LOS) detector
- B3ZS/HDB3 decoder with bipolar violation detector
- data squelching

Additional Functions:

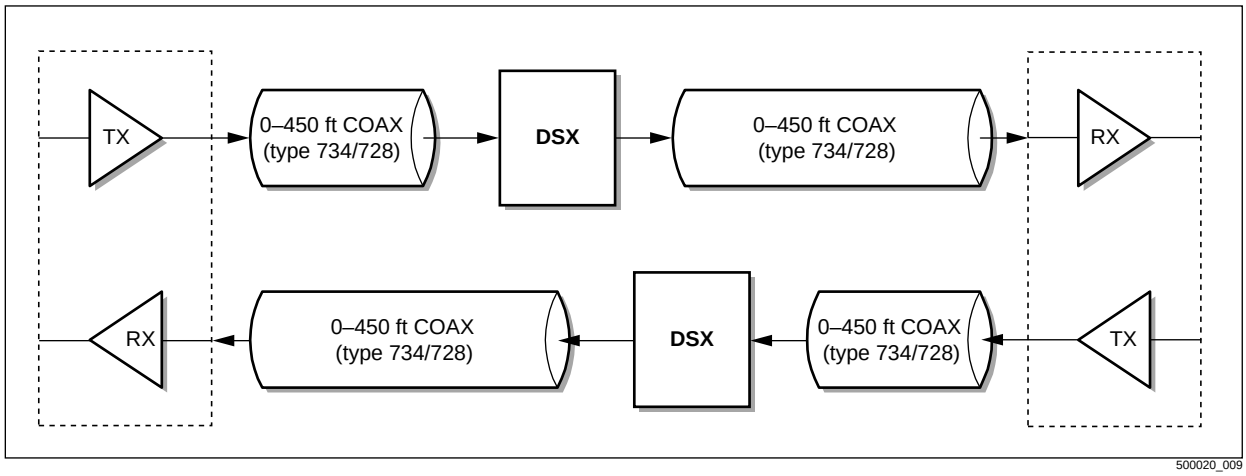
- bias generator
- power-on reset
- loopback MUXes

In addition, each channel has the ability to perform remote and local loopbacks. Figure 2-1 illustrates a typical application using the M28335 in a channel.

Each port can be controlled and configured by the Bus mode through a parallel port or by hardware mode through dedicated pins.

The M28335 is used as a data transceiver over a coaxial cable that is up to 900 feet long (or up to 450 feet from the DSX) in an on-premise environment within any public or private networks that use these data rates.

Figure 2-1. Typical Application of Single M28335 Channel



2.2 Configuration and Control

2.2.1 Hardware Mode

When BMODE pins are tied low or not connected, the device operates in the Hardware mode where the control bus signals are redefined and the configuration of each channel is determined by its associated dedicated PORTMODE pins. The pin redefinition is listed in Table 2-1.

Table 2-1. Pin Redefinition

Pin No.	Hardware Mode (BMODE = 00)	Bus Mode (BMODE = 10)	Serial Mode (BMODE = 11)
U3	PORTMODE1	BDATA0	SDOUT
U4	PORTMODE2	BDATA1	SDIN
U2	PORTMODE3	BDATA2	—
U1	PORTMODE4	BDATA3	—
V1	PORTMODE5	BDATA4	—
V2	PORTMODE6	BDATA5	—
V4	PORTMODE7	BDATA6	—
V3	PORTMODE8	BDATA7	—
T32	PORTMODE9	BADD0	—
T34	PORTMODE10	BADD1	—
U32	PORTMODE11	BADD2	—
U31	PORTMODE12	BADD3	—
V31	TMONTST	BADD4	—
W1	LMODE0	BOE~	SCLK
U34	LMODE1	BWR~	—
U33	GRLOOP	BCS~	BCS~

Pins LMODE0 and LMODE1 are common control lines. Together with the PORTMODEx lines, they control the configuration of the individual ports. The device decodes the three lines and sets the internal registers that determine the configuration of the port according to Table 2-2.

Table 2-2. Port Configuration in Hardware Mode

Pins		Internal Registers				Description
PORTMODEn	LMODE[1:0]	E3MODE	REQH	ENDECDIS	LBO	
0	00	0	0	0	0	DS3/STS-1, square DSX receive pulse (low eq), encode/decode on, LBO = off
0	01	0	1	0	0	DS3/STS-1, normal DSX receive pulse (high eq), encode/decode on, LBO = off
0	10	0	0	0	1	DS3/STS-1, square DSX receive pulse (low eq), encode/decode on, LBO = on
0	11	0	1	1	0	DS3/STS-1, normal DSX receive pulse (high eq) encode/decode off, LBO = off
1	00	1	0	0	0	E3 mode, encode/decode on
1	01	0	1	0	1	DS3/STS-1, normal DSX receive pulse (high eq), encode/decode on, LBO = on
1	10	1	0	1	0	E3 mode, encode/decode off (same as DS3, square, encode/decode off, LBO off)
1	11	0	1	1	1	DS3/STS-1, normal DSX receive pulse (high eq) encode/decode off, LBO = on

The Group Controls Global (GRLOOP) controls the remote loopback. When the GRLOOP pin is tied high, all twelve ports are placed in remote loopback. For normal operations, the GRLOOP should be tied low.

NOTE: The real-time status of the alarm signals RLOS and TLOS are available as dedicated output pins regardless of the BMODE state or bus read/write cycle.

2.2.2 Bus Mode

When the BMODE1 pin is tied high and the BMODE0 is tied low, the device operates in the Bus mode. In Bus mode, the internal registers that control the operation of each port can be accessed through an SRAM like parallel port. The pin redefinition is as follows:

BDATA[7:0]	Eight-bit bidirectional data bus
BADDR[4:0]	Five-bit address bus
BWR~	Write strobe
BOE~	BDATA output enable
BCS~	BDATA chip select

See Chapter 3.0 for definition of the internal registers.

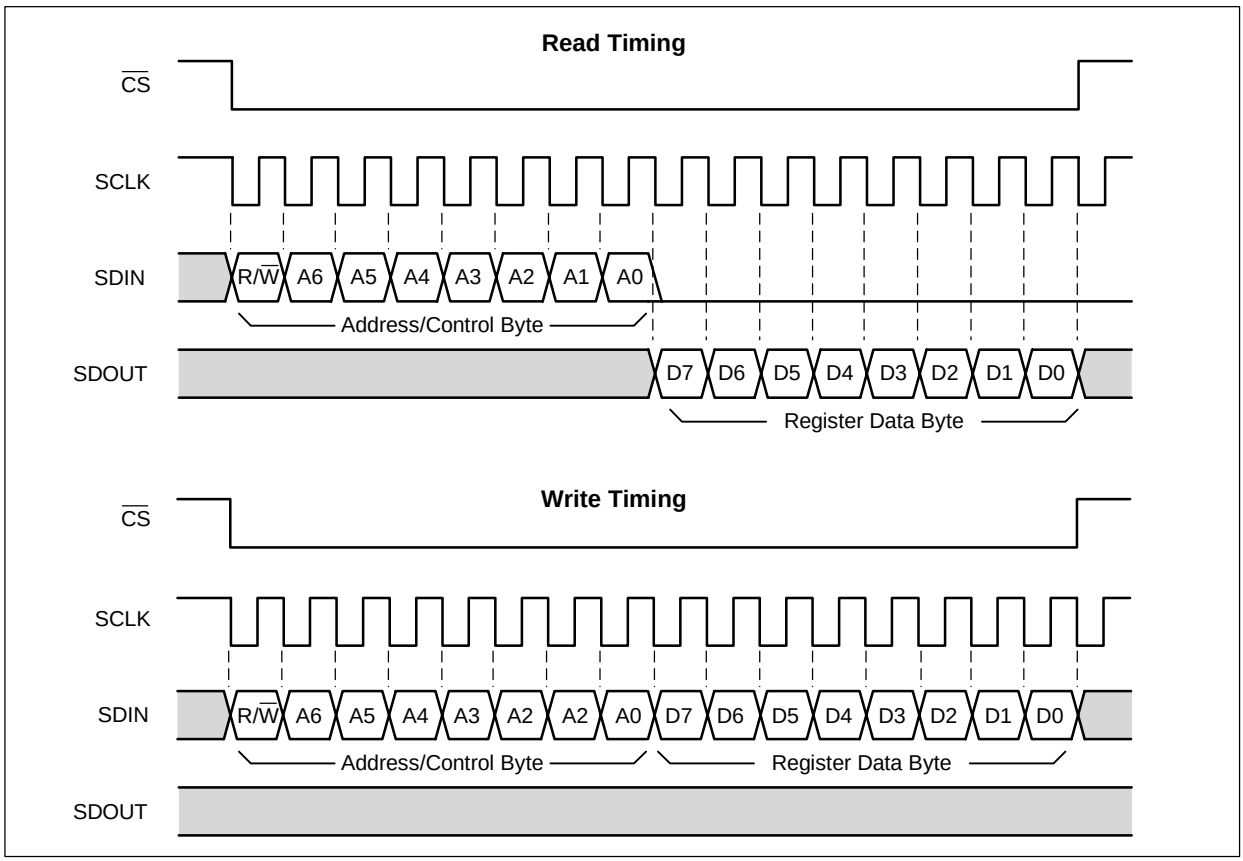
2.2.3 Serial Mode

The M28335 supports a Serial Peripheral Interface (SPI) for device control and configuration. The SPI is a four-wire, slave interface which allows a host processor or framer with a compatible master serial port to communicate with the device. This interface allows the host to control and query the M28335 status by writing and reading internal registers. One 8-bit register in the LIU can be written via the SDIN pin or read from the SDOUT pin at the clock rate determined by SCLK.

The serial port is enabled by pulling the chip select pin, CS, active (low) during the read and write cycles. See Figure 2-2 for the serial peripheral interface port signals. The serial interface uses a 16-bit process for each write or read operation. During a write or read operation, an 8-bit control word consisting of a read/write control bit (R/W) and a 7-bit LIU register address (A[6:0], where A[4:0] are used with A6 and A5 is always set to zero), are transmitted to the LIU at the SDIN pin.

If the operation is a write operation (R/W = 0), an 8-bit register data (D[7:0]) byte follows the address on the SDIN pin. This data is received by the M28335 and stored in the addressed register. If the operation is a read operation (R/W = 1), the M28335 outputs the addressed register contents on the SDOUT pin. The signal input on SDIN is sampled on the SCLK falling edge, and data output on SDOUT changes on the SCLK rising edge.

Figure 2-2. Device Serial Port Signals



2.3 Transmitter

This section describes the detailed operation of the various blocks in the M28335 transmitter.

2.3.1 AMI B3ZS/HDB3 Encoder

ENDECDIS and the E3MODE pins configure the encoder mode.

When ENDECDIS = 0, the encoder is receiving non-encoded Nonreturn to Zero (NRZ) data on the TNRZ (TPOS) pin alone, and the No Connect (NC) (TNEG) pin is ignored.

The data is encoded into a representation of a three-level B3ZS (E3MODE = 0) or HDB3 (E3MODE = 1) signal before going to the pulse shaper in the form of two binary signals representing the positive and negative three-level pulses.

When ENDECDIS = 1, the encoder is disabled. The encoder passes already-encoded data over TPOS (TNRZ) and TNEG (NC) to the pulse shaper.

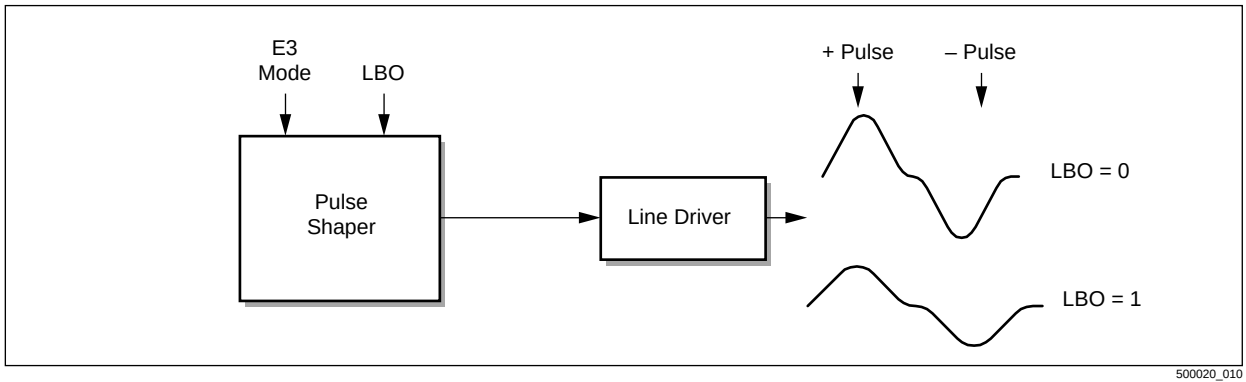
The transmit digital data is clocked into the chip via a rising TCLK edge, which must be equal to the symbol rate (line rate). A small delay added to the data provides a certain amount of negative data hold time.

2.3.2 Pulse Shaper

The pulse shaper converts the two digital (clocked) positive and negative pulses into a single analog three-level Alternate Mark Inversion (AMI) pulse. The pulses are in Return to Zero (RZ) format, meaning that all positive and negative pulses have a duration of the first half of the symbol period.

For the E3 rate (E3MODE = 1), the AMI pulse is a full-amplitude, square-shaped pulse with very little slope.

Figure 2-3. Pulse Shaper



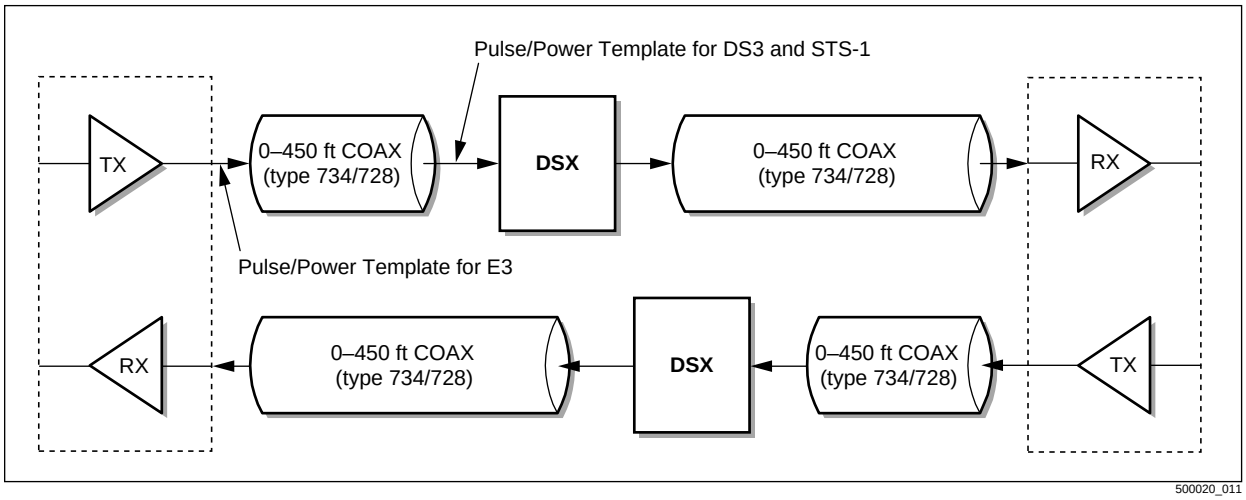
For DS3/STS-1 rates, a pulse-shaper block shapes the transmit waveform and reduces its high-frequency energy content. This ensures that the transmit pulse template is met at the cross-connect block, which follows 0–450 feet of transmit-side coaxial cable.

2.3.3 Line Driver

The differential line driver takes the shaped transmit waveform, increases it to the proper level, and drives it into the transmit magnetics. The two external discrete back-matching resistors (34 Ω) provide line matching. The driver is presented with an approximately 150 Ω differential load. Driver gain accounts for the 6 dB gain loss in the back-matching resistors.

Figure 2-4 illustrates the Pulse/Power template measurement points for the various data rates.

Figure 2-4. Pulse Power Measurement Points



2.3.3.1 Transmit Pulse Mask Templates

Figure 2-5, Figure 2-6, and Figure 2-7 illustrate the transmit pulse masks for DS3, STS-1, and E3 rates respectively.

Figure 2-5. Transmit Pulse Mask for DS3 Rates

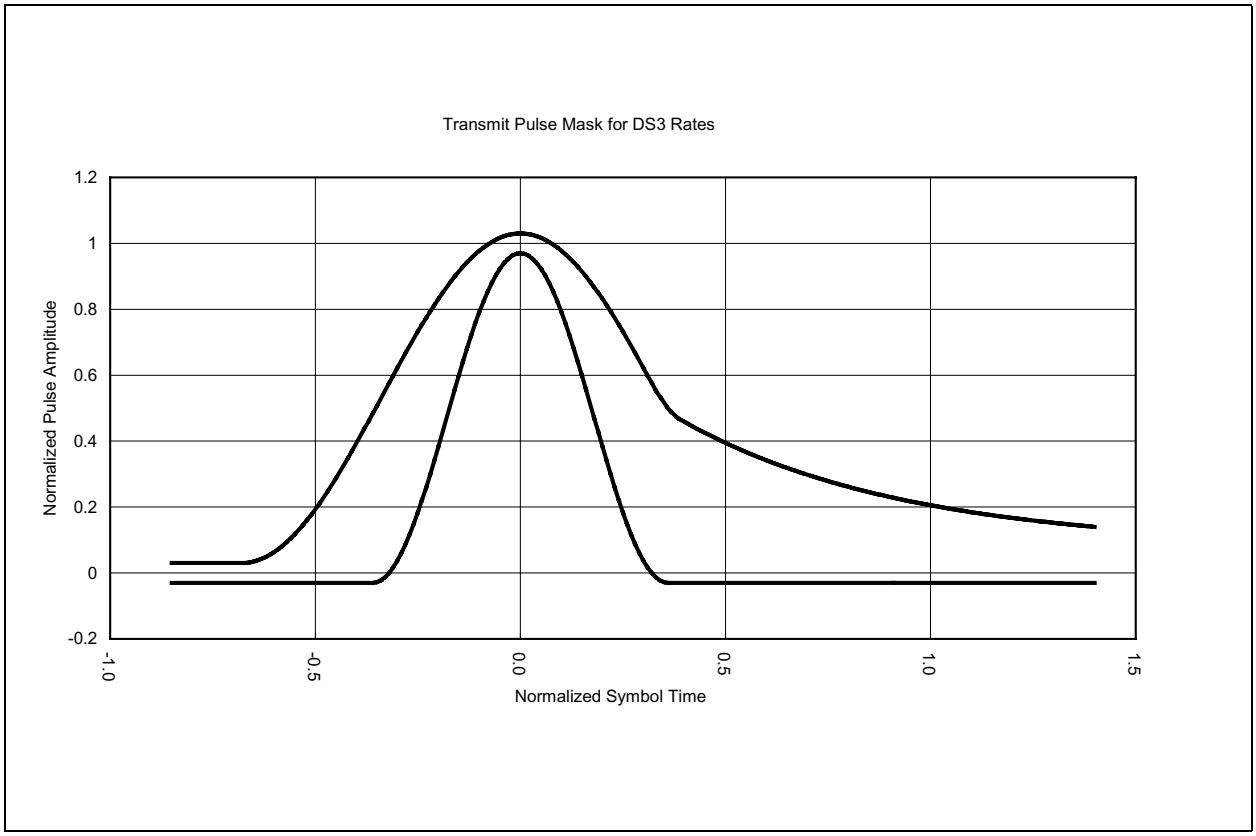


Table 2-3. DS3 Transmit Template Specifications

Time Axis Range (UI)	Normalized Amplitude Equation
Upper Curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.34)]\}$
$0.36 \le T \le 1.4$	$0.08 + 0.407\ e^{-1.84(T - 0.36)}$
Lower Curve	
$-0.85 \le T \le -0.36$	–0.03
$-0.36 \le T \le 0.36$	$-0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.18)]\}$
$0.36 \le T \le 1.4$	–0.03

Figure 2-6. Transmit Pulse Mask for STS-1 Rates

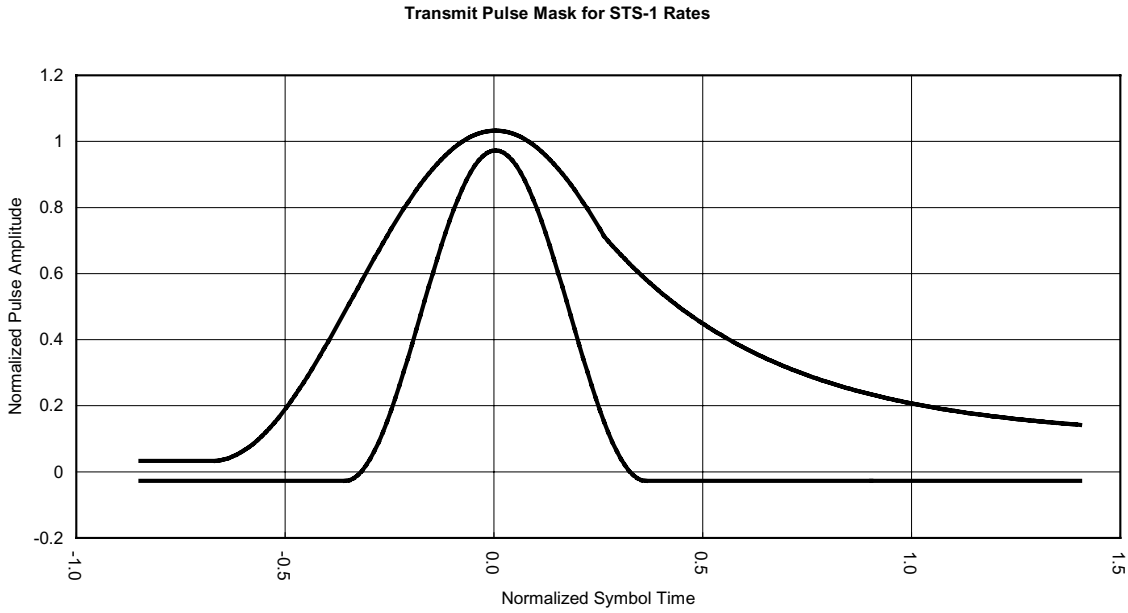
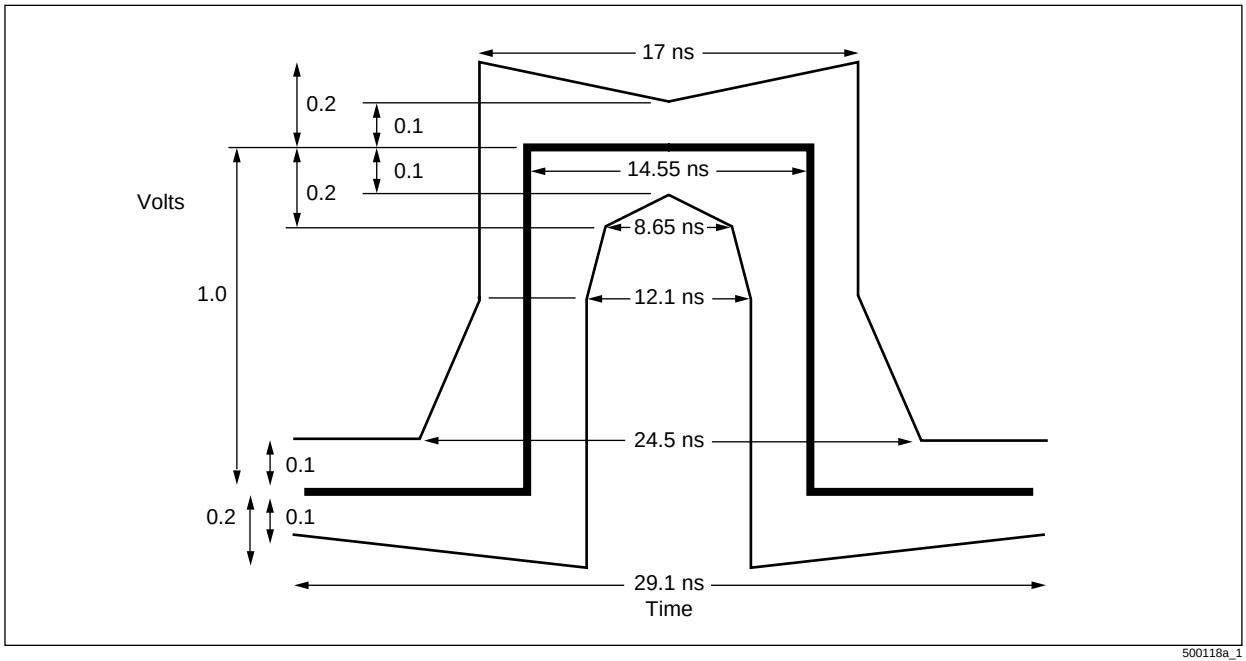


Table 2-4. STS-1 Transmit Template Specifications

Time Axis Range (T)	Normalized Amplitude Equation
Upper Curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.26$	$0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.34)]\}$
$0.26 \le T \le 1.4$	$0.1 + 0.61\ e^{-2.4(T - 0.26)}$
Lower Curve	
$-0.85 \le T \le -0.36$	–0.03
$-0.36 \le T \le 0.36$	$-0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.18)]\}$
$0.36 \le T \le 1.4$	–0.03

Figure 2-7. Transmit Pulse Mask for E3 Rate



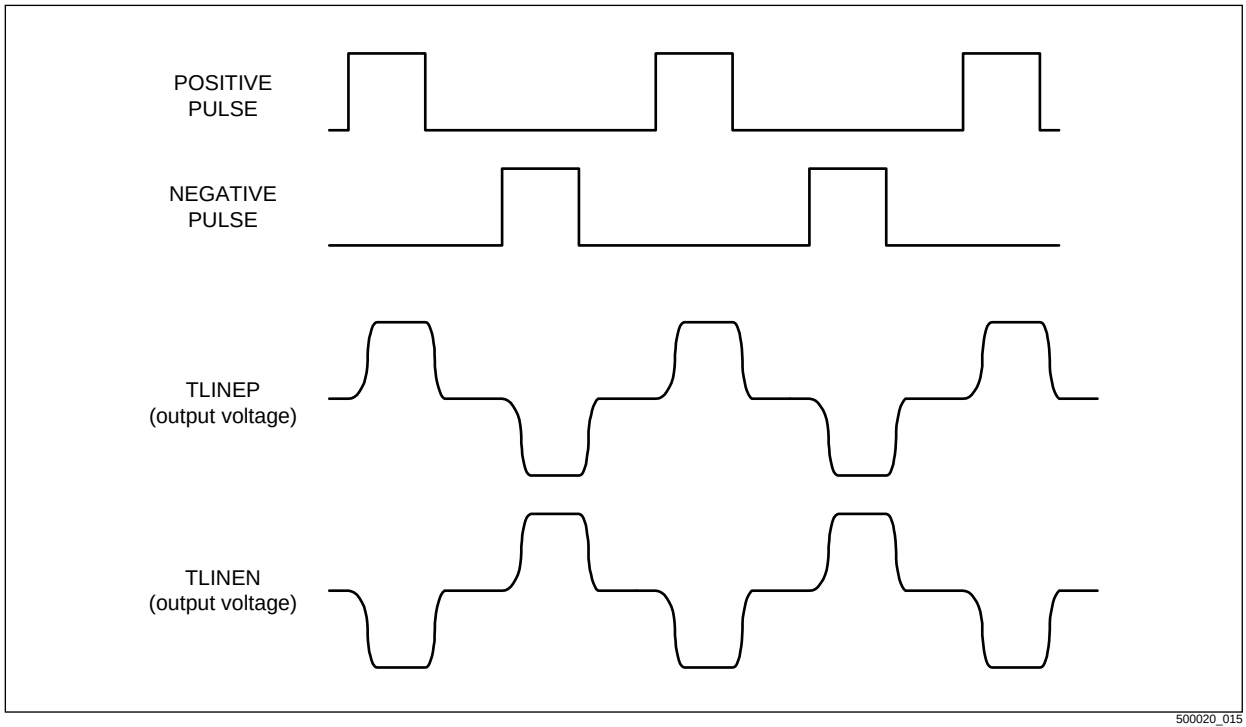
2.3.4 Alarm Indication Signal (AIS) Generator

When TAIS is asserted, an AIS replaces the transmit data at TPOS and TNEG. The E3 type of AIS signal (all 1s) is supported. In three-level signal form, this is a continuously alternating positive and negative pulse stream, as if the transmit data were a continuous string of logical 1s. Figure 2-8 illustrates the AIS signal.

The TAIS pin has the same data latency as the TX data pins and can be used to replace single symbols within a data stream. When the encoder is disabled (ENDECDIS = 1), the TAIS mode maintains the proper phase, based on the polarity of the last 1 received.

The AIS signal follows the same path as the TX data during local loopback, it does not affect remote loopback operation.

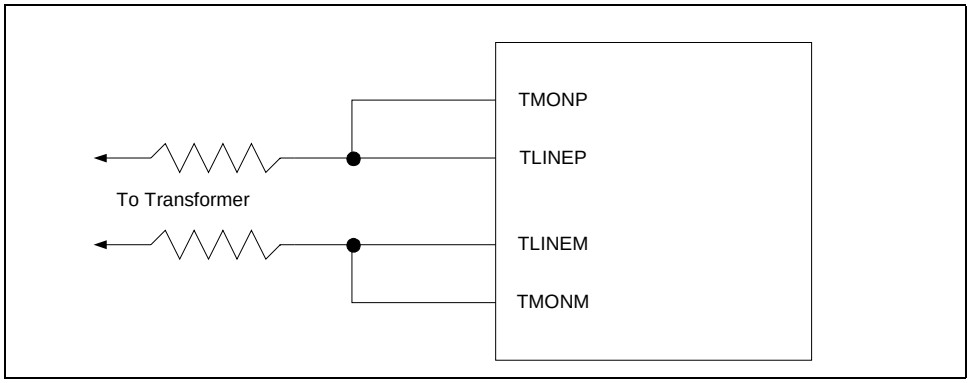
Figure 2-8. AIS Signal



2.3.5 Transmit Monitor Block

The transmit monitor inputs (TMONP and TMONM) are designed to monitor the line driver outputs (TLINEP and TLINEM) for pulses, and to assert a Loss Of Signal (TLOS) indictor when no output pulse has been detected for 32 TCLK periods. After TLOS is asserted, it will not deassert until a pulse is again detected. The transmit monitor is an independent function in which TMONP and TMONM must be externally connected to TLINEP and TLINEM, respectively. The transmit monitor logic does not require external hardware between the transmit signal and the monitor input. This is illustrated in Figure 2-9.

Figure 2-9.Direct Connection of Monitor Signal to Transmit Signal



NOTE: In order for the transmit monitor logic of a port to operate, the transmit clock (TCLK) of that port must be clocked.

A special pin (TMONTST) is available for testing board-level functionality downstream from the TLOS outputs. When TMONTST is high, it asserts all TLOS channel outputs. TLOS outputs are active high when the monitor inputs do not detect a signal.

2.3.6 Jitter Generation (Intrinsic)

The M28335 meets the jitter generation requirements for various rates with large margins, with the condition that the input transmit clock (TCLK) is jitter-free. Data rates and jitter generation requirements are defined in these three documents:

1. E3 rate—*ETSI TBR24, ITU-T G.823 (section 3.1.2)*
2. DS3 rate—*Bellcore Telcordia GR499, AT&T Accunet TR54014, ITU-T G.824*
3. STS-1 rate—*Bellcore Telcordia GR253*

2.4 Receiver

This section describes the detailed operation of the blocks in the M28335 receiver.

2.4.1 Receive Sensitivity

The receiver recovers data from the coaxial cable that is attenuated due to the frequency-dependent characteristics of the cable. In addition, the receiver compensates for the flat loss (across all frequencies) in the various electrical components and the variation in transmitted signal power.

The M28335 can recover data for cable distances shown in Table 2-5 when the cable has characteristics and attenuation consistent with ANSI *T1.102-1993*, Annex C, Figure C.2. This approximates the characteristics of AT&T type 734/728 cable; almost the same attenuation characteristics is achieved by one-half the length of AT&T type 735 cable.

Table 2-5. Receiver Sensitivity (Length of Cable) for DS3/E3/STS-1

Mode	Min	Typ	Max	Units
DS3	900	1275	—	Feet
E3	900	1275	—	Feet
STS-1	900	1200	—	Feet

2.4.2 AGC/VGA Block

The Variable Gain Amplifier (VGA) receives the AMI input signal from the coaxial cable. The VGA supplies flat gain (independent of frequency) to make up for various flat losses in the transmission channel and for loss at one-half the symbol rate that cannot be made up by the equalizer. The VGA gain is controlled by a feedback loop which senses the amplitude of the equalizer output, acts as an amplitude servo for optimal slicing.

2.4.3 Receive Equalizer

The receive equalizer receives the differential signal from a VGA and boosts the high frequency content of the signal to reduce intersymbol interference (ISI) to the point that correct decisions can be made by the slicer with a minimum of jitter in the recovered data.

The REQH pin when set high (REQH = 1) boosts the amount of equalization in the receive side of the LIU. DS3/STS-1 pulses require a greater amount of equalization then standard E3 pulses. REQH is therefore normally set high (REQH = 1) for standard DS3/STS-1 pulses.

For cases where a square-shaped DS3/STS-1 pulse (that does not meet the DS3/STS-1 standards) is transmitted to the receiver REQH can be set low (REQH = 0).

In E3 mode, the REQH pin should always be set low (REQH = 0) to prevent over-equalization.

2.4.4 The PLL Clock Recovery Circuit

The clock recovery circuit (RX PLL) extracts the embedded clock from the sliced data and provides it and the retimed data to the decoder (data mode). Upon startup (after the internal reset is deasserted), the RX PLL uses a reference clock (REFCLK, running at the symbol rate) and a phase-frequency detector to lock to the correct data rate (reference mode). During reference mode, the data outputs are squelched (set to 0). The RX PLL is kept in reference mode until a valid input is detected.

2.4.5 Loss Of Signal (LOS) Detector

The RLOS detector circuitry consists of two functional blocks: the analog section and the digital section. The analog section consists of high-speed, low-offset comparators used for amplitude qualification. The digital section qualifies the pulse stream 1s' density and 0-run length.

In the analog section, two bits control the declare and clear levels for each channel (see Table 2-6).

The digital section asserts RLOS when no valid pulses (per the analog section described above) have been received for 128 REFCLKs. The digital block clears the RLOS when the valid pulse density exceeds 20.3% with <64 consecutive 0s during a 128-symbol period.

The RLOS detector always monitors the cable-side RX inputs. The detector is not affected by the state of remote or local looping.

A bit for each channel, RDx (RLOS Disable), is used to decide if RLOS should disable data squelching. See RLOS Data Squelch Disable registers in Section 3.8.

Table 2-6. RLOS Threshold Control Bits

RMx	RTx	Action	Min Vpk(mV)	Typical Vpk(mV)	Max Vpk(mV)
0	0	RLOS Cleared	—	—	125
		RLOS Declared	18	—	—
0	1	RLOS Cleared	—	92	—
		RLOS Declared	—	58	—
1	0	RLOS Cleared	—	15	—
		RLOS Declared	—	15	—
1	1	Reserved	—	—	—
GENERAL NOTE: RMx RTx = 10: No Hysteresis					

2.4.6 B3ZS/HDB3 Decoder With Bipolar Violation Detector

In the M28335 device, when ENDECDIS = 0 (encoder/decoder enabled), the decoder takes the output from the clock recovery circuit and decodes the data (HDB3 or B3ZS) into a single retimed NRZ data signal. The data signal is then sent out of the M28335 RNRZ (RPOS) pin. Any detected Line Code Violations (LCV) are sent over

the corresponding RLCV (RNEG) pin. The RLCV pin is asserted for one symbol period at the time the violation appears on the RX output pin (RNRZ).

The following shows data sequence criteria for LCV; violations are indicated in bold text. A valid bipolar pulse is indicated by a B. A bipolar violation (non-alternating positive or negative) pulse is indicated by a V.

- Excessive zeros: 0, 0, 0, **0** (HDB3) or 0, 0, **0** (B3ZS). These violations are passed on as 0 data on the RNRZ pin.
- Bipolar violation: B, 0, **V** (i.e., +1, 0, **+1** or –1, 0, **–1** for HDB3) B, **V** (B3ZS and HDB3). These violations are passed on as 1 data on the RNRZ pin.
- Coding violation: 0, 0, **V** (HDB3) or 0, **V** (B3ZS) with an even number of Bs since the last valid 0 substitution V (follows coding rule). These violations are passed on as 0 data on the RNRZ pin.

The even/odd counter (used to count the number of Bs between Vs) will count a bipolar violation as a B. A coding violation or a valid 0 substitution resets the counter.

When ENDECDIS = 1, the decoder is disabled, and the retimed slicer outputs are sent out over RPOS (RNRZ) and RNEG (RLCV) pins. These outputs are then decoded by the Framer or other downstream device. LCVs are not detected in this mode of operation. The decoder is configurable for either:

- E3 mode using HDB3 coding (E3MODE = 1), or
- DS3/STS-1 mode using B3ZS coding (E3MODE = 0).

The receiver digital data outputs are centered on the rising edge of RCLK (see Section 2.8.8).

2.4.7 Data Squelching

A counter in the receiver counts the number of consecutive symbol periods without a valid data pulse. When 128 or more 0s in a row are counted, the receiver assumes it has lost the signal and resets itself to try to regain the signal. While the receiver is reacquiring the signal, the clock recovery block locks to the reference clock, and data squelching is achieved by forcing the data bits to 0. The data squelching is true in both NRZ and dual rail mode. When the input signal has been properly amplified and equalized, the clock recovery PLL then switches to the incoming data.

2.5 Jitter Tolerance

The M28335 receiver can tolerate a specified amount of high-frequency jitter in the received signal while providing error-free operation (generally defined as a BER of $< 10^{-9}$). The specifications (illustrated in Figure 2-10) for jitter tolerance are discussed in the following documents:

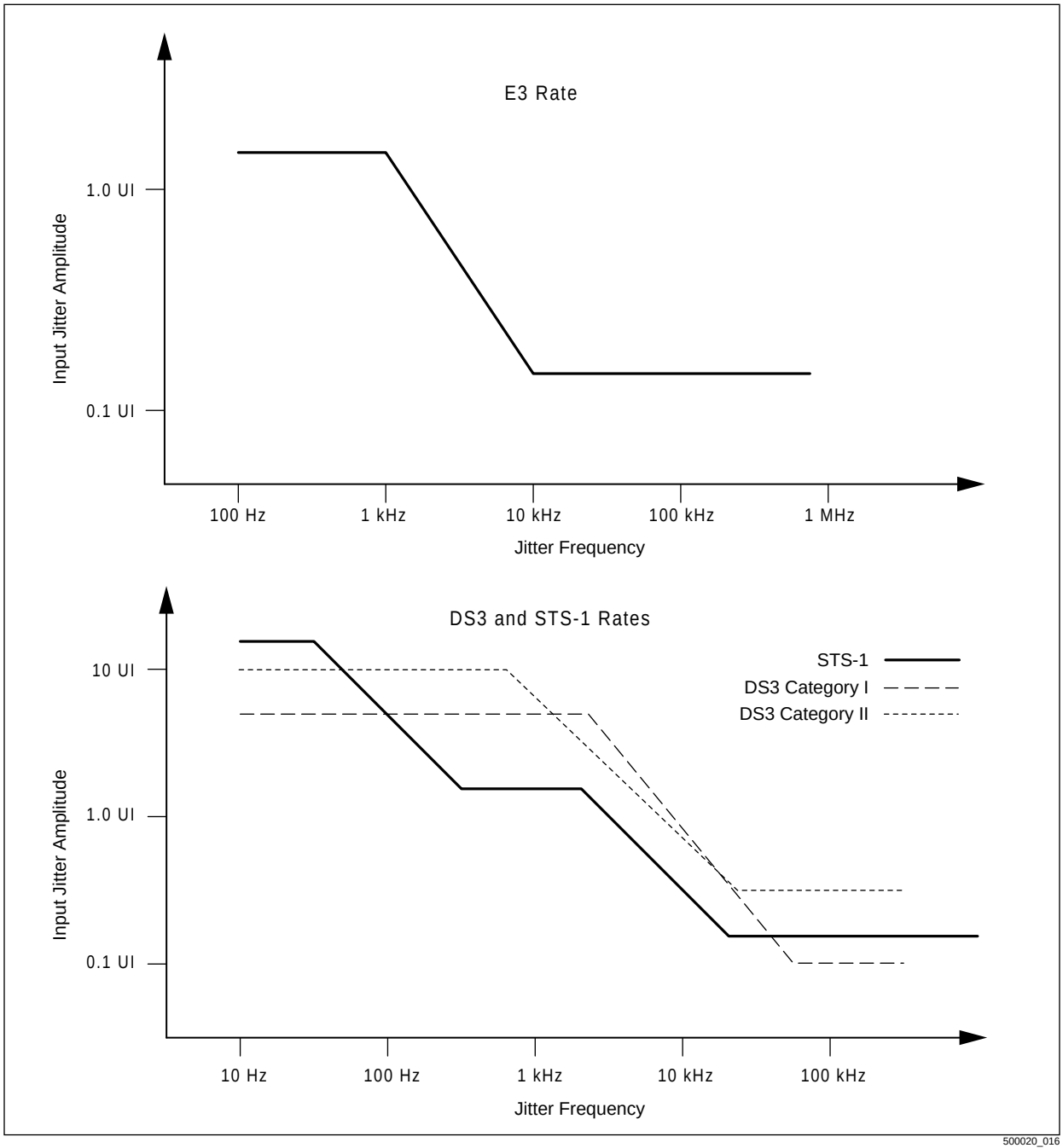
- E3 rate—*ITU-T G.823* and *ETSI TBR24* contain frequency masks for input jitter tolerance.

NOTE: To meet jitter transfer requirements for loop-timed operation, an external jitter attenuator is required. The jitter attenuator lessens jitter from the receive clock.

- DS3 rate—*Bellcore GR499* specifies jitter tolerance frequency masks for Category I and Category II interfaces.
- STS-1 rate—*Bellcore GR253* specifies a jitter tolerance.

NOTE: The STS-1 jitter tolerance differs from DS3 requirements only for Category II interfaces.

Figure 2-10. Minimum Jitter Tolerance Requirement



2.5.1 Jitter Transfer

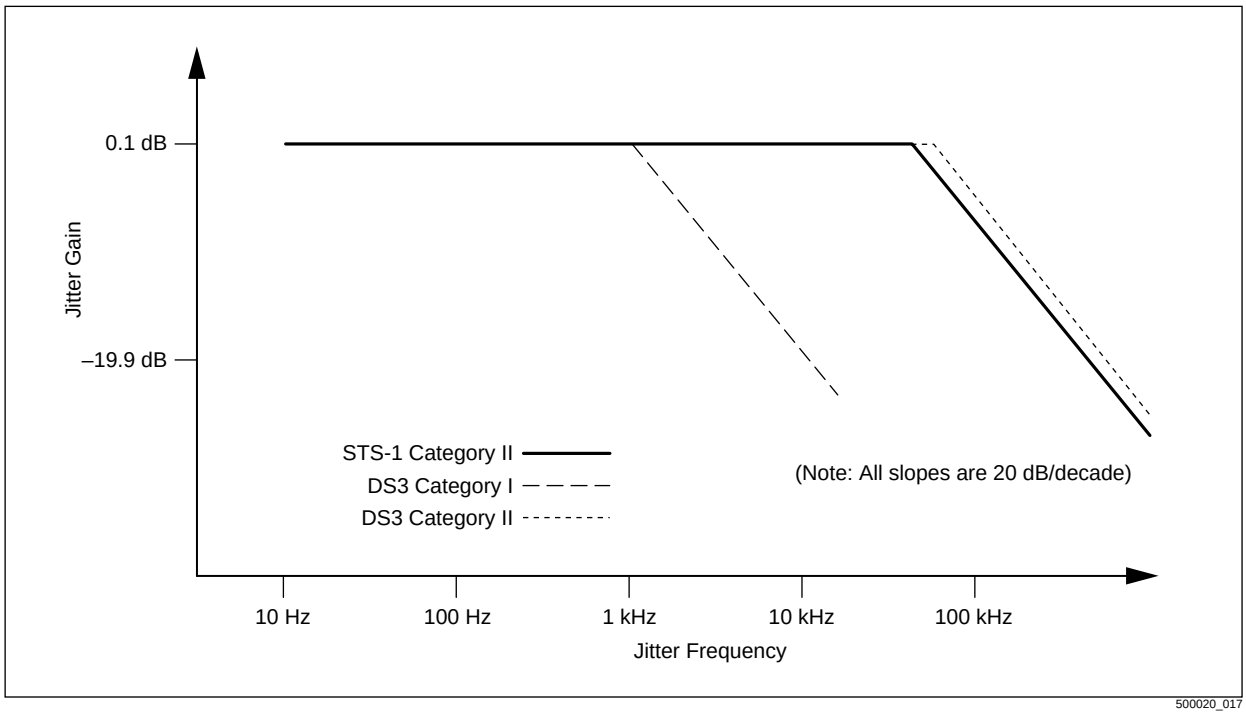
The receiver must meet certain jitter transfer specifications between the input and output jitter as a function of frequency. These specifications are only intended to be met with the use of a jitter attenuator. Because the M28335 does not contain a jitter attenuator, one must be supplied externally. For reference purposes, the specifications are discussed in the following documents and illustrated in Figure 2-11.

E3 rate—Assume the same as DS3.

DS3 rate—Bellcore *GR499*, section 7.3.2 and figures 7-3, 7-4, and 7-5, defines and describes DS3 jitter transfer.

STS-1 rate—Bellcore *GR253*, section 5.6.2.1, defines and describes jitter transfer for the STS-1 rate.

Figure 2-11. Maximum Jitter Transfer Curve Requirement



2.6 Additional M28335 Functions

2.6.1 Bias Generator

The four RBIAS resistors are used to convert internal current references into accurate voltage references used for internal voltage biasing. The RBIAS resistors ensure that internal voltage references are kept within tight tolerance.

The 12.1 kΩ external resistors from the RBIAS pins to ground are specified to have a tolerance of ±1%. This ensures tight control of the internal voltage references.

NOTE: Refer to Section 4.5.2 for RBIAS resistor placement.

2.6.2 External Reset

In hardware mode, if the system cannot guarantee a valid REFCLK frequency input during the power-on reset (POR) cycle, the M28335 requires assertion of the external reset signal (RESET) after power-up. Valid frequencies of REFCLK are DS3 (44.736 MHz ± 20 ppm), E3 (34.368 MHz ± 20 ppm) and STS-1 (51.84 MHz ± 20 ppm).

In bus or serial mode, an external reset should always be performed after power-up.

2.6.3 Power-On Reset (POR)

A POR circuit is provided in the device to initialize all resettable digital logic and analog control lines used in hardware mode operation (Registers, interrupt, and status used in bus/serial mode operation require an external reset after power-up). The POR circuit uses a fixed RC timer (~1µs) to deassert itself as soon as the power supply voltage reaches a minimum level (~2 V). When the minimum supply voltage is reached (see Table 2-9), the REFCLK input is counted for 128 clocks before the internal reset is deasserted. At this time the receiver block attempts to frequency lock onto a valid incoming REFCLK input. After frequency lock is achieved, the receiver attempts to phase lock onto the valid RLINE receive signal.

NOTE: If a valid REFCLK input is not present when POR releases the internal reset, the receiver block may be unable to lock to the RLINE receive signal. It is common for some types of crystal oscillators to oscillate at a lower fundamental frequency if the crystal oscillator supply has not reached its minimum operational voltage.

NOTE: An external reset should always be performed after power-up when using the device in bus or serial mode.

2.6.4 Interrupt

Each RLOS and TLOS signal goes to its dedicated edge-detector, whose output is stored in a flip-flop

Each interrupt has a dedicated enable register bit with which specific interrupt sources can be activated.

All the interrupt register outputs are ORed together and generate a global interrupt value, which can be read in the Global register

The Global Interrupt signal also has its enable register bit in the Global register, which activates the routing of the global interrupt to the interrupt pin.

The Interrupt Status register contents can be read through the parallel or serial interface. A read of an interrupt register should clear the register, but should leave the others untouched.

2.6.5 Loopback Multiplexers (MUXes)

Two loopback MUXes per channel in the M28335 allow for local loopback (terminal or framer side), remote loopback (cable side), or both. The RLOS signal monitors the RX cable inputs irrespective of any loopback.

Remote Loopback (RLOOP) is controlled by bit 4 in the Portn Control register. In RLOOP, the receive data (retimed after clock recovery but not decoded) loops back into the pulse shaper in place of the transmit data. Additionally, this data is sent out to the RPOS, RNEG, and RCLK pins.

Local Loopback (LLOOP) is controlled by bit 3 in the Portn Control register. In LLOOP, the transmit data loops back immediately from the encoder output to the decoder input in place of the received data. Additionally, this data is sent out to the TLINEP and TLINEM/N pins.

NOTE: During transmit AIS operation, data in local loopback will be overwritten with an all 1's pattern. AIS operation does not affect remote loopback.

Figure 2-12. Remote Loopback Diagram

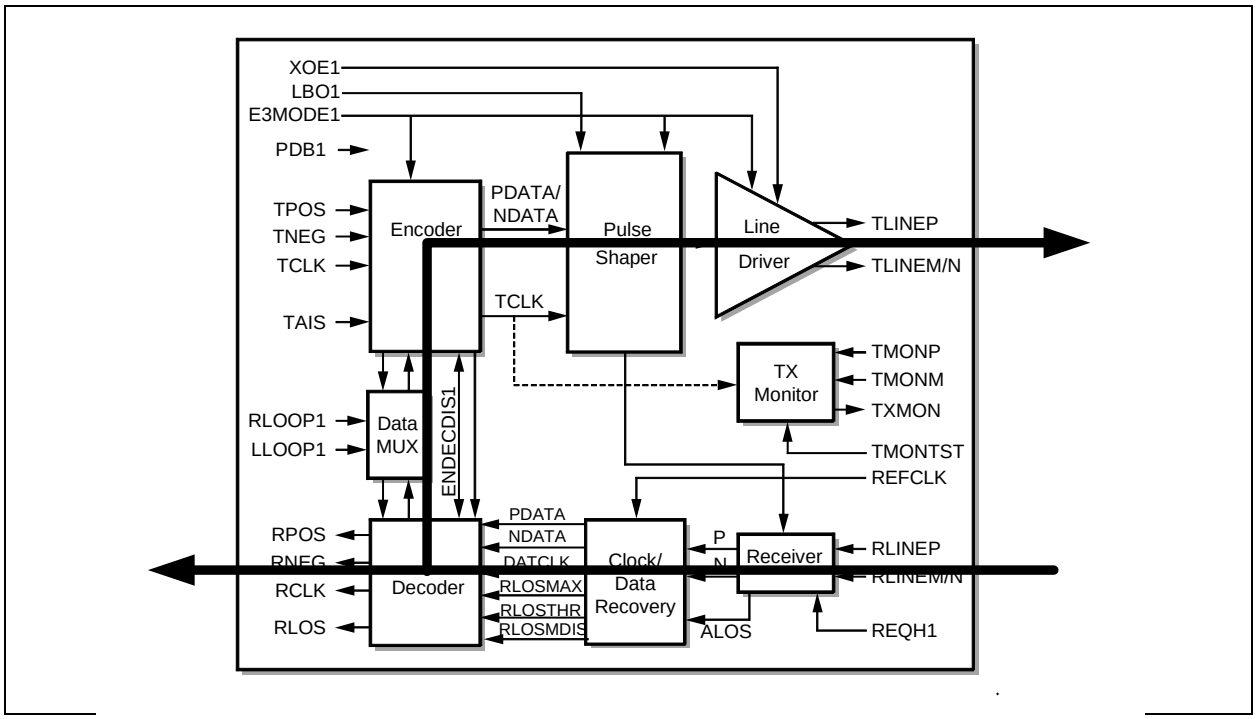
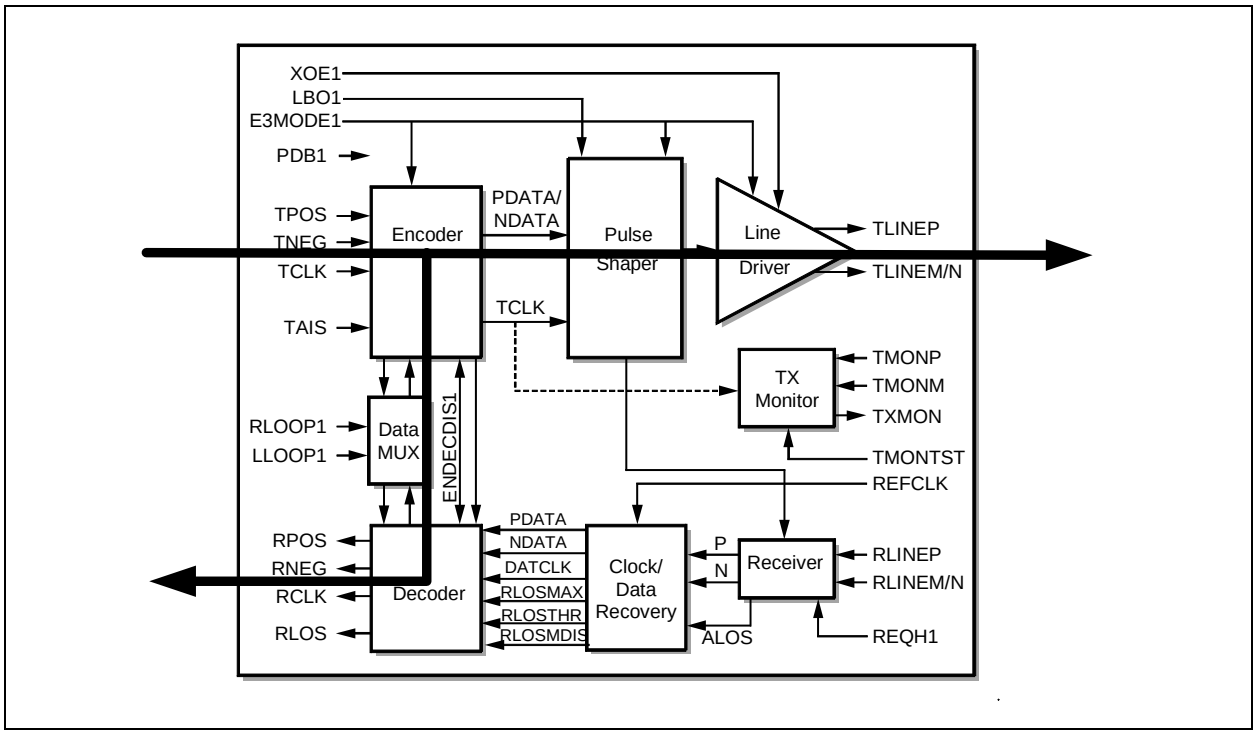
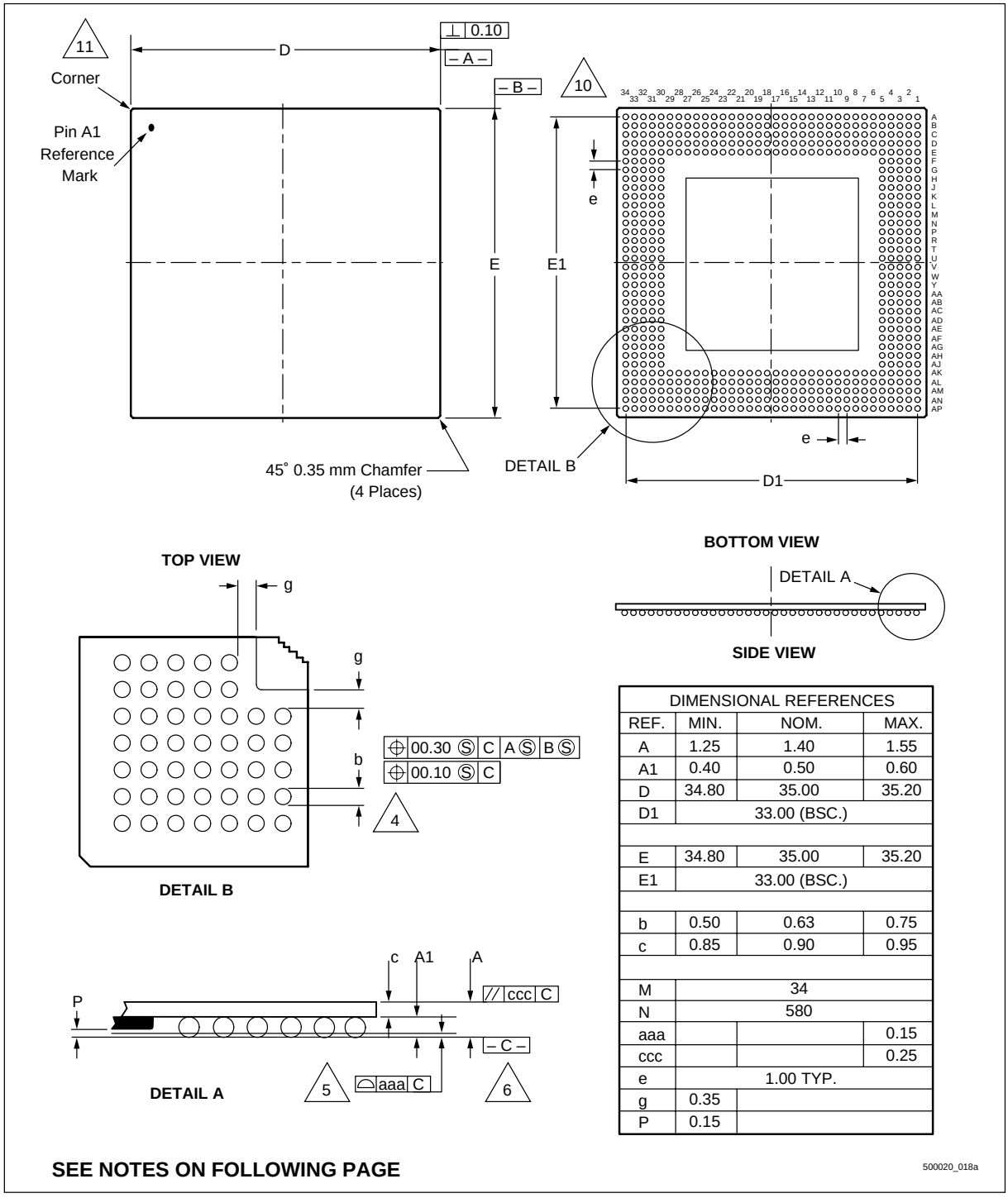


Figure 2-13. Local Loopback Diagram



2.7 Mechanical Specifications

Figure 2-14. M28335 Mechanical Drawing (35 mm TBGA)—Dimensions



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.25	1.40	1.55
A1	0.40	0.50	0.60
D	34.80	35.00	35.20
D1		33.00 (BSC.)	
E	34.80	35.00	35.20
E1		33.00 (BSC.)	
b	0.50	0.63	0.75
c	0.85	0.90	0.95
M		34	
N		580	
aaa			0.15
ccc			0.25
e		1.00 TYP.	
g	0.35		
P	0.15		

SEE NOTES ON FOLLOWING PAGE

500020_018a

Notes to Figure 2-14 on previous page:

1. All dimensions are in millimeters.

2. “e” represents the basic solder ball grid pitch.

3. “M” represents the basic solder ball matrix size, and symbol “N” is the maximum number of balls after depopulating.

4. “b” is measured at the maximum solder ball diameter after reflow parallel to primary datum –C–

5. Dimension “aaa” is measured parallel to primary datum –C–

6. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.

7. Package surface shall be black oxide.

8. Cavity depth C1 varies with die thickness.

9. Substrate material base is copper.

10. Bilateral tolerance zone is applied to each side of package body.

11. 45 degree 0.35 mm chamfer corner for Pin 1 identification.

12. Encapsulant size may vary with die size.

13. Refer to ASME Y14.5M-1994 FOC for the standard on dimensioning and tolerance.

2.7.1 Moisture Sensitivity

The device meets moisture sensitivity level (MSL) 4.

2.8 Electrical/Thermal Characteristics

2.8.1 Absolute Maximum Ratings

Table 2-7. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
DVDD/ RVDD/ TVDD/ VGG	Power supply voltage	–0.3	5.5	V
V_I	Voltage on any signal pin	–1.0	VGG + 0.3 V	V
T_{ST}	Storage temperature	–40	125	°C
T_{VSOL}	Vapor phase soldering temperature (1 min.)	—	220	°C
T_{AC}	Ambient operating temperature	–40	85	°C
θ_{JA}	Thermal resistance (Junction-Ambient)	—	10	°C/W
θ_{JC}	Thermal resistance (Junction-Case)	—	1	°C/W
T_c	Maximum Case Temperature	—	121	°C
T_j	Junction temperature	—	125	°C

GENERAL NOTE:

1. Stresses above those listed as absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.8.2 ESD Ratings

Testing Method—The devices were subjected to ESD events at the rated voltage with both positive and negative polarities relative to each other pin or supply domain on the device. The given pin was then curve-traced to detect leaky or shorted ESD diodes. The criterion for passing is three devices that withstand voltage without any leaky pins or functional failures.

Table 2-8. ESD Ratings

Model	Observed Minimum
Human Body	2,500 V
Charged Device	500 V

2.8.3 Recommended Operating Conditions

Table 2-9 lists various operating conditions, power supplies, and the bias resistor.

Table 2-9. Recommended Operating Conditions

Parameter	Conditions	Min	Nom	Max	Unit
Power supply voltage	DVDD, RVDD, TVDD	3.135	3.3	3.465	V
ESD voltage[1, 2]	VGG	3.135	5	5.5	V
External bias resistor	Pin RBIAS to GND; ±1%	11.98	12.1	12.22	KΩ

FOOTNOTE:

(1) With 5 V logic input, VGG should be tied to 5 V. With 3.3 V logic input, VGG should be tied to 3.3 V. VGG must be equal to or greater than the power supply voltage (DVDD, RVDD, TVDD).

(2) VGG must be sequenced with respect to VDD (DVDD, RVDD, TVDD) as discussed in Appendix B.

2.8.4 DC Characteristics

Table 2-10. DC Characteristics

Parameter	Conditions	Min	Nom	Max	Unit
V_{ih} high threshold	Digital inputs	2.0	—	VGG + 0.3	V
V_{il} low threshold	Digital inputs	–0.3	—	0.8	V
V_{oh} high threshold	Digital outputs, I_{oh} = –4 mA	2.4	—	—	V
V_{ol} low threshold	Digital outputs, I_{ol} = 4 mA	—	—	0.4	V
I_{LEAK} (digital inputs and outputs)	0 V ≤ digital V_{in} ≤ VGG	–10	—	200	µA
I_{LEAK} (RLINExP, RLINExM, TLINExP, TLINExM)		–270	—	270	µA
I_{LEAK} (TMONxP, TMONxM)		–50	—	400	µA
Input capacitance	Digital inputs	—	—	10	pF
Load capacitance	Digital outputs	—	—	15	pF
Power dissipation (total chip)	STS1	—	3.72	4.00	W
	DS3	—	3.52	3.86	W
	E3	—	3.15	3.65	W

GENERAL NOTE:

1. The digital inputs are TTL 5 V-compliant when VGG=5V. These inputs are diode protected to the VGG pin. Additionally, all digital inputs contain 75 kΩ pull-down resistors.
2. The digital outputs are also TTL 5 V-compliant when VGG=5V. However, these outputs will not drive to 5 V, nor will they accept 5 V external pull-ups.
3. Power dissipation for an all 1s pattern with all ports active.

2.8.5 DS3 Electrical Characteristics

Table 2-11. DS3 Receiver Characteristics

Parameter	Min	Typ	Max	Unit
Receiver Sensitivity	900	1275		Feet
Intrinsic Jitter (all “1’s” pattern) Remote Loopback		0.005		UI
Jitter Tolerance @ Jitter Frequency = 100 Hz		>64*		UI
Jitter Tolerance @ Jitter Frequency = 1 KHz		>64*		UI
Jitter Tolerance @ Jitter Frequency = 10 KHz		19		UI
Jitter Tolerance @ Jitter Frequency = 300 KHz (Cat II)		1		UI
* Limited by test equipment capabilities.				

2.8.6 E3 Electrical Characteristics

Table 2-12. E3 Receiver Characteristics

Parameter	Min	Typ	Max	Unit
Receiver Sensitivity (length of cable)	900	1275		Feet
Interference Margin	-20			dB
Intrinsic Jitter (all “1’s” pattern) Remote Loopback		0.010		UI
Jitter Tolerance @ Jitter Frequency = 100 Hz		>64*		UI
Jitter Tolerance @ Jitter Frequency = 1 KHz		>64*		UI
Jitter Tolerance @ Jitter Frequency = 10 KHz		18		UI
Jitter Tolerance @ Jitter Frequency = 800 KHz		0.7		UI
* Limited by test equipment capabilities.				

2.8.7 STS-1 Electrical Characteristics

Table 2-13. STS-1 Receiver Characteristics

Parameter	Min	Typ	Max	Unit
Receiver Sensitivity	900	1200		Feet
Intrinsic Jitter (all “1’s” pattern) Remote Loopback		0.005		UI
Jitter Tolerance @ Jitter Frequency = 100 Hz		>64*		UI
Jitter Tolerance @ Jitter Frequency = 1 KHz		>64*		UI
Jitter Tolerance @ Jitter Frequency = 10 KHz		19		UI
Jitter Tolerance @ Jitter Frequency = 400 KHz		0.8		UI
* Limited by test equipment capabilities.				

2.8.8 AC Characteristics

Table 2-14. AC Characteristics (Logic Timing)

Parameter	Conditions	Min	Nom	Max	Unit
Tosym, Tisym RCLK and TCLK	E3 DS-3 STS-1	—	29.10 22.35 19.29	—	ns ns ns
Clock Duty Cycle	Towidth/Tosym, RCLK Tiwidth/Tisym, TCLK Tiwidth/Tisym, REFCLK	45 30 40	—	55 70 60	% % %
Todelay	—	—	—	3.5	ns
Tisetup	TPOS/TNRZ, TNEG, TAIS	4	—	—	ns
Tihold	TPOS/TNRZ, TNEG, TAIS	0	—	—	ns
Trise	—	—	2.22	3.50	ns
Tfall	—	—	1.28	2.50	ns

GENERAL NOTE:

1. The description applies to the DS3, E3, and STS-1 clock rates and other parameters such as pulse width, set-up time, hold time, and duty cycle.
2. The timing diagram, illustrated in Figure 2-15, describes the logical relationship between various clock and data signals, and parameter values.

Figure 2-15. Timing Diagram

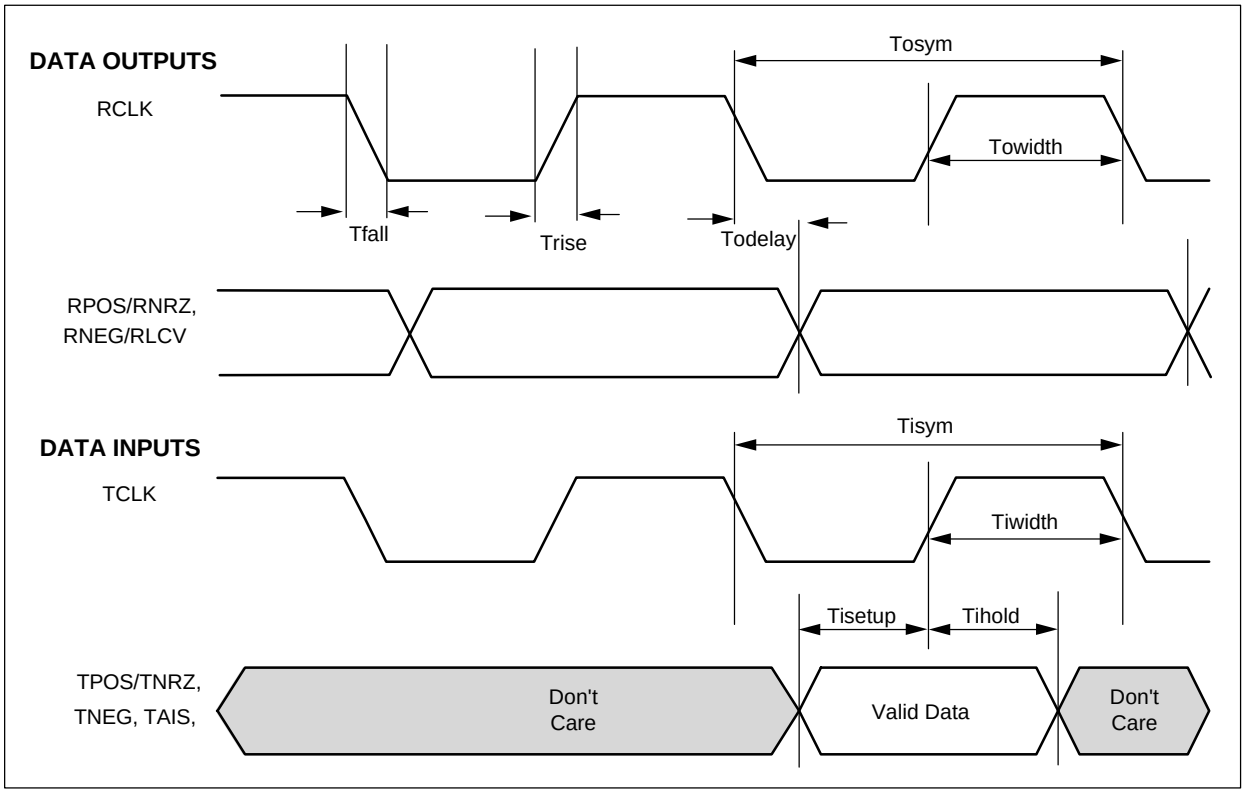


Table 2-15. Bus Mode Timing—Read Cycles

Parameter	Description	Min	Typ	Max
T_{AZD}	Address valid to data valid	—	—	12 ns
t_h	Address hold after BCS~ & BOE~ rising edge	5 ns	—	—
t_{en}	BCS~ & BOE~ falling edge to BDATA drive	1 ns	—	8 ns
t_{dis}	BDATA hold after BCS~ & BOE~ rising edge	1 ns	—	8 ns
t_{pwh}	BCS~ & BOE~ high time	20 ns	—	—
t_{pwl}	BCS~ & BOE~ low time	20 ns	—	—

Figure 2-16. Bus Mode Read Timing

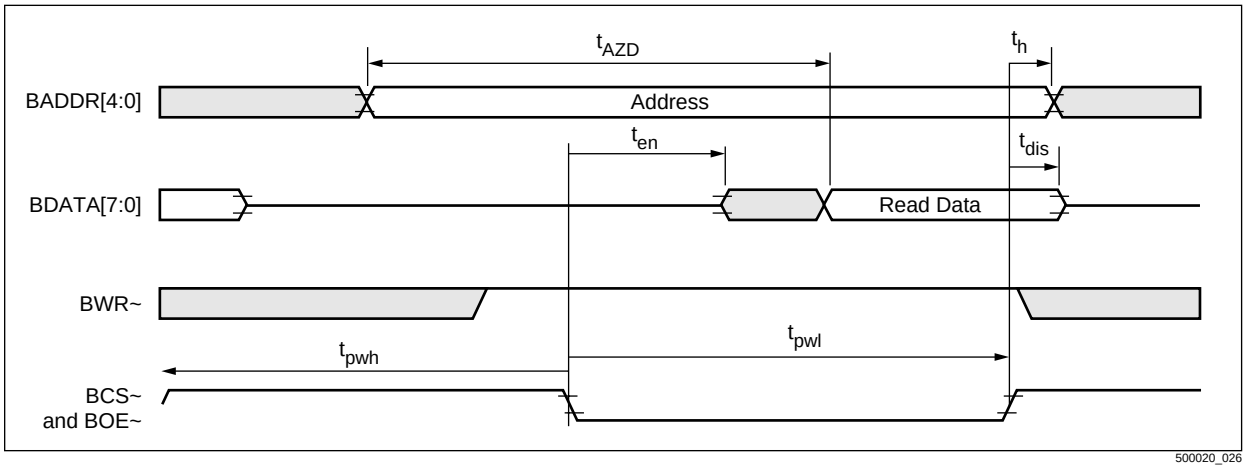


Table 2-16. Bus Mode Timing—Write Cycles

Parameter	Description	Min	Type	Max
t_{s1}	Address setup before BCS~ & BWR~ rising edge	12 ns	—	—
t_{h2}	Address hold after BCS~ & BWR~ rising edge	5 ns	—	—
t_{s2}	Data setup before BCS~ & BWR~ rising edge	12 ns	—	—
t_{h1}	Data hold after BCS~ & BWR~ rising edge	5 ns	—	—
t_{pwh}	BCS~ & BWR~ high time	20 ns	—	—
t_{pwl}	BCS~ &BWR~ low time	20 ns	—	—

Figure 2-17. Bus Mode Write Timing

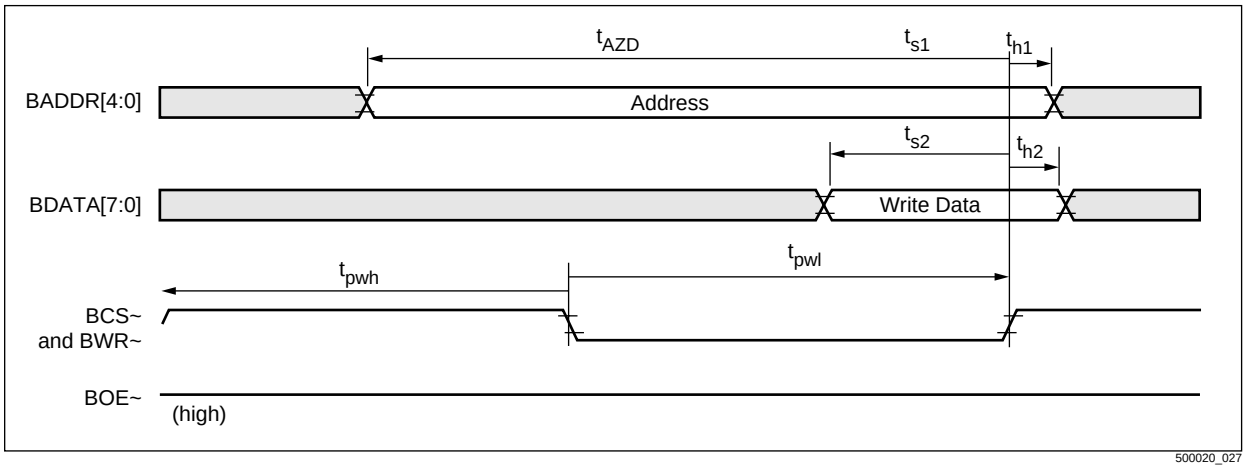


Table 2-17. Serial Mode Timing

Symbol	Parameter	Min	Max	Unit
Tcssu	BCS~ set-up time to SCLK rising edge	10	—	ns
PWsch	Pulse width SCLK high	80	—	ns
PWscl	Pulse width SCLK low	80	—	ns
Tsisu	SDI to SCLK rising edge set-up time	10	—	ns
Tsihf	SCLK rising edge to SDI hold time	5	—	ns
Tvsif	SCLK falling edge to SDO valid time	—	50	ns
Tsiz	BCS~ inactive to SDO three-state	—	100	ns
PWcsi	Pulse width BCS~ inactive	100	—	ns
Tcsur	SCLK rising edge to BCS~ hold time	5	—	ns

Figure 2-18. Serial Mode Register Read (see Note below)

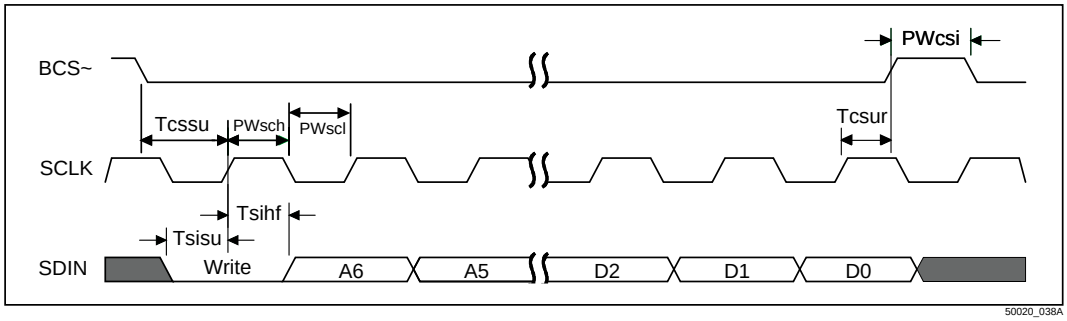
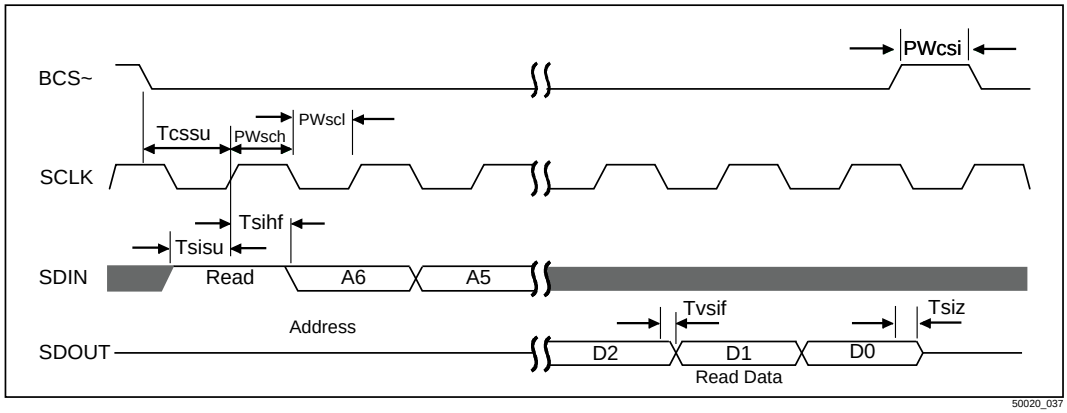


Figure 2-19. Serial Mode Register Write (see Note below)



NOTE: In Serial mode,

- BDATA1/PORTMODE2/SDIN pin is configured as SDIN
- BDATA0/PORTMODE1/SDOUT pin is configured as SDOUT
- BOE~/LMODE0/SCLK pin is configured as SCLK

3.0 Registers

3.1 Address Map

Table 3-1. Register Address Map(1 of 2)

Address	Name	Description	R/W	Default
0x00	GC	Global Control Register	R/W	0x00
0x01	PC1	Port1 Control Register	R/W	0x04
0x02	PC2	Port2 Control Register	R/W	0x04
0x03	PC3	Port3 Control Register	R/W	0x04
0x04	PC4	Port4 Control Register	R/W	0x04
0x05	PC5	Port5 Control Register	R/W	0x04
0x06	PC6	Port6 Control Register	R/W	0x04
0x07	PC7	Port7 Control Register	R/W	0x04
0x08	PC8	Port8 Control Register	R/W	0x04
00x9	PC9	Port9 Control Register	R/W	0x04
0x0A	PC10	Port10 Control Register	R/W	0x04
0x0B	PC11	Port11 Control Register	R/W	0x04
0x0C	PC12	Port12 Control Register	R/W	0x04
0x0D	RMTR1	RLOS Max/Threshold Register 1	R/W	0x00
0x0E	RMTR2	RLOS Max/Threshold Register 2	R/W	0x00
0x0F	RMTR3	RLOS Max/Threshold Register 3	R/W	0x00
0x10	RALM1	RLOS Alarm Register 1	R	—
0x11	RALM2	RLOS Alarm Register 2	R	—
0x12	TALM1	TLOS Alarm Register 1	R	—
0x13	TALM2	TLOS Alarm Register 2	R	—
0x14	RISR1	RLOS Interrupt Status Register 1	R/C	—
0x15	RISR2	RLOS Interrupt Status Register 2	R/C	—
0x16	TISR1	TLOS Interrupt Status Register 1	R/C	—
0x17	TISR2	TLOS Interrupt Status Register 2	R/C	—
0x18	RIER1	RLOS Interrupt Enable Register 1	R/W	0x00
0x19	RIER2	RLOS Interrupt Enable Register 2	R/W	0x00

Table 3-1. Register Address Map(2 of 2)

Address	Name	Description	R/W	Default
0x1A	TIER1	TLOS Interrupt Enable Register 1	R/W	0x00
0x1B	TIER2	TLOS Interrupt Enable Register 2	R/W	0x00
0x1C	RDR1	RLOS Data Squelch Disable Register 1	R/W	0x00
0x1D	RDR2	RLOS Data Squelch Disable Register 2	R/W	0x00

3.2 Global Register

0x0—Global Control Register (GC)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	BINTR	Reserved	TMONTST	INTEN	RESET
Default	—	—	—	X	0	0	0	0

BINTR Interrupt Status

0 = No alarm interrupt is pending

1 = One or more alarm interrupt is pending

NOTE: The BINTR bit may be different from the hardware BINTR~ pin because BINTR~ may be masked by the INTEN bit.

RESERVED Reserved

This bit is reserved for internal testing and should be kept low for normal operation.

TMONTST Tx Monitor Test

0 = Normal operation for TLOS

1 = Asserts all TLOS outputs; this pin is used to test board-level functionality downstream from the TLOS outputs

INTEN Interrupt Enable

0 = Open drain BINTR~ pin is held inactive

1 = BINTR bit propagates to the BINTR~ pin.

NOTE: BINTR~ is active low.

RESET Software reset

Setting the software reset bit initializes the resettable digital logic and analog control lines. All register bits, except the reset bit, will be initialized to the default state. The device will stay in reset until the reset bit is cleared.

NOTE: Performing a hardware reset via the reset pin will clear the software reset bit.

3.3 Per Port Registers

0x1–0xC—Portn Control Register (PCn)

Bit	7	6	5	4	3	2	1	0
Name	ENCDECDIS	LBO	PD~	RLOOP	LLOOP	REQH	E3	XOE
Default	0	0	0	0	0	1	0	0

ENDECDIS Encoder/Decoder Disable
- 0 = Device accepts NRZ data on TNRZ (TPOS) and outputs decoded single-ended data on RNRZ (RPOS)
- 1 = Device accepts bipolar AMI/B3ZS/HDB3 data on TPOS/TNEG and outputs receive bipolar data on RPOS/RNEG

LBO Line Build Out
- 0 = Line Build Out disabled (used for transmit cable lengths ≥ 450 feet)
- 1 = Line Build Out enabled (used for transmit cable lengths ≤ 450 feet)

PD~ Per Port Power-down
- 0 = Transmitter and receiver for this port are disabled. The alarms (RLOS and TLOS) from a powered down port will read back 0 (no loss of signal). An interrupt will not be generated while the port is powered down. If interrupts are enabled, an interrupt will be generated during a port power down (PD~ transitions from high to low) if there is a loss of signal on the port while the port is being powered down. Similarly an interrupt will also be generated during power up (PD~ transitions from low to high) if there is a loss of signal the port while the port is being powered up.
- 1 = Normal operation

RLOOP Remote Loopback
- 0 = Normal operation
- 1 = Remote Loopback enabled for this port

LLOOP Local Loop Back
- 0 = Normal operation
- 1 = Local Loopback enabled for this port

REQH Receive Equalizer High
- 0 = Receive Equalizer is forced to low gain. Used for E3 mode operation or to correctly receive square DS3 pulses.
- 1 = Used for normal DS3 operation. This setting is not recommended for E3 mode as it may over-equalize the received signal.

E3 E3 Mode
- 0 = DS3/STS-1 mode
- 1 = E3 mode

XOE Transmit Output Enable
- 0 = Transmit output disabled
- 1 = Transmit output enabled

3.4 Alarm Registers

The Alarm Registers provide real time status of the Receive Loss Of Signal (RLOS) alarms and the Transmit Loss Of Signal (TLOS) alarms.

0x10—RLOS Alarm Register 1 (RALMR1)

Bit	7	6	5	4	3	2	1	0
Name	RALM8	RALM7	RALM6	RALM5	RALM4	RALM3	RALM2	RALM1

RALMn Receive Loss Of Signal Alarm status
0 = No Loss of Signal
1 = Loss of Signal Alarm

0x11—RLOS Alarm Register 2 (RALMR2)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RALM12	RALM11	RALM10	RALM9

RALMn Receive Loss Of Signal Alarm status
0 = No Loss of Signal
1 = Loss of Signal Alarm

0x12—TLOS Alarm Register 1 (TALMR1)

Bit	7	6	5	4	3	2	1	0
Name	TALM8	TALM7	TALM6	TALM5	TALM4	TALM3	TALM2	TALM1

TALMn Transmit Loss Of Signal Alarm status
0 = No Loss of Signal
1 = Loss of Signal Alarm

0x13—TLOS Alarm Register 2 (TALMR2)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	TALM12	TALM11	TALM10	TALM9

TALMn Transmit Loss Of Signal Alarm status
0 = No Loss of Signal
1 = Loss of Signal Alarm

3.5 Interrupt Status Registers

The appropriate Loss Of Signal (RLOS/TLOS) interrupt status bit is set when the corresponding loss of signal alarm is set (goes from inactive to active) or cleared (goes from active to inactive). The interrupt status bits are cleared when the register is read.

0x14—RLOS Interrupt Status Register 1 (RISR1)

Bit	7	6	5	4	3	2	1	0
Name	RIS8	RIS7	RIS6	RIS5	RIS4	RIS3	RIS2	RIS1

RISn Receive Loss Of Signal (RLOS) Interrupt status
0 = No RLOS interrupt pending
1 = RLOS interrupt pending

0x15—RLOS Interrupt Status Register 2 (RISR2)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RIS12	RIS11	RIS10	RIS9

RISn RLOS Interrupt status
0 = No RLOS interrupt pending
1 = RLOS interrupt pending

0x16—TLOS Interrupt Status Register 1 (TISR1)

Bit	7	6	5	4	3	2	1	0
Name	TIS8	TIS7	TIS6	TIS5	TIS4	TIS3	TIS2	TIS1

TISn Transmit Loss Of Signal (TLOS) Interrupt status
0 = No TLOS interrupt pending
1 = TLOS interrupt pending

0x17—TLOS Interrupt Status Register 2 (TISR2)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	TIS12	TIS11	TIS10	TIS9

TISn TLOS Interrupt status
0 = No TLOS interrupt pending
1 = TLOS interrupt pending

3.6 Interrupt Enable Registers

Setting the appropriate RLOS/TLOS Interrupt Enable bit will allow the corresponding interrupt status register bit to propagate to the BINTR bit in the Global Control Register. If the INTEN bit is set in the Global Control Register, BINTR will propagate to the BINTR~ pin.

0x18—RLOS Interrupt Enable Register 1 (RIER1)

Bit	7	6	5	4	3	2	1	0
Name	RIE8	RIE7	RIE6	RIE5	RIE4	RIE3	RIE2	RIE1
Default	0	0	0	0	0	0	0	0

RIEn RLOS Interrupt enable
0 = RLOS interrupt disabled
1 = RLOS interrupt enabled

0x19—RLOS Interrupt Enable Register 2 (RIER2)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RIE12	RIE11	RIE10	RIE9
Default	0	0	0	0	0	0	0	0

RIEn RLOS Interrupt enable
0 = RLOS interrupt disabled
1 = RLOS interrupt enabled

0x1A—TLOS Interrupt Enable Register 1 (TIER1)

Bit	7	6	5	4	3	2	1	0
Name	TIE8	TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1
Default	0	0	0	0	0	0	0	0

TIEn TLOS Interrupt enable
0 = TLOS interrupt disabled
1 = TLOS interrupt enabled

0x1B—TLOS Interrupt Enable Register 2 (TIER2)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	TIE12	TIE11	TIE10	TIE9
Default	0	0	0	0	0	0	0	0

TIEn TLOS Interrupt enable
0 = TLOS interrupt disabled
1 = TLOS interrupt enabled

3.7 RLOS Threshold Control Registers

0x0D—RMTR1 (RLOS Max and Threshold Register 1)

Bit	7	6	5	4	3	2	1	0
Name	RM4	RT4	RM3	RT3	RM2	RT2	RM1	RT1
Default	0	0	0	0	0	0	0	0

RMn&RTn RLOS Maximum and RLOS Threshold
See Table 2-6 for RLOS threshold control bits.

0x0E—RMTR2 (RLOS Max and Threshold Register 2)

Bit	7	6	5	4	3	2	1	0
Name	RM8	RT8	RM7	RT7	RM6	RT6	RM5	RT5
Default	0	0	0	0	0	0	0	0

RMn&RTn RLOS Maximum and RLOS Threshold
See Table 2-6 for RLOS threshold control bits.

0x0F—RMTR3 (RLOS Max and Threshold Register 3)

Bit	7	6	5	4	3	2	1	0
Name	RM12	RT12	RM11	RT11	RM10	RT10	RM9	RT9
Default	0	0	0	0	0	0	0	0

RMn&RTn RLOS Maximum and RLOS Threshold
See Table 2-6 for RLOS threshold control bits.

3.8 RLOS Data Squelch Disable Registers

0x1C—RDR1 (RLOS Disable Register 1)

Bit	7	6	5	4	3	2	1	0
Name	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1
Default	0	0	0	0	0	0	0	0

RDn RLOS disable
0 = RLOS auto data squelch enabled
1 = RLOS no data squelch disabled

0x1D—RDR2 (RLOS Disable Register 2)

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RD12	RD11	RD10	RD9
Default	0	0	0	0	0	0	0	0

RDn RLOS disable
0 = RLOS auto data squelch enabled
1 = RLOS no data squelch disabled

4.0 Applications

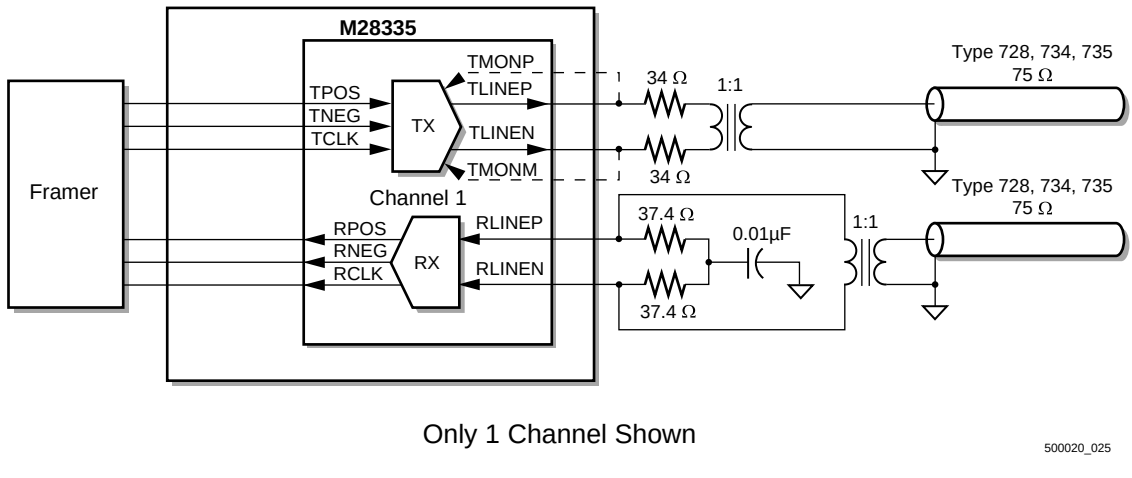
The M28335 can be used in a variety of applications.

4.1 Line Interface Example

Figure 4-1 illustrates an example of a DS3 line being terminated by the M28335. The data and clock are extracted and passed on to the framer chip for further data manipulation and user interface.

It is important to employ high-frequency design techniques for the printed board layout.

Figure 4-1. DS3 Line Interface Example



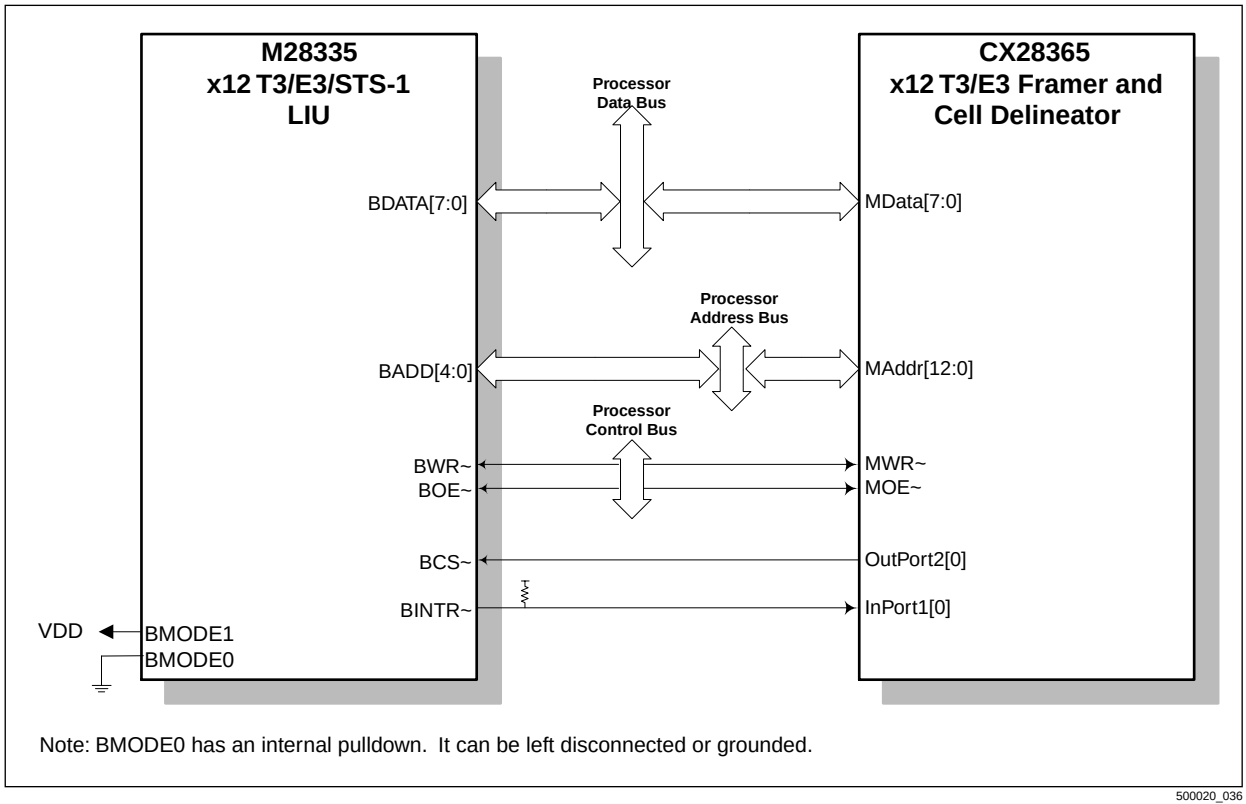
GENERAL NOTE:

1. All transformers are part number T3001 from Pulse Technology. See Recommended Vendors, Section 4.5.6.
2. TMONP and TMONM are denoted by dotted lines.

4.2 Interface Example to CX28365 in Bus Mode

The M28335 can be interfaced to the CX28365 x12 T3/E3 Framer and Cell Delineator without any glue logic as illustrated in Figure 4-2. The M28335 can be configured in Bus mode to provide more flexible control. One line of the Framer/ Delineator OutPort2 can be configured to provide a “Chip-Select” for the M28335. One line of the InPort1 of the Framer/Delineator can be configured as interrupt input to receive the interrupt from the M28335. The BADD bus and BDATA bus of the M28335 are located in the processor address and data bus respectively. The TLOS and RLOS status can be accessed through the M28335’s internal registers. The TLOS and RLOS hardware status from the M28335 can be used to drive LEDs to provide a real-time display of the status of the lines, or they can be used for further status processing.

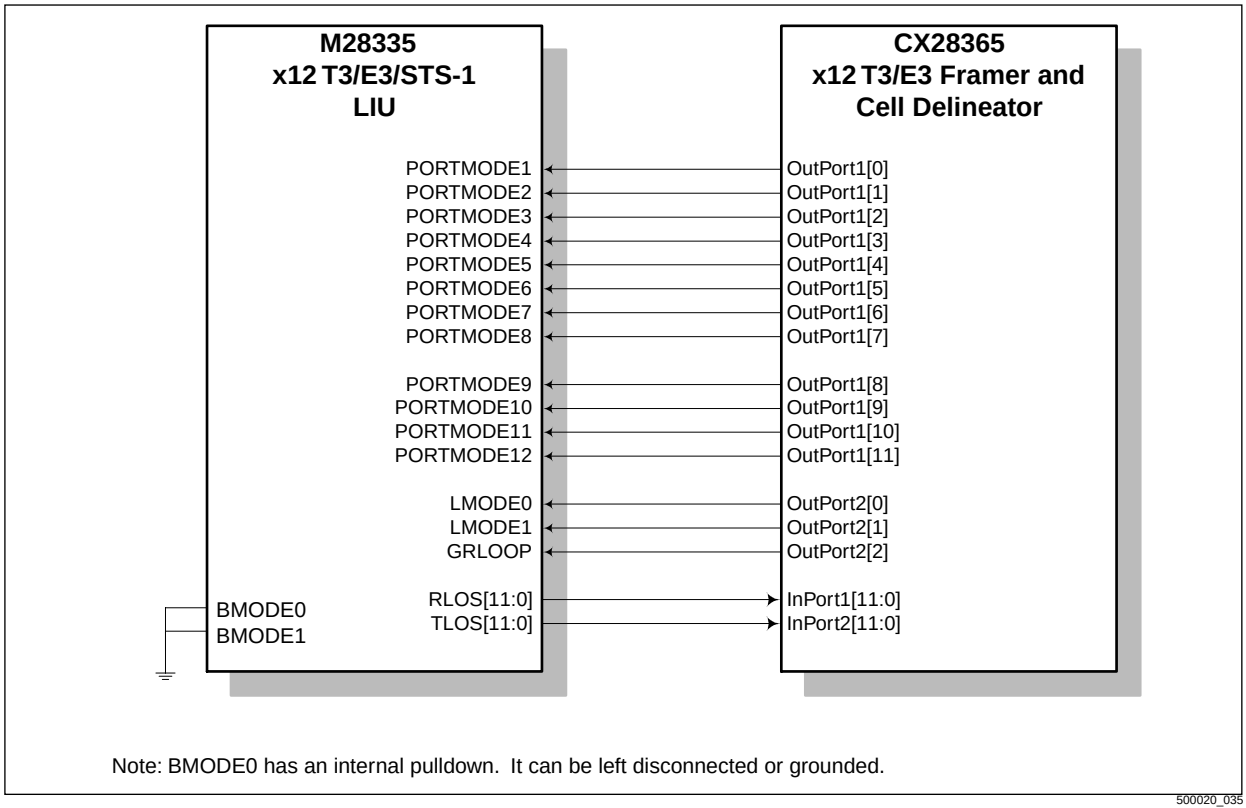
Figure 4-2. Interface to CX28365 in Bus Mode



4.3 Interface Example to CX28365 in Hardware Mode

The M28335 can be interfaced to the CX28365 x12 T3/E3 Framer and Cell Delineator in hardware mode as illustrated in Figure 4-3. OutPort1 of the Framer/ Delineator can be configured as output to control the twelve PORTMODE lines of the M28335. Three of the OutPort2 lines of the Framer/Delineator can be configured as output to handle the global remote loop back and chip-wide mode controls. InPort1 and InPort2 can be configured as input to monitor the RLOS and TLOS from the M28335.

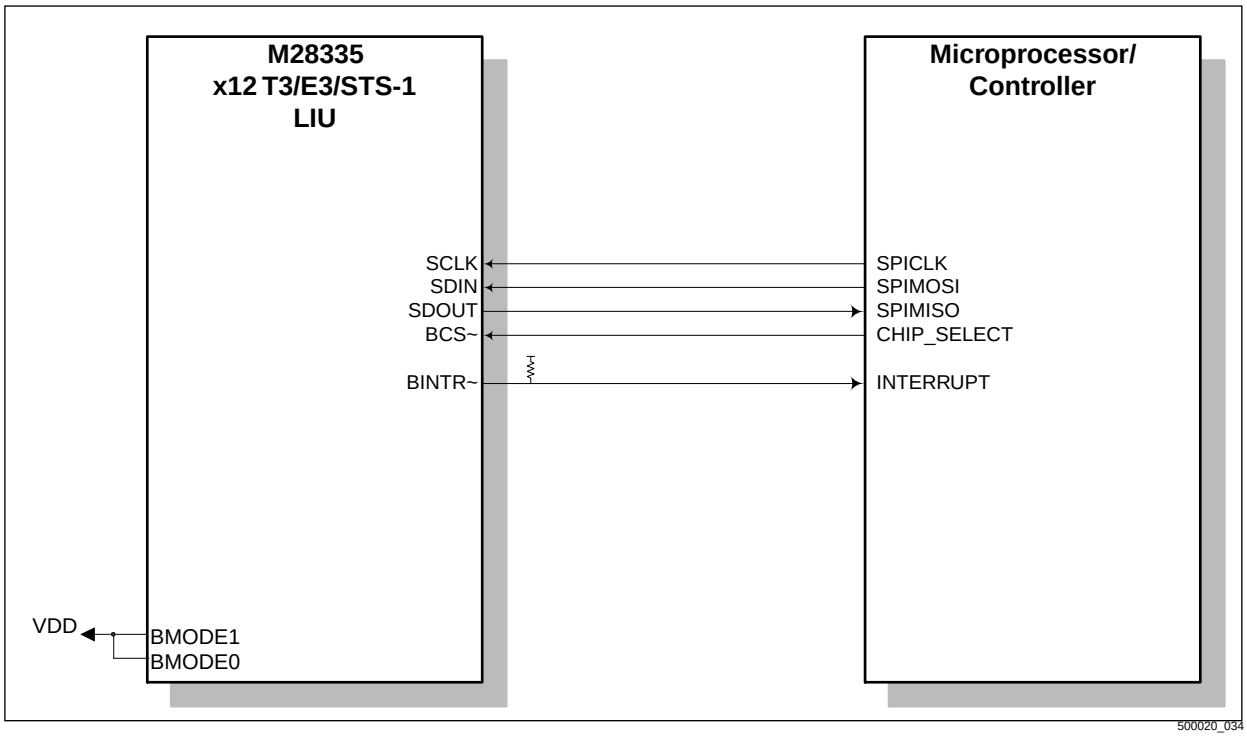
Figure 4-3. Interface to CX28365 in Hardware Mode



4.4 Serial Mode Interface Example

The M28335 can be interfaced to a microprocessor or microcontroller that supports a Serial Peripheral Interface (SPI) as shown in Figure 4-4. The microprocessor/ microcontroller SPI is working as a master. It generates the SPICLK that shifts in the data from the M28335 SDOUT pin to its SPI Master In, Slave Out (SPIMISO) pin and shifts out data to the M28335 SDIN pin through its SPI Master Out, Slave In (SPIMOSI) pin. The microprocessor/microcontroller also provides the chip-select function and receives the interrupt from the M28335.

Figure 4-4. Serial Mode Interface Example



4.5 PCB Design Considerations for the M28335

The M28335 is a mixed signal 12-port LIU device operating at frequencies up to 51.84 MHz. This calls for a careful design of the PCB layout.

Some design considerations are outlined below.

4.5.1 Power Supply and Ground Plane

A single power plane with bulk capacitors (typically 10 µf) distributed throughout the board will mitigate most power rail-related voltage transients. A bulk capacitor should also be placed where the power enters the board. Because this M28335 is a BGA, routing of decoupling capacitors to power pins can be very difficult. It is recommended that that decoupling capacitors only be routed directly to the power pin if they can be placed within 1/8 of an inch of the pin. Decoupling capacitors should be dispersed around the outside of the chip on the top side and underneath the chip on the bottom side of the board. It is recommended that 0.1 µf, 0.01 µf, and 0.001 µf decoupling capacitors be used. All three values are not required on each pin, but values should be dispersed uniformly to filter different frequencies of noise. 10 µf tantalum capacitors should be placed on all four corners of the chip.

A continuous ground plane is the best way to minimize ground impedance. Most ground noise is produced by the return currents and power supply transients during switching. This effect is minimized by reducing the ground plane impedance.

4.5.2 Component Placement

4.5.2.1 RBIAS Resistor

It is important to keep the RBAIS pins quiet, as any noise coupled to these pins affect the internal references. The RBIAS resistors should be placed as close as possible to the RBIAS pins and no digital signals should be routed near the pins or the resistors. Additionally, it would be wise to guard the pin, resistor, and traces with ground vias.

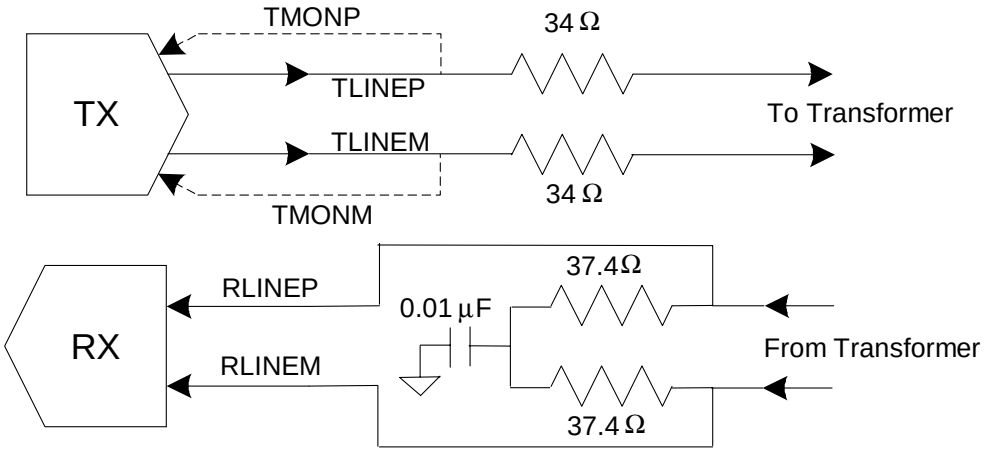
4.5.2.2 VGG Decoupling

It is recommended that the VGG pin be decoupled with a 0.1 µf, 0.01 µF and 0.001 µf capacitors. These capacitors should be placed close to the VGG pin.

4.5.2.3 Termination Resistors and Capacitors

The termination resistors and capacitors on the receive RLINE pins should be placed as close the receiver input on the chip as possible. The series resistors for the transmit TLINE pins should also be placed as close to the transmitter output pins as possible, but are less of a priority then the RLINE.

Figure 4-5. TX/RX Terminations



4.5.3 Impedance Matching

It is critical that both the transmit and receive traces around the transformers and the matching resistors be kept to a minimum length and that the trace impedance be matched to 75 ohms.

The transmit signals should be routed both differentially and single ended. Between the device and the transformer the signals should be routed 75 ohm differentially. The signals should be routed single ended between the transformer and the BNC connector.

The receive signals should be routed differentially between the transformers and either differentially or single ended from the transformers to the BNC connectors, depending on the application. If the application requires ground termination it is recommended that the signals be routed single ended. If the application does not require ground termination, then the signals can be routed differentially.

To route signals differentially, the signal pair (positive and negative) should be 75 ohm coupled and should be surrounded by solid power/ground planes (buried strip line) or be coupled to a power/ground plane (microstrip). Buried strip line is recommended for internal layers while microstrip line is used for signals routed on surface layers. There should be no discontinuity in the planes during the path of the signal traces.

Single ended signals should be 75 ohm coupled between power/ground planes for inner layers or 75 ohm coupled to a power/ground plane on the outer layers. There should be no discontinuities in the power/ground planes over the trace path.

Impedance discontinuities occur when a signal passes through vias and travels between layers. It is recommended to minimize the number of vias and layers that the transmit/receive signals travel through in the design.

4.5.4 Other Passive Parts

Mindspeed recommends the use of 1:1 transformers for coupling the BNC connectors to the device. The M28335 EVM uses two Pulse Tx3051 (12 transformer) devices to handle the 12 Tx and Rx channels.

It is recommended that a 220 µF tantalum capacitor be used where the power enters the board.

4.5.5 IBIS Models

IBIS (Input/Output Buffer Interface Specification) models for the M28335 are available from Mindspeed's web site (www.Mindspeed.com).

4.5.6 Recommended Vendors

	Product: Transformers		**Product: Crystals**
America	**Pulse**		**Crystek Corp.**
Address:	Corporate Office 12220 World Trade Drive San Diego, CA 92128		12730 Commonwealth Drive Fort Myers, FL 33913
Tel:	858-674-8100	Tel:	800-237-3061
Fax:	858-674-8262	Fax:	941-561-1025
		E-mail:	sales@crystek.com
		Web site:	www.crystek.com
Northern Asia	**Pulse** 3F-4, No. 81, Sec. 1 Hsin Tai Wu Road Hsi-Chih Tapei Hsien, Taiwan R.O.C.		
Tel:	886-2-26980228 886-2-26980948		
Northern Europe	**Pulse** 1S2 Huxley Road The Surrey Research Park Guildford, Surrey GU2 5RE United Kingdom		
Tel:	44-1483-401700		
Fax:	44-1483-401701		

Appendix A: Applicable Standards

The applicable standards documents are as follows:

- *ANSI T1.102-1993* (DS3 and STS-1 standard)
- *ANSI T1.404a-1996* (DS3 metallic interface)
- *ITU Recommendation G.703* (DS3 and E3 standard)
- *ITU Recommendation G.823* and *G.824* (jitter and wander)
- *Bellcore GR499*, Issue 1, 12/89 (formerly *TR-TSY-000499*) (DS3 and STS-1 requirements)
- *Bellcore GR253*, Issue 2, 12/91 (formerly *TA-NWT-000253*) (STS-1 requirements and jitter)
- *Bellcore TR-TSY-000191*, Issue 1, 5/86 (AIS and LOS)
- *ETSI TBR24* and *TBR25* (E3 terminal equipment interface)
- *ETSI ETS 300 686* and *ETS 300 687* (E3 standard)
- *AT&T Technical Reference TR54014*, May 1992 (Accunet Interface Specification for DS-3 jitter only)

Appendix B: Power Sequencing

When VGG is operated at 5V, the power-up and power-down sequencing of VGG and VDD (DVDD, RVDD, TVDD) must conform to the diagrams below (See note below). As can be seen, VGG must not be higher than VDD by 3.6V or lower than VDD by 0.5V.

NOTE: VGG can exceed VDD by up to 5V (± 10%) for short durations of less than 10 ms. VGG must never be less than VDD by more than 0.5V.

Figure B-1. Power -up sequence of VGG and VDD.

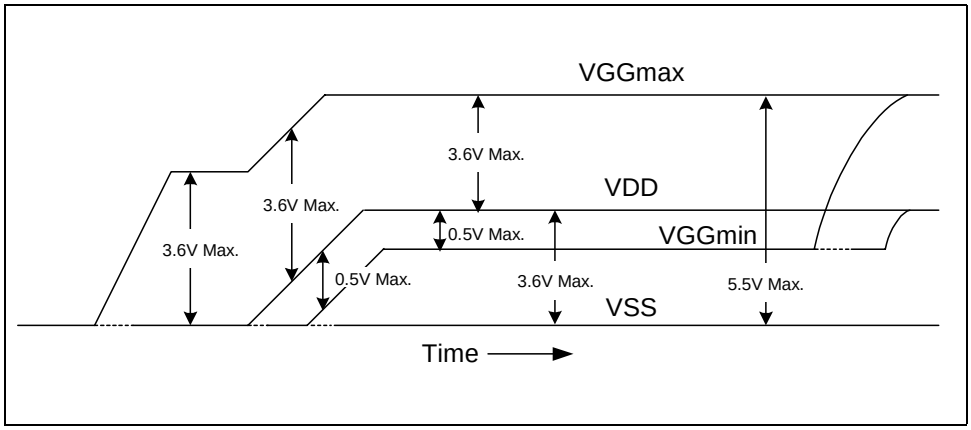
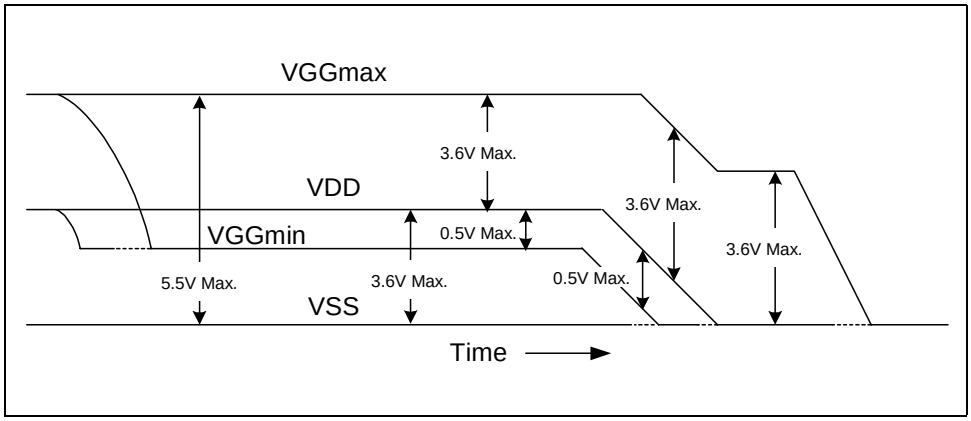


Figure B-2. Power-down sequence of VGG and VDD.



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