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MA28151

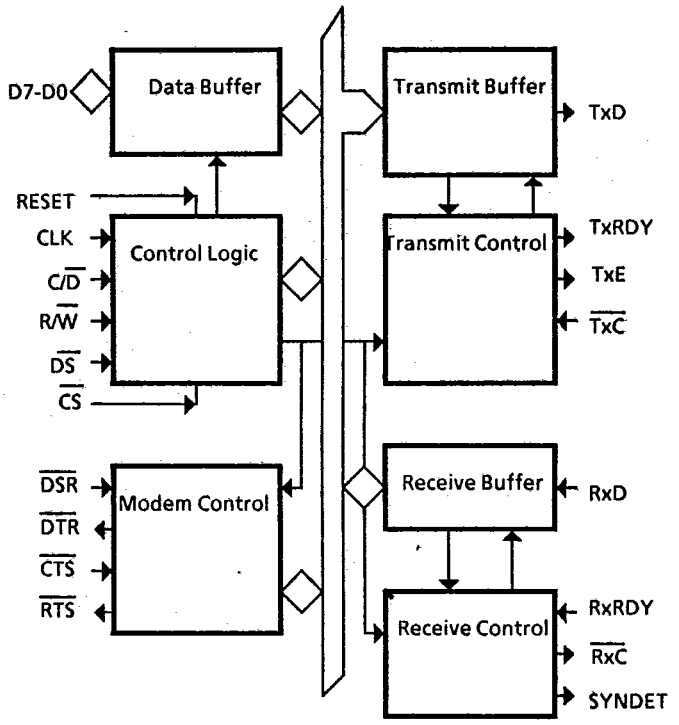
T-75-37-07

Radiation Hard Programmable Communication Interface

FEATURES

- Radiation Hard to 1MRad(Si)
- Latch up free, High SEU immunity
- Silicon-on-Sapphire technology
- Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion
- Asynchronous 5-8 Bit Characters; Clock Rate-1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½ or 2 Stop Bits.
- All Inputs and Outputs are TTL Compatible
- Compatible with the MAS-281 (Mil Std 1750A)

BLOCK DIAGRAM



GENERAL DESCRIPTION

The MA28151 is the enhanced version of the industry standard, 8251 Universal Synchronous Asynchronous Receiver/Transmitter (USART), modified for data communications with the MAS281 microprocessor.
The MA28151 is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it has received a character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY.

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FEATURES

The MA28151 is an advanced design on the industry standard USART, the Intel 8251A. Familiarization time is minimal because of compatibility and involves only the additional features/enhancements and reviewing the AC and DC specifications. The MA28151 incorporates the following features:

* MA28151 has double-buffered data paths with separate I/O registers for control, status. Data in and Data out, which considerably simplifies control programming and minimizes CPU overhead.
* In synchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
* A refined Rx initialisation prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
* At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.,
* Tx Enable logic enhancement prevents a Tx Disable command from halting transmission unit all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
*When external Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
* Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be continuously detected and also by clearing the Rx register to all 1's whenever Enter Hunt command is issued in Sync mode.
* As long as the MA28151 is not selected, the RD/W and DS lines do not affect the internal operation of the device.
* The MA28151 Status can be read at any time but the status update will be inhibited during status read.
* The MA28151 is free from extraneous glitches providing higher speed and better operating margins.
* Synchronous Baud rate is from DC to 64K.
*Asynchronous Baud rate is from DC to 19.2K.

GENERAL

The MA28151 is a Universal Synchronous /Asynchronous Receiver/Transmitter designed for use with the MAS281 microprocessor. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The MA28151 can support most serial data techniques in use, including IBM bi-sync.

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence , the interface should appear transparent to the CPU , simple input or output of byte-oriented system data.

DATA BUS BUFFER

This 3-state bidirectional, 8-bit buffer is used to interface the MA28151 to the system Data Bus. Data is transmitted or received by the buffer upon execution of OUTput or INput instructions of the CPU. Control word, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-in and Data-out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET

A high on this input forces the MA28151 into idle mode. The device will remain at idle until a new set of control words is written into the MA28151 to program its functional definition. Minimum RESET pulse width is 6 t_{cy} (clock must be running).

A command reset operation also puts the device into the idle state.

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CLK (CLOCK)

The CLK input is used to generate internal device timing and is normally connected to the clock generator(OSC) of the MAS281. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver of Transmitter data bit rates.

DS (Data Strobe)

This input indicates that a data transfer is taking place. During a CPU write operation the MA28151 reads data from the bus on the rising edge of DS. During a read operation the MA28151 can output data while DS is low. Data is valid on the rising edge of DS.

RD/WR (Read/Write Select)

A high on the RD/WR input indicates a read of data or status information from the MA28151. A low on this input indicates a transfer of data or control words into the MA28151. The RD/W line is valid only when DS is low.

C/D	RD/WR	DS	CS	ACTION
0	1	0	0	28151 TO CPU
0	0	0	0	CPU TO 28151
1	1	0	0	STATUS TO CPU
1	0	0	0	CPU TO CONTROL
X	X	1	0	BUS TRISTATE
X	X	X	1	BUS TRISTATE

C/D (Control/Data)

This input, in conjunction with the DS and RD/WR inputs, informs the MA28151 that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL/STATUS ; 0 = DATA

CS (Chip Select)

A low on this input selects the MA28151. No reading or writing will occur unless the device is selected. When CS is high, the Data Bus is in the float state and the DS and RD/WR lines have no effect on the chip.

Modem Control

The MA28151 has a set of control inputs and outputs that can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

DSR (Data Set Ready)

The DSR input signal is a general-purpose, 1-bit inverting input port. It's condition can be tested by the CPU using a Status Read operation. The DSR input is normally used to test modem conditions such as Data Set Ready.

DTR (Data Terminal Ready)

The DTR output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The DTR output signal is normally used for modem control such as Data Terminal Ready.

RTS (Request to Send)

The RTS output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The RTS output signal is normally used for modem control such ad Request to Send.

CTS (Clear to Send)

A low on this input enables the MA28151 to transmit serial data if the Tx Enable bit in the Command byte is set to a high. If either a Tx Enable off or CTS off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx disable command, before shutting down.

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TRANSMITTER BUFFER

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of TxC. The transmitter will begin transmission upon being enabled if CTS = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable or CTS = 1 or the transmitter is empty.

TRANSMITTER CONTROL

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (TRANSMITTER READY)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system , since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation TxRDY is automatically reset by the falling edge of DS (with RD/W low) when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data input Register.

TxE (TRANSMITTER EMPTY)

When the MA28151 has no characters to send, the TxEMPTY output will go high. It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU knows when to turn the line around in the half-duplex operational mode.

In the Synchronous mode, a high on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or being transmitted automatically as fillers TxEMPTY does not go low when the SYNC characters are being shifted out.

$\overline{\text{TxC}}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the TxC frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual TxC frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the TxC.

For Example

If Baud Rate equals 110 Baud
TxC equals 110Hz in the 1x mode
TxC equals 1.72 KHz in the 16x mode
TxC equals 7.04 KHz in the 64x mode
The falling edge of TxC shifts the serial data out of the MA28151.

RECEIVER BUFFER

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communications techniques and sends an assembled character to the CPU. Serial data is input to the RxD pin, and is clocked in on the rising edge of RxC.

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Receiver Control

This functional block manages all receiver-related activities which consist of the following features.

The RxD initialization circuit prevents the MA28151 from mistaking an unused input line for an active low data line in the break condition. Before starting to receive serial characters on the RxD line a valid 1 must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit.

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

RxRDY (Receiver Ready)

This output indicates that the MA28151 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

RxEnable, when off holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register. Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring , the overrun error will be set and the old character will be lost.

$\overline{\text{RxC}}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received . In Synchronous Mode the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous Mode, the Baud Rate is a fraction of the actual RxC frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 of the Receiver Clock.

For Example
Baud Rate equals 300 Baud, if
RxC equals 300 Hz in the 1x mode:
RxC equals 4800 Hz in the 16x mode
RxC equals 19.2 KHz in the 64x mode.

Baud Rate equals 2400 Baud if
RxC equals 2400Hz in the 1x mode
RxC equals 38.4 KHz in the 16x mode;
RxC equals 153.6 KHz in the 64x mode.
Data is sampled into the MA28151 on the rising edge of RxC.

NOTE: In most communications systems, the MA28151 will be handling both the transmission and reception operations of a single link. Consequently the Receive and Transmit Baud Rates will be the same Both TxC and RxC will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

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SYNDET (SYNC Detect/BRKDET Break Detect)

This pin is used in Synchronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode, low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go high to indicate that the MA28151 has located the SYNC character in the Receive mode. If the MA28151 is programmed to use double Sync characters (bi-sync), the SYNDET will go high in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as input (external SYNC detect mode), a positive going signal will cause the MA28151 to start assembling data characters on the rising edge of the next RxC. Once in SYNC the high input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

BREAK (Async Mode Only)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

$C/\overline{D}$	ACTION
1	MODE INSTRUCTION
1	SYNC CHARACTER 1 (SYNC ONLY) *
1	SYNC CHARACTER 2 (SYNC ONLY) *
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION

TYPICAL DATA BLOCK

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the MA28151 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the MA28151 to support the desired communications format. These control words will program the:BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc.. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the MA28151 is ready to perform its communication functions. The TxRDY output is raised high to signal the CPU that the MA28151 is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the MA28151. Alternatively, the MA28151 receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised high to signal the CPU that the MA28151 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The MA28151 cannot begin transmission until the TxEnable (Transmitter Enable) bit is set in the Command instruction and it has received a Clear To Send (CTS) input. The TxD output will be held in the marking state upon Reset.

* NOTE: The second sync character is skipped if mode instruction has programmed the MA28151 to single character mode. Both sync characters are skipped if mode instruction has programmed the MA28151 to async mode.

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Programming the MA28151

Prior to starting data transmission or reception, the MA28151 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the MA28151 and must immediately follow a Reset operation (internal or external)
The control words are split into two formats:
1. Mode Instruction
2. Command Instruction

MODE INSTRUCTION
This instruction defines the general operational characteristics of the MA28151. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the MA28151 by the CPU, SYNC characters or Command Instructions may be written.

COMMAND INSTRUCTION
This instruction defines a word that is used to control the actual operation of the MA28151.
Both the Mode and Command Instruction must conform to a specified sequence for proper device operation. The Mode instruction must be written immediately following a Reset operation, prior to using the MA28151 for data communications.
All control words written into the MA28151 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the MA28151 at any time in the data block during the operation of the MA28151. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the MA28151 back into the Mode Instruction format. Command Instruction must follow the Mode Instructions or Sync characters.

MODE INSTRUCTION DEFINITION
The MA28151 can be used for either Asynchronous or Synchronous data communications. To understand how the Mode Instruction defines the functional operation of the MA28151 the designer can best view the device as two separate components, one Asynchronous and the other Synchronous, sharing the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.
NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are don't care when writing data to the MA28151, and will be zeros when reading the data from the MA28151.

Test Mode
The Mode Instruction can be used to select a scan path test facility. In this mode a test vector is read in through RxD and read out in TxD. It provides an extensive test of the MA28151 circuit.

Asynchronous Mode (Transmission)
Whenever a data character is sent by the CPU the MA28151 automatically adds a Start bit (low level) followed by the data bits (least significant bit first,) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The Character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of TxC at a rate equal to 1, 1/16 or 1/64 that of the TxC, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.
When no data characters have been loaded into the MA28151 the TxD output remains high (marking) unless a Break (continuously low) has been programmed.

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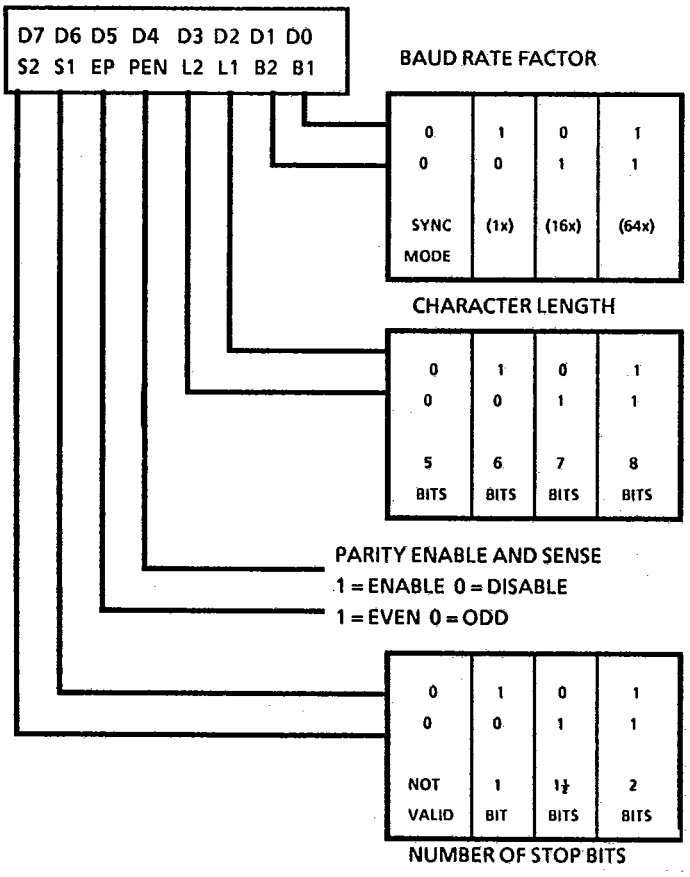
Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16x or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of RxC. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver requires only one stop bit*, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the MA28151. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the MA28151.



Synchronous Mode (Transmission)

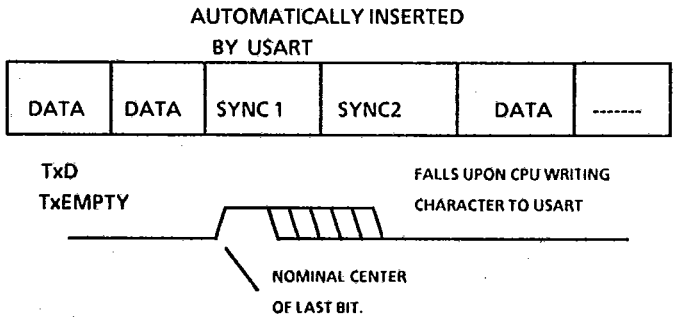
The TxD output is continuously high until the CPU sends its first character to the MA28151 which usually is a SYNC character. When the CTS line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of TxC. Data is shifted out at the same rate as the TxC.

Once transmission has started, the data stream at the TxD output must continue at the TxC rate. If the CPU does not provide the MA28151 with a data character before the MA28151 Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the MA28151.

Synchronous Mode (Receiver)

In this mode character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of RxC. The content of the Rx buffer is compared to every bit boundary with the first SYNC character until a match occurs. If the MA28151 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit, instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the MA28151 out of the HUNT mode. The high level can be removed after one RxC cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.



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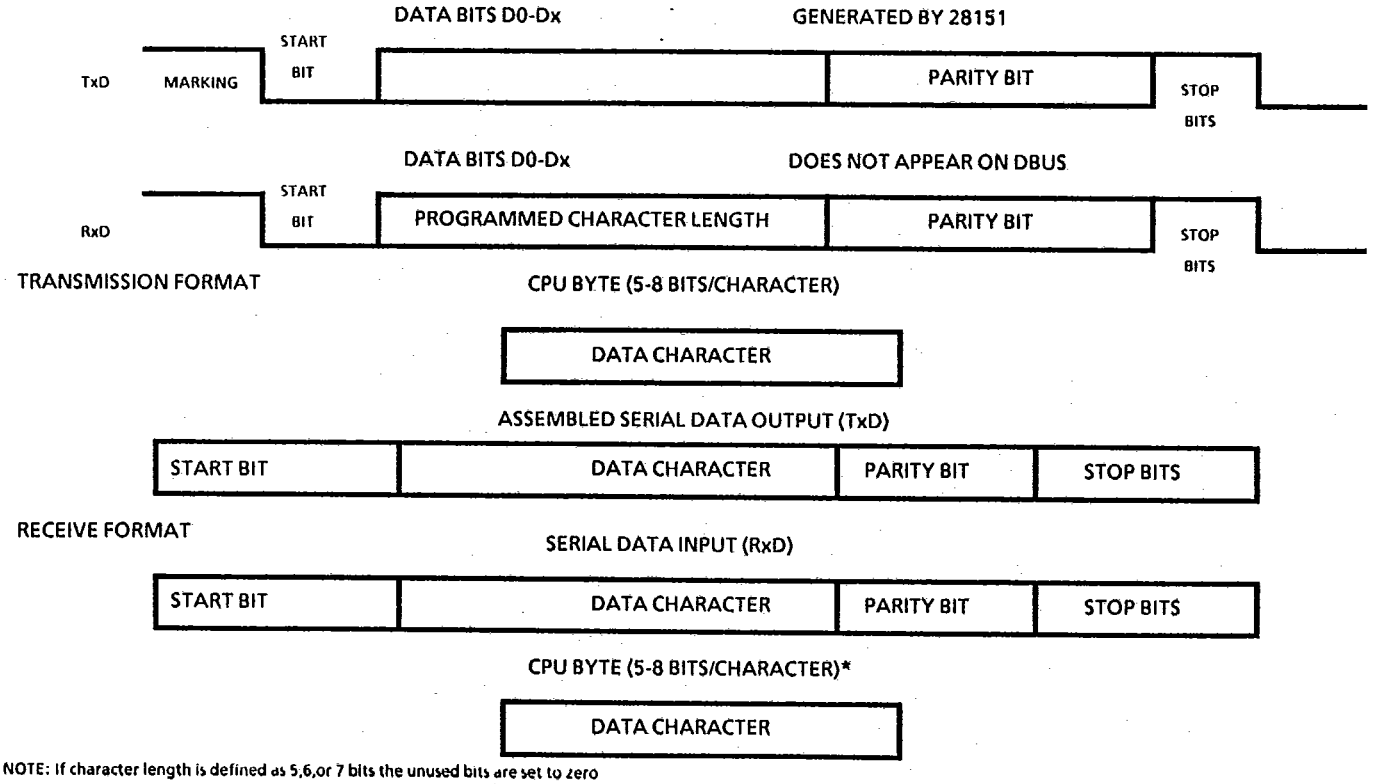
Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a one thus preventing a possible false SYNDET caused by data that happens to be in the Rx buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal of external SYNC has been programmed. This does not cause the MA28151 to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the known word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been contiguously received to gate a SYNDET indication) When external SYNDET mode is selected,internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.

ASYNCHRONOUS MODE



* NOTE: If character length is defined as 5,6,or 7 bits the unused bits are set to zero

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the MA28151 has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communications. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the MA28151 and Sync characters inserted, if necessary, then all further control writes (C/D = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the MA28151 to the Mode instruction format.

NOTE: Internal Reset on Power-up

When power is first applied, the MA28151 may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with C/D = 1 configures sync operation and writes two dummy 00H sync characters. An internal reset command (40H) may then be issued to return the device to the idle state.

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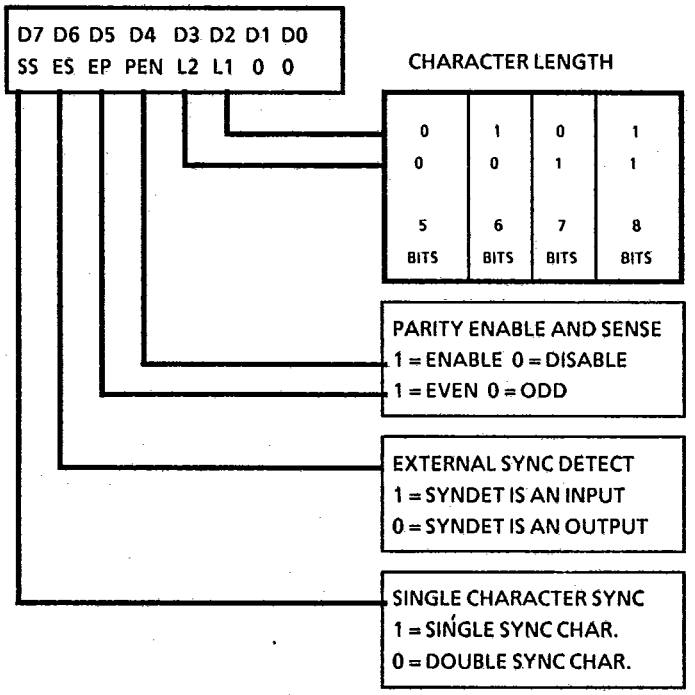
STATUS READ DEFINITION

In data communication systems it is ofter necessary to examine the status of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The MA28151 has facilities that allow the programmer to read the status of the device at any time during the functional operation. (Status update is inhibited during status read).

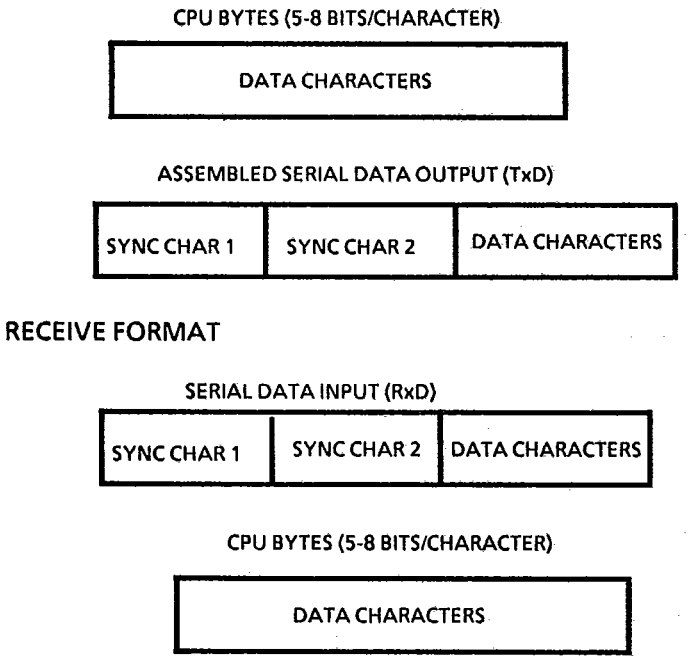
A normal read command is issued by the CPU with C/D = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the MA28151 can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



MODE INSTRUCTION FORMAT, SYNCHRONOUS MODE



DATA FORMAT, SYNCHRONOUS MODE

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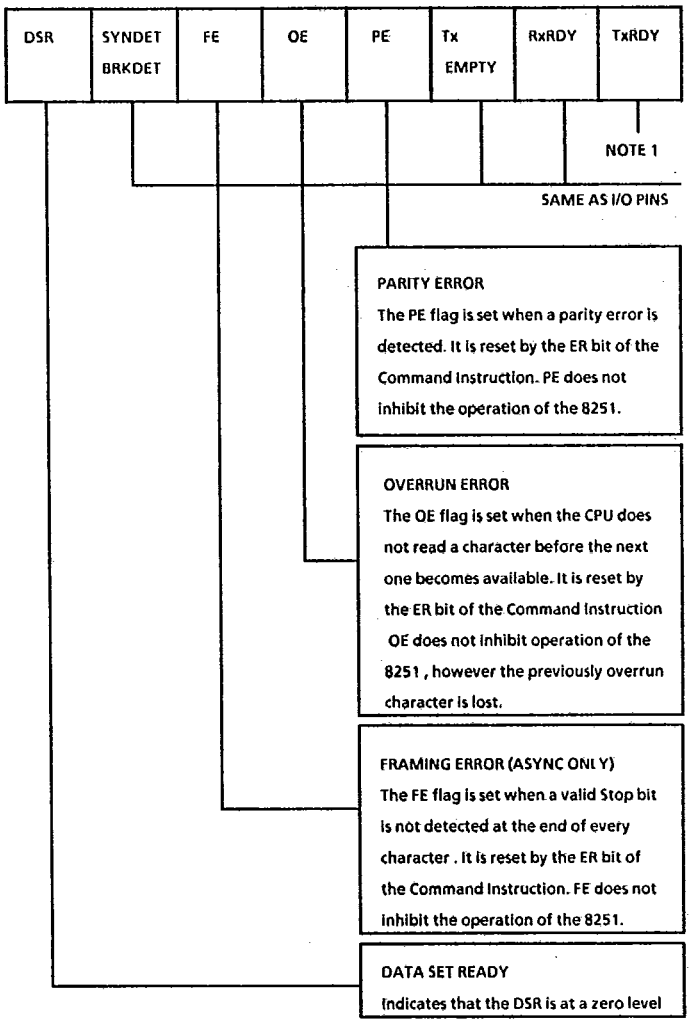
STATUS READ FORMAT.



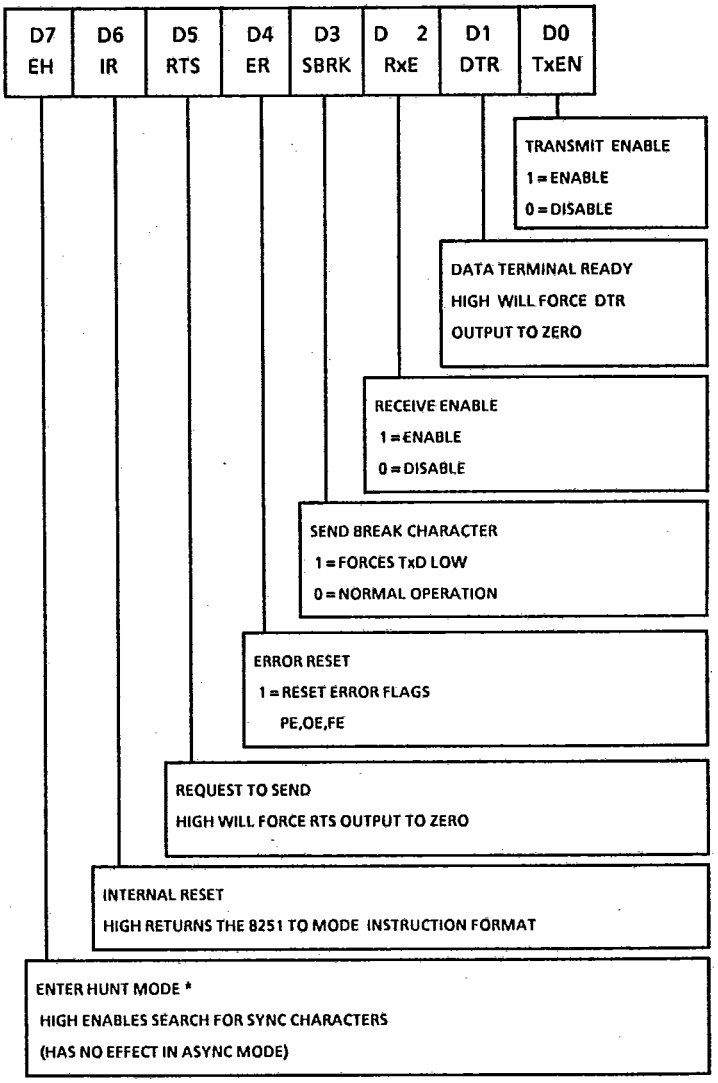
NOTE 1:

TxRDY status bit has different meanings from the Txrdy output pin. The former is not conditioned by CTS and TxEN, the latter is conditioned by both CTS and TxEN.

I.e. TxRDY status bit 0 DB buffer empty

TxRDY pin out = DB buffer empty OR (CTSN = 0) OR (TxEN = 1)

COMMAND INSTRUCTION FORMAT.



*NOTE: ERROR RESET MUST BE PERFORMED WHENEVER RxENABLE AND ENTER HUNT ARE PROGRAMMED

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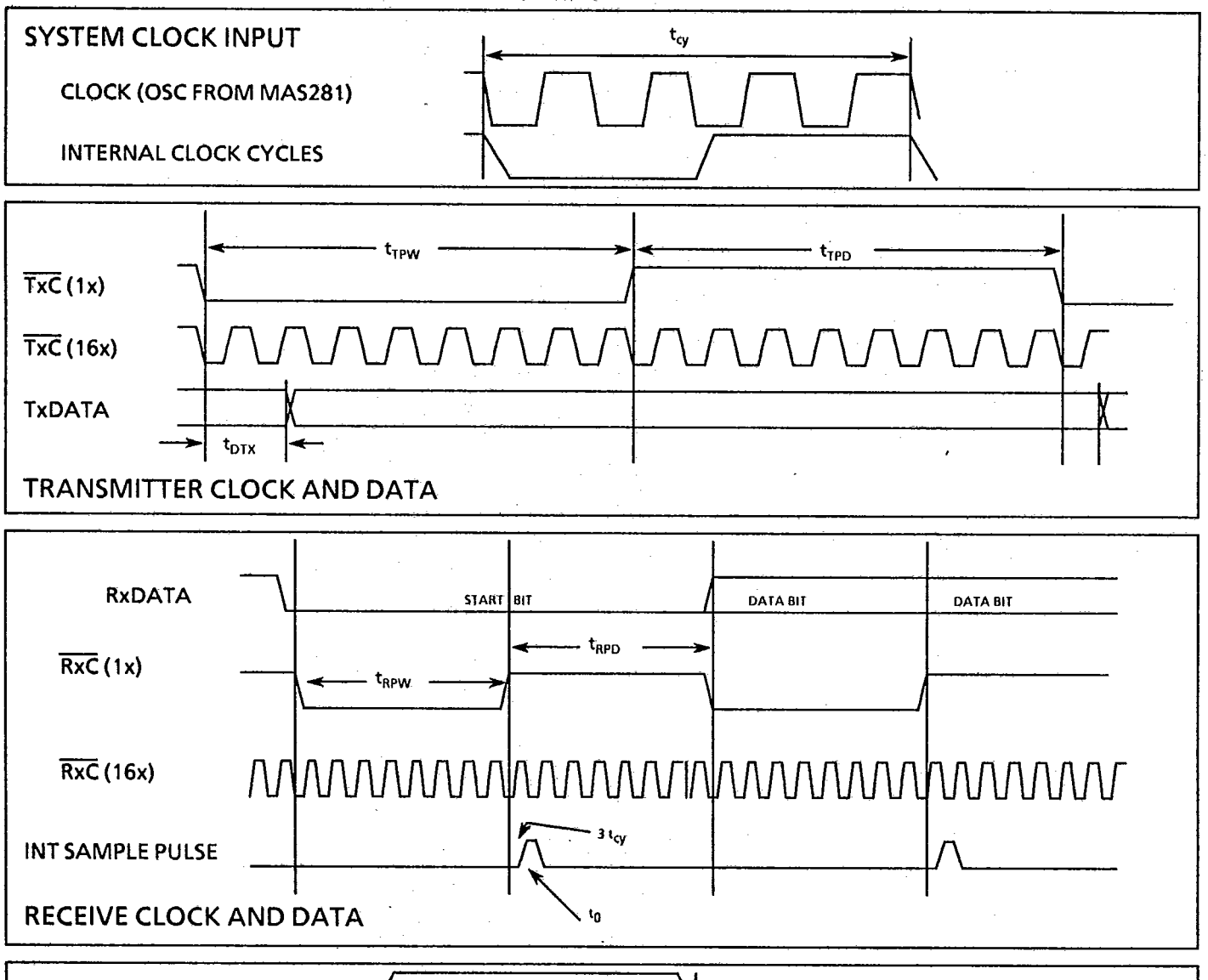
WAVEFORMS



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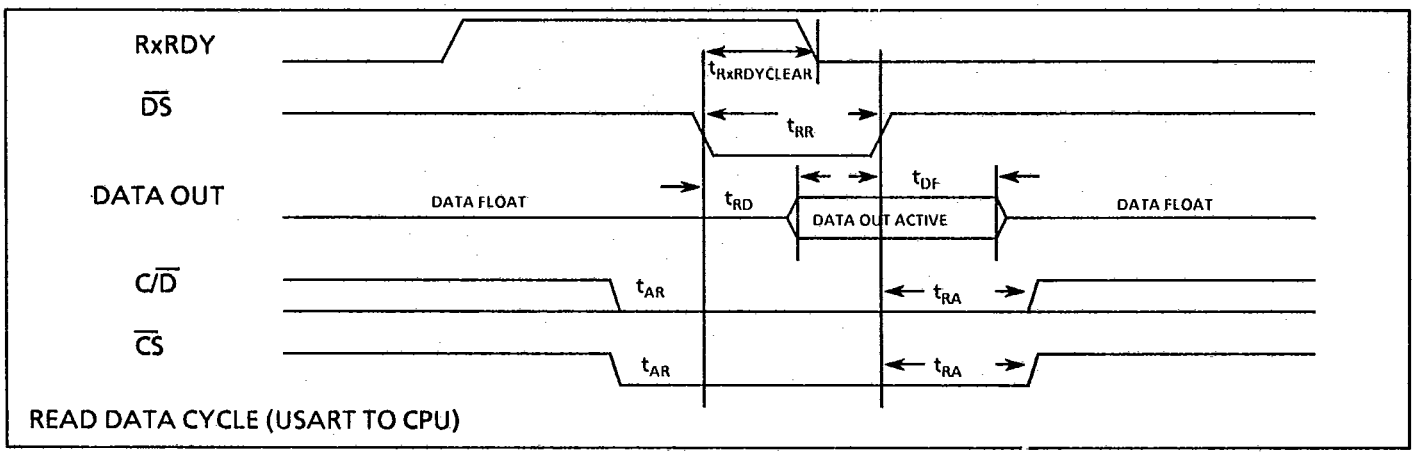
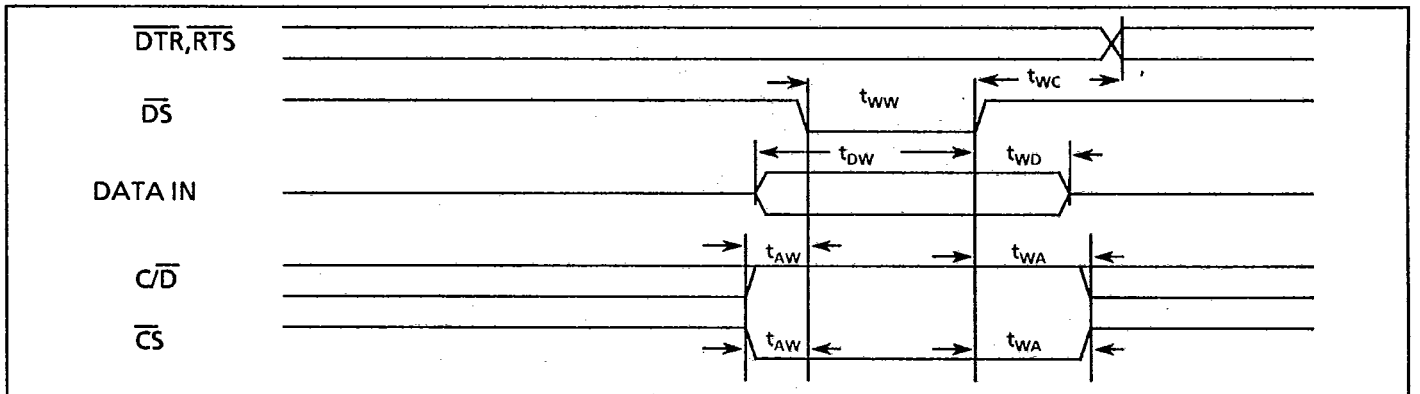
WAVEFORMS (continued)

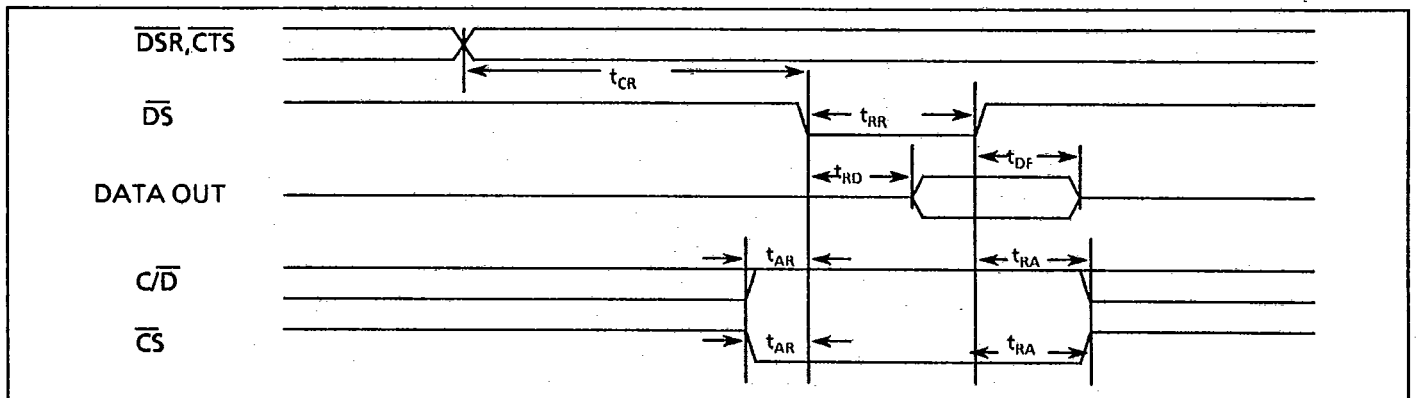


READ DATA CYCLE (USART TO CPU)



WRITE CONTROL OR OUTPUT PORT CYCLE (CPU TO USART)

NOTE : t_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROI BYTE.



READ CONTROL OR INPUT PORT CYCLE (USART TO CPU)

NOTE . t_{CR} INCLUDES THE EFFECT OF CTS ON THE TxENABLE CIRCUITRY

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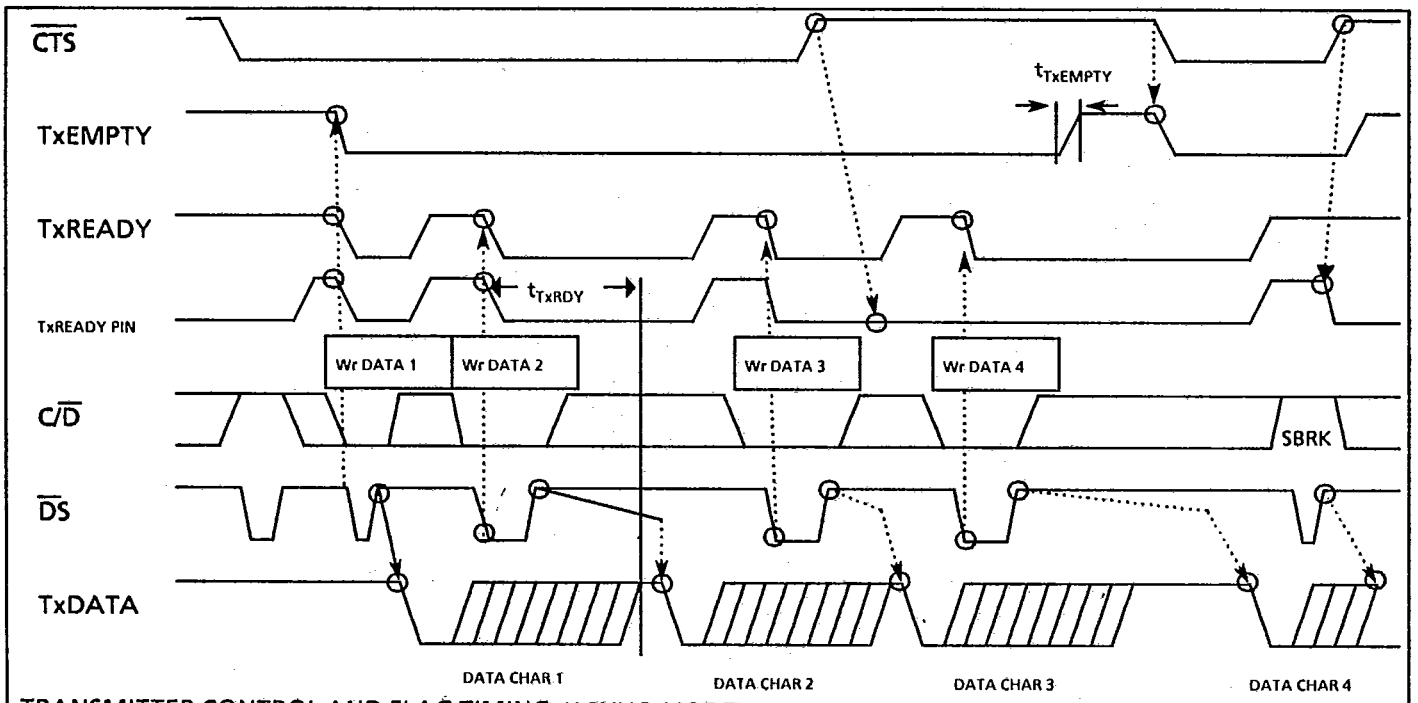
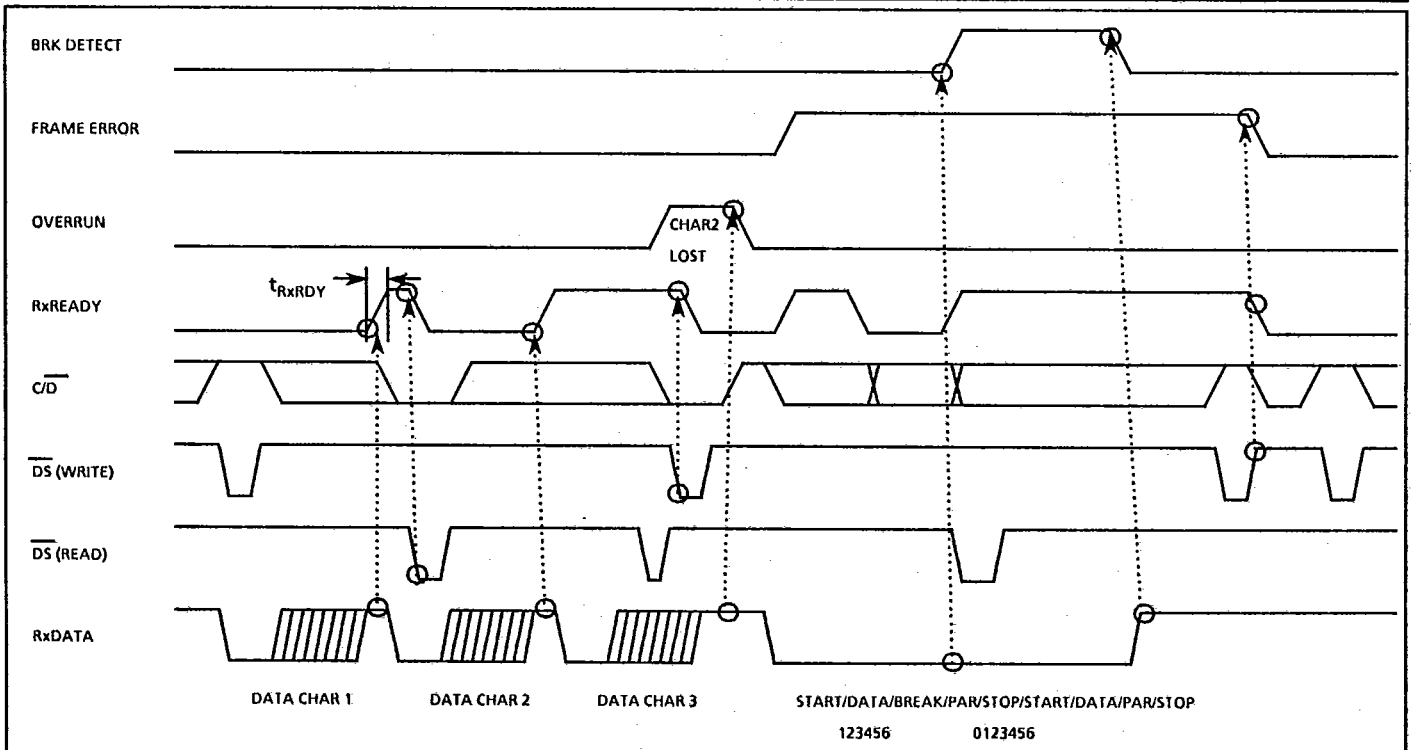


TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE).

EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS.



RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE).

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
SUPPLY VOLTAGE	-0.5	10	V
INPUT VOLTAGE	-0.3	V_{DD} + 0.3	V
CURRENT THROUGH ANY PIN	-20	20	mA
OPERATING TEMP.	-55	125	°C
STORAGE TEMP.	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10%. Over full operating temperature range.

SYMBOL	PARAMETER	TOTAL DOSE RADIATION NOT EXCEEDING $3x10^5$ RAD (Si)			TOTAL DOSE ≤ 1 MRAD (Si)		UNITS	CONDITION
		MIN	TYP	MAX	MIN	MAX		
V_{DD}	SUPPLY VOLTAGE	4.5	5.0	5.5	4.5	5.5	V	
V_{IH}	TTL Input High Voltage	2.0			2.0		V	
V_{IL}	TTL Input Low Voltage			0.8		0.3	V	
V_{OH}	TTL Output High Voltage	2.4			2.4		V	I_{OH} = -0.8mA
V_{OL}	TTL Output low Voltage			0.4		0.4	V	I_{OL} = 2.0mA
I_{IL}	Input Low Current			10		100	uA	V_{DD} = 5.5V, V_{IN} = V_{SS}
I_{IH}	Input High Current			20		100	uA	V_{DD} = 5.5V, V_{IN} = V_{DD}
I_{DD}	Power Supply Current		0.1	1		10	mA	Static

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
t_{CY}	CLOCK PERIOD	240	1000	nS	NOTES 1,5,6.
	CLOCK HIGH PULSE WIDTH	120	t_{CY-90}	nS	
	CLOCK LOW PULSE WIDTH	120		nS	
	CLOCK RISE AND FALL TIME		20	nS	
t_{DTX}	TxD DELAY FROM FALLING EDGE OF TxC		1	uS	
f_{Tx}	TRANSMITTER INPUT CLOCK FREQUENCY 1x BAUD RATE 16x BAUD RATE 64x BAUD RATE	 DC DC DC	 64 310 615	 kHz kHz kHz	
t_{TPW}	TRANSMITTER INPUT CLOCK PULSE WIDTH 1x BAUD RATE 16x AND 64x BAUD RATE	 12 1		 t_{CY} t_{CY}	
t_{TPD}	TRANSMITTER INPUT CLOCK PULSE DELAY 1x BAUD RATE 16x AND 64x BAUD RATE	 15 3		 t_{CY} t_{CY}	
f_{Rx}	RECEIVER INPUT CLOCK FREQUENCY 1x BAUD RATE 16x BAUD RATE 64x BAUD RATE	 DC DC DC	 64 310 615	 kHz kHz kHz	
t_{RPW}	RECEIVER INPUT CLOCK PULSE WIDTH 1x BAUD RATE 16x AND 64x BAUD RATE	 12 1		 t_{CY} t_{CY}	
t_{RPD}	RECEIVER INPUT CLOCK PULSE DELAY 1x BAUD RATE 16x AND 64x BAUD RATE	 15 3		 t_{CY} t_{CY}	
t_{TxRDY}	TxRDY PIN DELAY FROM CENTER OF LAST BIT		8	t_{CY}	NOTE 7
$t_{TxRDY\ CLEAR}$	TxRDY FALL FROM LEADING EDGE OF WR		400	nS	NOTE 7
t_{RxRDY}	RxRDY PIN DELAY FROM CENTER OF LAST BIT		26	t_{CY}	NOTE 7
$t_{RxRDY\ CLEAR}$	RxRDY FALL FROM LEADING EDGE OF RD		400	nS	NOTE 7
$t_{TxEMPTY}$	TxEMPTY FROM CENTER OF LAST BIT	20		t_{CY}	NOTE 7
t_{WC}	CONTROL DELAY FROM RISING EDGE OF WRITE	8		t_{CY}	NOTE 7
t_{CR}	CONTROL TO READ SETUP TIME (DSR,CTS)	20		t_{CY}	NOTE 7

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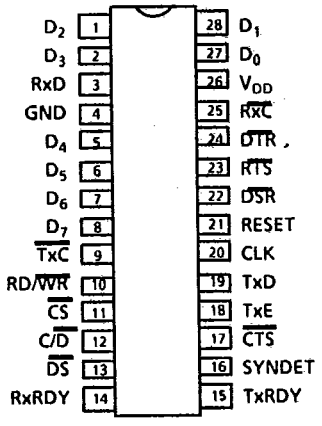
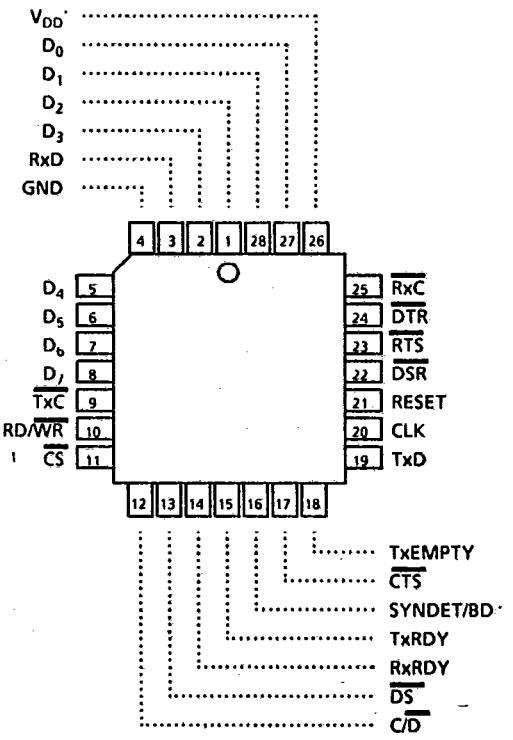
AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AR}	ADDRESS STABLE BEFORE DS(CS,C/D) .	0		ns	NOTE 2
t_{RA}	ADDRESS HOLD TIME BEFORE DS(CS,C/D) .	0		ns	NOTE 2
t_{RR}	DS PULSE WIDTH	50		ns	
t_{RD}	DATA DELAY FROM DS (READ).		200	ns	NOTE 3
t_{DF}	DS TO DATA FLOATING (READ).	10	100	ns	
t_{DW}	DATA SETUP TIME TO DS (WRITE).	150		ns	
t_{WD}	DATA HOLD TIME TO DS (WRITE).	20		ns	
t_{RV}	RECOVERY TIME BETWEEN WRITES (NOT SHOWN)	6		t_{CY}	NOTE 4

NOTES:
1 AC Timings measured V_{OH} = 1.5 V_{OL} = 1.5,
2 CS and Command/Data are considered as addresses.
3 Assumes that address is valid before DS goes low
4 This recovery time is for Mode Initialization only. Write data is allowed when TxRDY = 1. Recovery time between writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5 The TxC and RxC frequencies have the following limitation with respect to clock: For 1xBaud rate, f_{TX} or $f_{RX} \leq 1/(30t_{CY})$: For 16x and 64x Baud rate, f_{TX} or $f_{RX} \leq 1/(4.5t_{CY})$.
6 Reset Pulse Width = $6t_{CY}$ minimum; System clock must be running during Reset.
7 Status update can have a maximum delay of 28 clock periods fromt he event affecting the status.

PIN ASSIGNMENT





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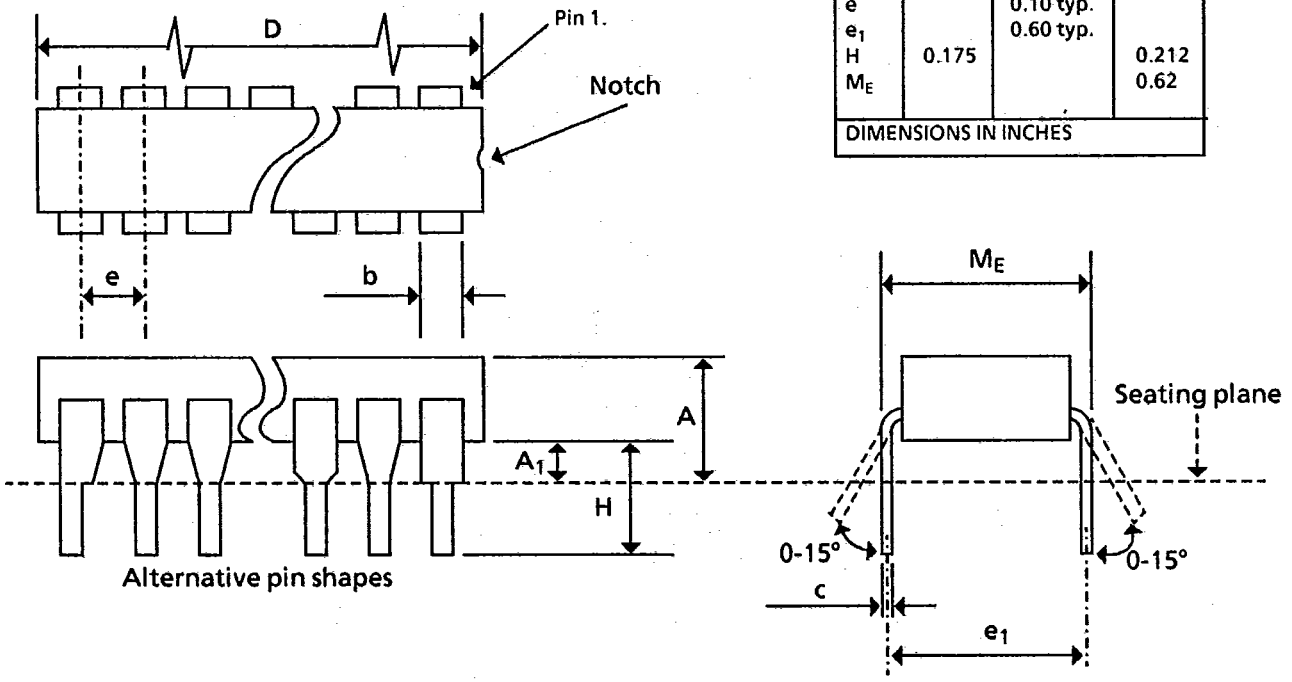
PACKAGE OUTLINES

28 Lead Ceramic DIL

Ref.	Min.	Nom.	Max.
A	0.105		0.145
A_1	0.025		0.045
b	0.047		0.053
c		0.01	
D	1.389		1.111
e		0.10 typ.	
e_1		0.60 typ.	
H	0.175		0.212
M_E			0.62

DIMENSIONS IN INCHES



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TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

RADIATION PERFORMANCE

Total Dose (Function to specification, note 1)	$1x10^6$ Rad(Si)
Total Dose (Function to specification, note 2)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$3x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm2
Latch-up	Not possible
Single Event Upset (note 3)	$<10^{-10}$ errors/bit day

Note 1: Circuits with all inputs 'CMOS' types.
Note 2: Circuits with 'TTL' type inputs.
Note 3:GSO 10% Worst Case

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ORDERING INFORMATION

Unique circuit designator.

MAx28151xxx

PACKAGE

- C Ceramic DIL
- F Flatpack
- L Leadless Chip Carrier
- N Naked Die

RADIATION TOLERANCE

- 'Blank' No tolerance implied
- S Radiation hard processing
- R 100 kRads (Si) guaranteed
- Q 300 kRads (Si) guaranteed
- H 1000 kRads (Si) guaranteed

QUALITY LEVEL

USA Standards (note 1)
- B1 Class B
- B9 Class B + SEM inspection and PIND screening
- S0 Class S without internal visual inspection by customer
- S2 Class S

ESA/SCC 9000 (note 2)
- T1 level B, Lat 1
- T2 level B, Lat 2
- T3 level B, Lat 3
- T4 level C, Lat 1
- T5 level C, Lat 2
- T6 level C, Lat 3

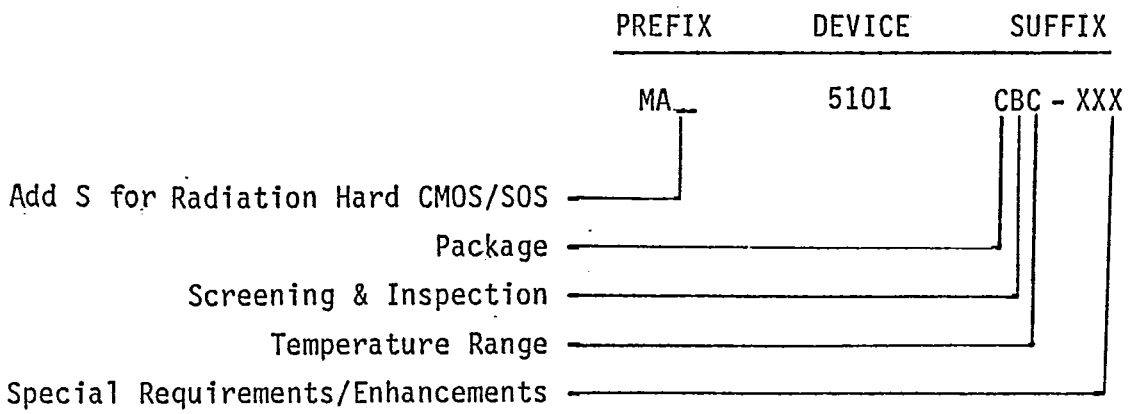
'Blank' No tolerance implied
S Radiation hard processing

- GB Commercial 0 to 70°C
- GC Commercial -55 to 125°C

1 Marconi Electronic Devices quality levels conform to MIL STD 883C class B/S, screening method 5004 and Quality Conformance Inspection method 5005 . This does not imply DESC certification, however MIL-M-38510 qualified product listing is being sought.

2 Marconi's specifications for European Space manufacturing flows, including their associated screening procedures, conform to ESA/SCC Generic Specification No.9000. A Process Identification Document, describing the manufacture of these devices, has been approved by the European Space Agency.

MARCONI ELECTRONIC DEVICES, INC



PACKAGE

A. Pin Grid Array
C. Ceramic DIL
E. Epic
F. Flat Pack
G. Cerdip
L. Leadless Chip Carrier
M. Module
N. Naked Die
P. Plastic DIL
Q. Quad Plastic J-Lead
R. Qual Cerpack J-Lead
S. SO Plastic
X. Special

TEMPERATURE RANGE

A. Special
B. 0 to 70°C
C. -55 to +125°C
D. -25 to +70°C
E. -25 to +85°C
F. -40 to +85°C
G. -55 to +85°C
H. -40 to +125°C
J. -10 to +80°C
K. 0 to +200°C

SCREENING & INSPECTION

B. Mil Std-883C Class B
G. Commercial Hermetic
L. Commercial Plastic
S. Mil Std-883C Class S
T. ESA9000
X. Special

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