1 Megabit (64K x 16) UV Erasable CMOS EPROM

Features

- **Fast Read Access Time - 45 ns**
- **Low Power CMOS Operation**
  - **100 µA max. Standby**
  - **30 mA max. Active at 5 MHz**
- **Wide Selection of JEDEC Standard Packages**
  - **40-Lead 600-mil PDIP and Cerdip**
  - **44-Pad PLCC and LCC**
  - **40-Lead TSOP**
- **5 V ± 10% Power Supply**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid Programming - 100 µs/word (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

Description

The AT27C1024 is a low-power, high performance 1,048,576 bit ultraviolet erasable and electrically programmable read only memory (EPROM) organized 64K x 16. It requires only one 5-V power supply in normal read mode operation. Any word can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states. The by-16 organization make this part ideal for high-performance 16 and 32 bit microprocessor systems.

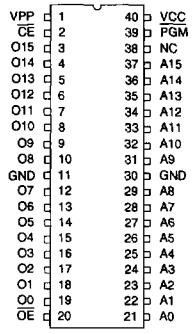
(continued)

Pin Configurations

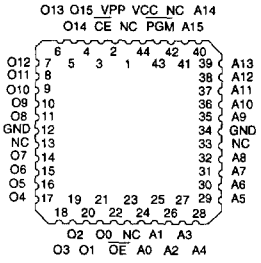
Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.

CDIP, PDIP Top View

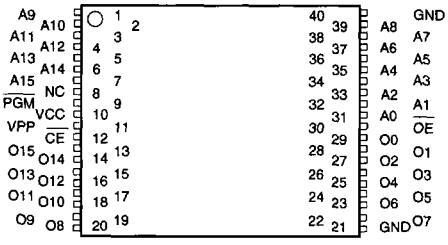


LCC, JLCC, PLCC Top View



Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

TSOP Top View
Type 1



Description Continued

In read mode, the AT27C1024 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C1024 is available in industry standard JEDEC-approved packages including: one time programmable (OTP) plastic PDIP, PLCC, and TSOP, as well as windowed ceramic Cerdip and LCC. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

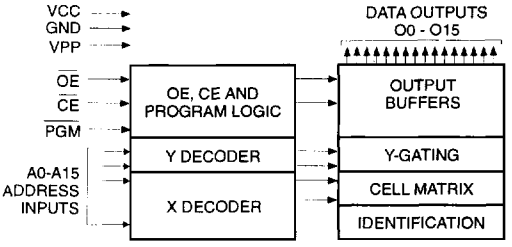
With high density 64K word storage capability, the AT27C1024 allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C1024 have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C1024 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

Notes:

1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes:

1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5$ V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C1024						
		-45	-55	-70	-85	-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.				-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

= Advance Information

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D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	Com., Ind.		±1	µA
			Mil.		±5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	Com., Ind.		±5	µA
			Mil.		±10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC}+0.5 V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind., Mil.		40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+ 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

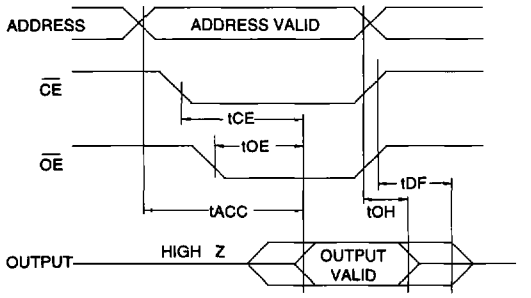
A.C. Characteristics for Read Operation

				AT27C1024												
				-45		-55		-70		-85		-10		-12		-15		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com., Ind.		45		55		70		85		100		120		150	ns
			Mil.								85		100		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			45		55		70		85		100		120		150	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			20		25		25		30		30		35		50	ns
t_{DF} (4,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float				20		25		25		30		30		30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first			7		7		7		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

= Advance Information

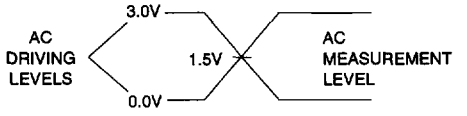
A.C. Waveforms for Read Operation [1]



Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified. Timing measurement reference is 1.5 V for -45, -55 and -70 parts. Input AC driving levels are 0.0 V and 3.0 V for -45, -55 and -70 parts, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

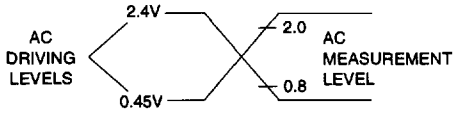
Input Test Waveforms and Measurement Levels

For -45, -55, and -70 Devices Only:



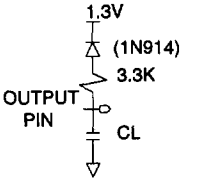
t_R, t_F < 5 ns (10% to 90%)

For -85, -10, -12, -15 Devices Only:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



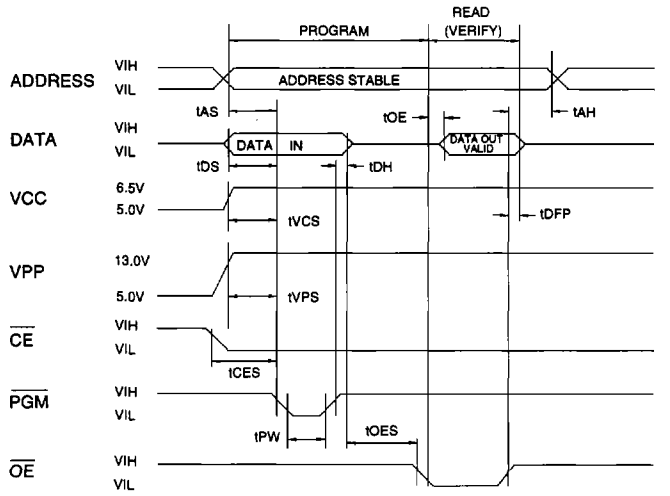
Note: C_L = 100 pF including jig capacitance except -45, -55 and -70 devices, where C_L = 30 pF.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C1024 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+0.1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C1024 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

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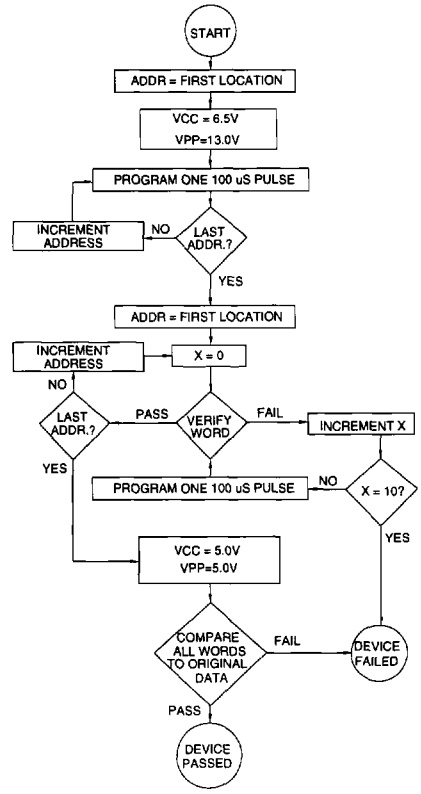
Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

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t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	30	0.1	AT27C1024-45DC AT27C1024-45JC AT27C1024-45LC AT27C1024-45PC AT27C1024-45TC	40DW6 44J 44LW 40P6 40T	Commercial (0°C to 70°C)
45	40	0.1	AT27C1024-45DI AT27C1024-45JI AT27C1024-45LI AT27C1024-45PI AT27C1024-45TI	40DW6 44J 44LW 40P6 40T	Industrial (-40°C to 85°C)
55	30	0.1	AT27C1024-55DC AT27C1024-55JC AT27C1024-55LC AT27C1024-55PC AT27C1024-55TC	40DW6 44J 44LW 40P6 40T	Commercial (0°C to 70°C)
55	40	0.1	AT27C1024-55DI AT27C1024-55JI AT27C1024-55LI AT27C1024-55PI AT27C1024-55TI	40DW6 44J 44LW 40P6 40T	Industrial (-40°C to 85°C)
70	30	0.1	AT27C1024-70DC AT27C1024-70JC AT27C1024-70LC AT27C1024-70PC AT27C1024-70TC	40DW6 44J 44LW 40P6 40T	Commercial (0°C to 70°C)
70	40	0.1	AT27C1024-70DI AT27C1024-70JI AT27C1024-70LI AT27C1024-70PI AT27C1024-70TI	40DW6 44J 44LW 40P6 40T	Industrial (-40°C to 85°C)
85	30	0.1	AT27C1024-85DC AT27C1024-85JC AT27C1024-85LC AT27C1024-85PC AT27C1024-85TC	40DW6 44J 44LW 40P6 40T	Commercial (0°C to 70°C)
85	40	0.1	AT27C1024-85DI AT27C1024-85JI AT27C1024-85LI AT27C1024-85PI AT27C1024-85TI	40DW6 44J 44LW 40P6 40T	Industrial (-40°C to 85°C)
			AT27C1024-85DM AT27C1024-85KM AT27C1024-85LM	40DW6 44KW 44LW	Military (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	30	0.1	AT27C1024-10DC AT27C1024-10JC AT27C1024-10KC AT27C1024-10LC AT27C1024-10PC AT27C1024-10TC	40DW6 44J 44KW 44LW 40P6 40T	Commercial (0°C to 70°C)
100	40	0.1	AT27C1024-10DI AT27C1024-10JI AT27C1024-10KI AT27C1024-10LI AT27C1024-10PI AT27C1024-10TI	40DW6 44J 44KW 44LW 40P6 40T	Industrial (-40°C to 85°C)
			AT27C1024-10DM AT27C1024-10KM AT27C1024-10LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
120	30	0.1	AT27C1024-12DC AT27C1024-12JC AT27C1024-12KC AT27C1024-12LC AT27C1024-12PC AT27C1024-12TC	40DW6 44J 44KW 44LW 40P6 40T	Commercial (0°C to 70°C)
120	40	0.1	AT27C1024-12DI AT27C1024-12JI AT27C1024-12KI AT27C1024-12LI AT27C1024-12PI AT27C1024-12TI	40DW6 44J 44KW 44LW 40P6 40T	Industrial (-40°C to 85°C)
			AT27C1024-12DM AT27C1024-12KM AT27C1024-12LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-12DM/883 AT27C1024-12KM/883 AT27C1024-12LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	30	0.1	AT27C1024-15DC AT27C1024-15JC AT27C1024-15KC AT27C1024-15LC AT27C1024-15PC AT27C1024-15TC	40DW6 44J 44KW 44LW 40P6 40T	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT27C1024-15DI AT27C1024-15JI AT27C1024-15KI AT27C1024-15LI AT27C1024-15PI AT27C1024-15TI	40DW6 44J 44KW 44LW 40P6 40T	Industrial (-40°C to 85°C)
			AT27C1024-15DM AT27C1024-15KM AT27C1024-15LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-15DM/883 AT27C1024-15KM/883 AT27C1024-15LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	40	0.1	5962-86805 07 QX 5962-86805 07 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	40	0.1	5962-86805 06 QX 5962-86805 06 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	40	0.1	5962-86805 05 QX 5962-86805 05 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	40	0.1	5962-86805 04 QX 5962-86805 04 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	40	0.1	5962-86805 03 QX 5962-86805 03 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	40	0.1	5962-86805 02 QX 5962-86805 02 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	40	0.1	5962-86805 01 QX 5962-86805 01 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
40T	40 Lead, Plastic Thin Small Outline Package OTP (TSOP)