FAIRCHILD
A Schlumberger Company

μA5116
μ255-Law Companding Codec

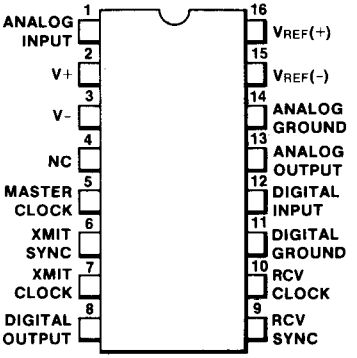
Telecommunication Products

Description

The 5116 is a monolithic CMOS Companding Codec containing both an analog-to-digital converter and a digital-to-analog converter which have transfer characteristics conforming to the μ255-Law companding code. This device performs a coder-decoder function designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in PCM systems. Digital input and output are in serial format using sign-plus-magnitude coding. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64 kb/s to 2.1 Mb/s rate with analog signal sampling occurring at an 8 kHz rate. A SYNC pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.

- **EXCEEDS D3 CHANNEL BANK SPECIFICATIONS**
- **LOW POWER DISSIPATION 30 mW TYPICAL**
- **SYNCHRONOUS/ASYNCHRONOUS OPERATION**
- **ON-CHIP S/H CIRCUIT**
- **ON-CHIP OFFSET NULL CIRCUIT**
- **SEPARATE ANALOG AND DIGITAL GROUNDS**
- **64 kb/s to 2.1 Mb/s SERIAL DATA RATE**
- **±5V POWER SUPPLY OPERATION**

Connection Diagram
16-Pin DIP

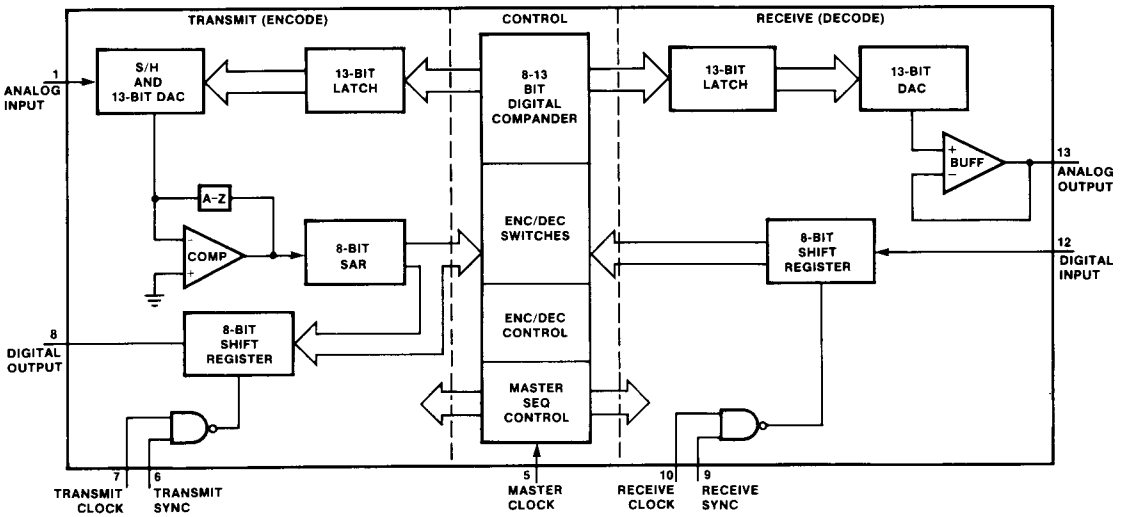


(Top View)

Order Information

Type	Package	Code	Part No.
μA5116	Ceramic DIP	FW	μA5116 DC
μA5116	Ceramic DIP (Side Brazed)	FB	μA5116 JC

Block Diagram



Pin 4 = not connected

8

Absolute Maximum Ratings (Note)

Supply Voltage (V+)	+6
Supply Voltage (V−)	−6
Analog Input Range	$V- \leq V_{IN} \leq V+$
Digital Input Range	$-0.5\ V \leq V_{IN} \leq V+$
Reference Voltage $V_{REF}(+)$	$-0.5\ V \leq V_{REF}(+) \leq V+$
Reference Voltage $V_{REF}(-)$	$V- \leq V_{REF}(-) \leq 0.5\ V$
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

Note
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

Functional Description (Refer to Block Diagram)

Positive and Negative Reference Voltages, ($V_{REF}(+)$ and $V_{REF}(-)$ Pins 16 and 15)
These inputs provide the conversion references for the digital-to-analog converters in the 5116. $V_{REF}(+)$ and $V_{REF}(-)$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

Analog Input, Pin 1
Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to *Figure 6*). The Analog Input must remain between $V_{REF}(+)$ and $V_{REF}(-)$ for accurate conversion.

Master Clock, Pin 5
This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV Clock, XMIT SYNC or XMIT Clock and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to *Figure 2* for the Timing Diagram)
This input is synchronized with XMIT Clock. When XMIT SYNC goes HIGH, the Digital Output is activated and the A/D conversion begins on the next positive edge of Master Clock. The conversion by Master Clock can be asynchronous with XMIT Clock. The serial output data is clocked out by the positive edges of XMIT Clock. The negative edge of XMIT SYNC causes the Digital Output to become 3-state. XMIT SYNC must go LOW for at least 1 Master Clock prior to the transmission of the next digital word. (Refer to *Figure 10.*)

XMIT Clock, Pin 7 (Refer to *Figure 2* for the Timing Diagram)
The on-chip 8-bit output shift register of the 5116 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for XMIT Clock. The positive edge of the internal clock transfers the data from the master to the slave of a master-slave flip-flop (refer to *Figure 7*). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT Clock, XMIT SYNC will determine when the first positive edge of the internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV SYNC, Pin 9 (Refer to *Figure 3* for the Timing Diagram)
This input is synchronized with RCV Clock, and serial data is clocked in by RCV Clock. Duration of the RCV SYNC pulse is approximately eight RCV Clock periods. The conversion from digital-to-analog starts after the negative edge of RCV SYNC pulse (refer to *Figure 6*). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay LOW for 17 Master Clocks (minimum) before the next digital word is to be received (Refer to *Figure 11*).

RCV Clock, Pin 10 (Refer to *Figure 3* for Timing Diagram)
The on-chip 8-bit shift register for the 5116 is loaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for RCV Clock. Valid data should be applied to the digital input before the positive edge of the internal clock (refer to *Figure 7).* This set-up time, t_{rds}, allows the data to be transferred into the Master of a master-slave flip-flop. The positive edge of the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{rdh}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV Clock, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

Digital Output, Pin 8
The 5116 output register stores the 8-bit encoded sample of the Analog Input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT Clock. When XMIT SYNC is LOW, the Digital Output is an open circuit. When XMIT SYNC is HIGH, the state of the Digital Output is determined by the value of the output bit in the serial shift register. The output is composed of a sign bit, 3 chord bits, and 4 step bits.

The sign bit indicates the polarity of the Analog Input while the chord and step bits indicate the magnitude. In the first chord, the step bit has a value of 0.6 mV. In the second chord, the step bit has a value of 1.2 mV. This doubling of the step value continues for each of the next six successive chords.

Each chord has a specific value and the step bits, 16 in each chord, specify the displacement from that value (refer to *Table 1*. Thus the output, which follows the μ255-Law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit a/d converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the a/d converter (μ255-Law Encoder) is shown in *Figure 8*.

Digital Input, Pin 12
The 5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV Clock. The timing diagram is shown in *Figure 3*. When RCV SYNC goes HIGH, the 5116 uses RCV Clock to clock the serial data into its input register. RCV SYNC goes LOW to indicate the end of serial input data. The eight bits of the input data have the same functions described for the Digital Output. The transfer characteristic of the d/a converter (μ255-Law Decoder) is shown in *Figure 9*.

Analog Output, Pin 13
The Analog Output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with (sin x)/x correction to recreate the sampled voice signal.

Operation of Codec With 64 kHz XMIT/RCV Clock Frequencies
XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for one Master Clock period (minimum) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 Master Clock periods (minimum) before the next digital word is received (refer to *Figures 10* and *11*).

Offset Null
The offset null feature of the 5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate a/d conversion for inputs near ground. There is no offset adjust of the output amplifier since the output is intended to be ac-coupled to the external filter and the resultant dc error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the Analog Input. Therefore, for an Analog Input of 0 V, the sign bit will be stable.

Table 1 Digital Output Code for 5116

	Chord Code	Chord Value	Step Value
1.	000	0.0 mV	0.613 mV
2.	001	10.11 mV	1.226 mV
3.	010	30.3 mV	2.45 mV
4.	011	70.8 mV	4.90 mV
5.	100	151.7 mV	9.81 mV
6.	101	313 mV	19.61 mV
7.	110	637 mV	39.2 mV
8.	111	1.284 V	78.4 mV

Example:

1	011	0010 = +70.8 mV + (2 x 4.90 mV)
Sign Bit	Chord	Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

8

Electrical Operating Characteristics

Power Supply Requirements

Symbol	Characteristic	Min	Typ	Max	Unit
V+	Positive Supply Voltage	4.75	5.0	5.25	V
V−	Negative Supply Voltage	−5.25	−5.0	−4.75	V
$V_{REF}(+)$	Positive Reference Voltage (Note 1)	2.375	2.5	2.625	V
$V_{REF}(-)$	Negative Reference Voltage (Note 1)	−2.625	−2.5	−2.375	V

DC Characteristics V+ = 5 V, V− = −5 V, $V_{REF}(+)$ = 2.5 V, V_{REF} (−) = −2.5 V.

Symbol	Characteristic	Min	Typ	Max	Unit
R_{INAS}	Analog Input Resistance During Sampling (Note 2)		2		kΩ
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ
C_{INA}	Analog Input Capacitance		150	250	pF
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	±8	mV
R_{OUTA}	Analog Output Resistance		20	50	Ω
I_{OUTA}	Analog Output Current	0.25	0.5		mA
$V_{OFFSET/O}$	Analog Output Offset Voltage		±200	±850	mV
I_{IL}	Logic Input LOW Current (V_{IN} = 0.8 V) Digital Input, Clock Input, SYNC Input (Note 3)		±0.1	±10	μA
I_{IH}	Logic Input HIGH Current (V_{IN} = 2.4 V) Digital Input, Clock Input, SYNC Input (Note 3)		−0.25	−0.8	mA
C_{DO}	Digital Output Capacitance		8	12	pF
I_{DOL}	Digital Output Leakage Current		±0.1	±10	μA
V_{OL}	Digital Output LOW Voltage (Note 4)			0.4	V
V_{OH}	Digital Output HIGH Voltage (Note 4)	3.9			V
I+	Positive Supply Current		4	10	mA
I−	Negative Supply Current		2	6	mA
I_{REF+}	Positive Reference Current		4	20	μA
I_{REF-}	Negative Reference Current		4	20	μA

AC Characteristics Refer to *Figures 2* and *3.*

Symbol	Characteristic	Min	Typ	Max	Unit
f_m	Master Clock Frequency	1.5	1.544	2.1	MHz
f_r, f_x	RCV, XMIT Clock Frequency	0.064	1.544	2.1	MHz
PW_{clk}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns
t_{rc}, t_{fc}	Clock Rise, Fall Time (MASTER, XMIT, RCV			25% of PW_{clk}	ns
t_{rs}, t_{fs}	SYNC Rise, Fall Time (XMIT, RCV)			25% of PW_{clk}	ns
t_{Dlr}, t_{Dlf}	Data Input Rise, Fall Time			25% of PW_{clk}	ns
t_{wsx}, t_{wsr}	SYNC Pulse Width (XMIT,RCV)		$\frac{8}{f_x(f_r)}$		μs
t_{ps}	SYNC Pulse Period (XMIT,RCV)		125		μs
t_{xcs}	XMIT Clock-to-XMIT SYNC Delay (Note 5)	50% of $t_{fc}(t_{rs})$			ns
t_{xcsn}	XMIT Clock-to-XMIT SYNC (Negative Edge) Delay	200			ns
t_{xss}	XMIT SYNC Set-Up Time	200			ns
t_{xdd}	XMIT Data Delay (Note 4)	0		200	ns
t_{xdp}	XMIT DATA Present (Note 4)	0		200	ns
t_{xdt}	XMIT Data Three State (Note 4)			150	ns
t_{dof}	Digital Output Fall Time (Note 4)		50		ns
t_{dor}	Digital Output Rise Time (Note 4)		50		ns
t_{src}	RCV SYNC-to-RCV Clock Delay (Note 5)	50% $t_{rc}(t_{fs})$			ns
t_{rds}	RCV Data Set-Up Time (Note 6)	50			ns
t_{rdh}	RCV Data Hold Time (Note 6)	200			ns
t_{rcs}	RCV Clock-to-RCV SYNC Delay	200			ns
t_{rss}	RCV SYNC Set-Up Time (Note 6)	200			ns
t_{sao}	RCV SYNC-to-Analog Output Delay		7		μs
Slew+	Analog Output Positive Slew Rate		1		V/μs
Slew−	Analog Output Negative Slew Rate		1		V/μs
Droop	Analog Output Droop Rate		25		μV/μs

8

Notes

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging the internal capacitor to within 1/2 LSB (≤ 300 μV) in 20 μs. Therefore, the external source resistance must be 3 kΩ or less. The equivalent circuit during sampling is shown in *Figure 1.*
3. The 5116 will source current through an internal 6 kΩ resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with $I_{OH} = -100$ μA, $I_{OL} = 500$ μA.
5. This delay is necessary to avoid overlapping Clock and SYNC.
6. The first bit of data is loaded when SYNC and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

System Characteristics Refer to *Figures 4* and *5*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
S/D	Signal-to-Distortion	35 29 24	39 34 29		dB dB dB	Analog Input = 0 to −30 dBmO Analog Input = −40 dBmO Analog Input = −45 dBmO
GT	Gain Tracking		±0.1 ±0.1 ±0.2	±0.4 ±0.8 ±2.5	dB dB dB	Analog Input = +3 to −37 dBmO Analog Input = −37 to −50 dBmO Analog Input = −50 to −55 dBmO
N_{IC}	Idle Channel Noise		10	18	dBrnC0	Analog Input = 0 V
TLP	Transmission Level Point		+4		dB	600 Ω

Fig. 1 Equivalent Circuit During Sampling

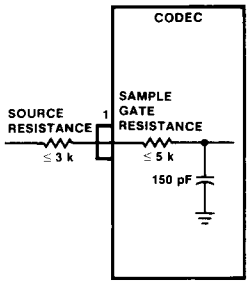
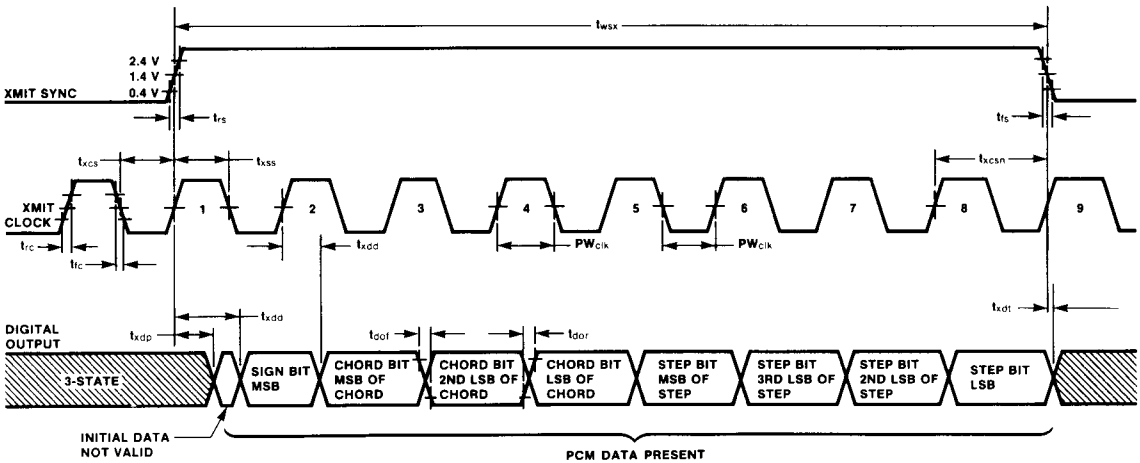


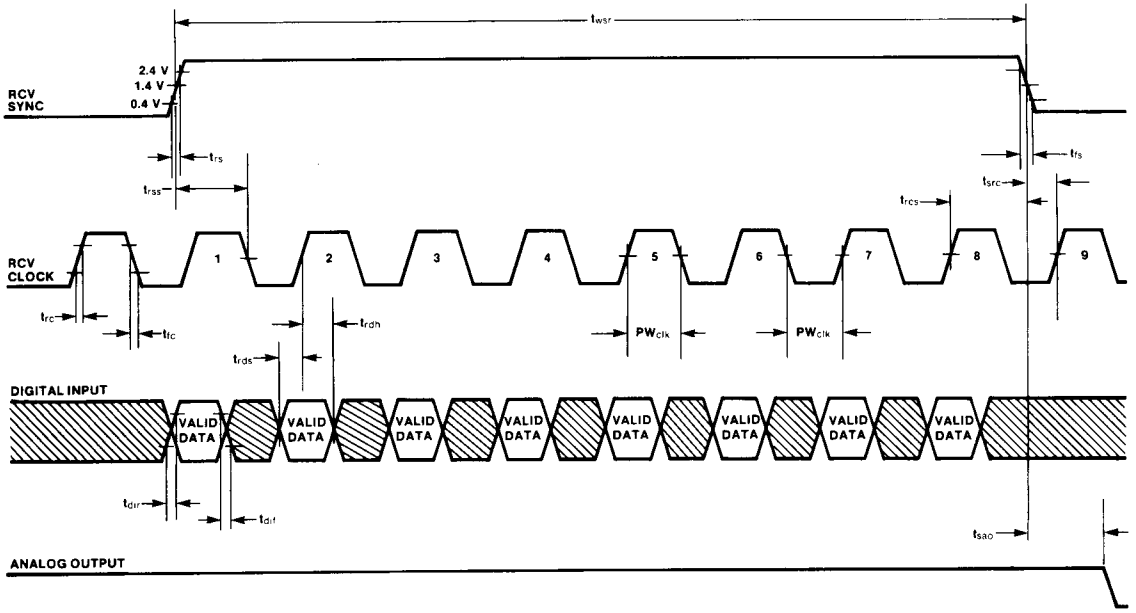
Fig. 2 Transmitter Section Timing



Note

All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Fig. 3 Receiver Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Fig. 4 S/D Ratio vs Input Level

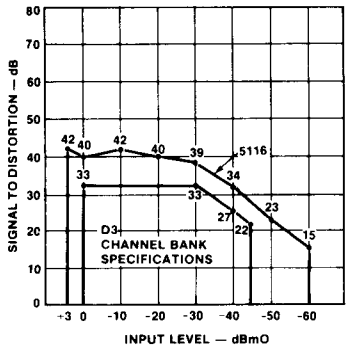


Fig. 5 Gain Tracking Performance

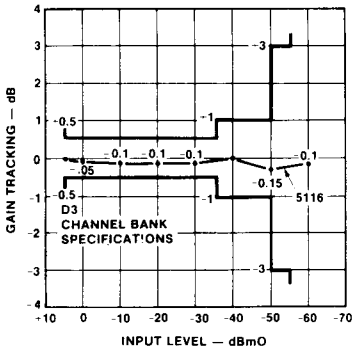


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Fig. 6 A/D, D/A Conversion Timing

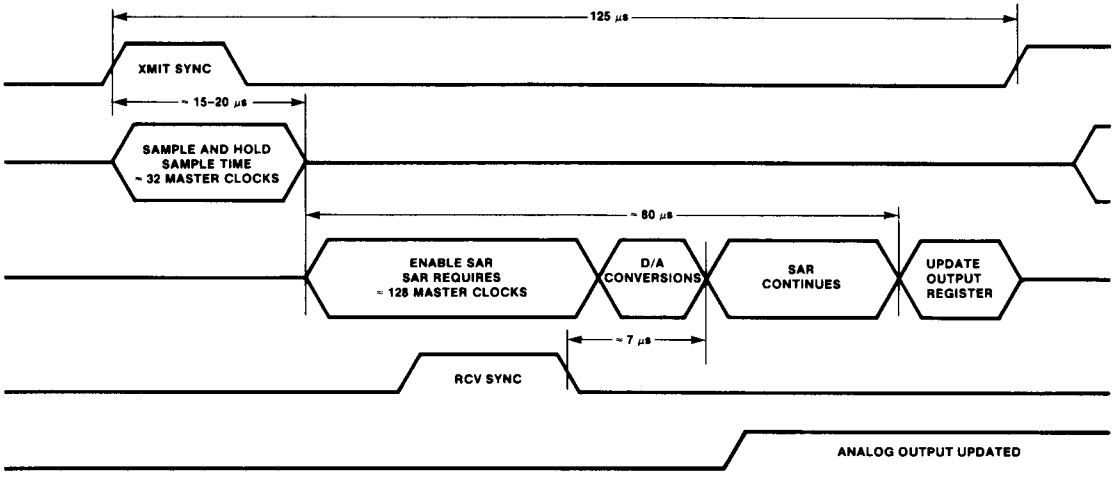
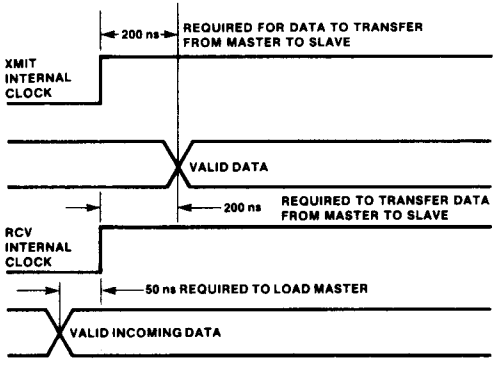


Fig. 7 Data Input/Output Timing



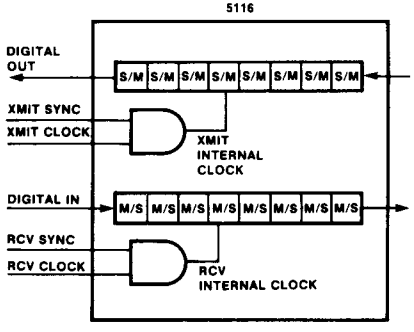


Fig. 8 A/D Converter (μ255-Law Encoder) Transfer Characteristic for 5116

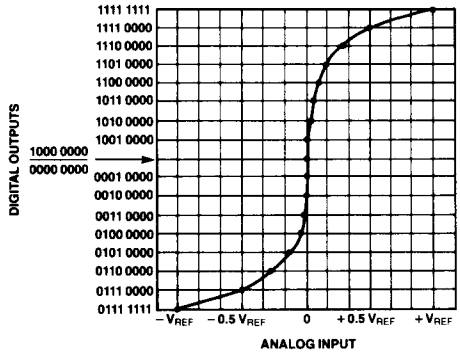


Fig. 9 D/A Converter (μ255-Law Decoder) Transfer Characteristic for 5116

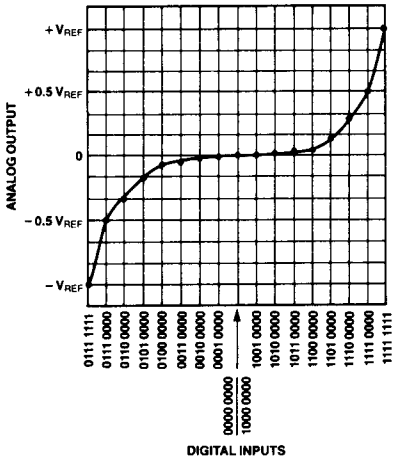
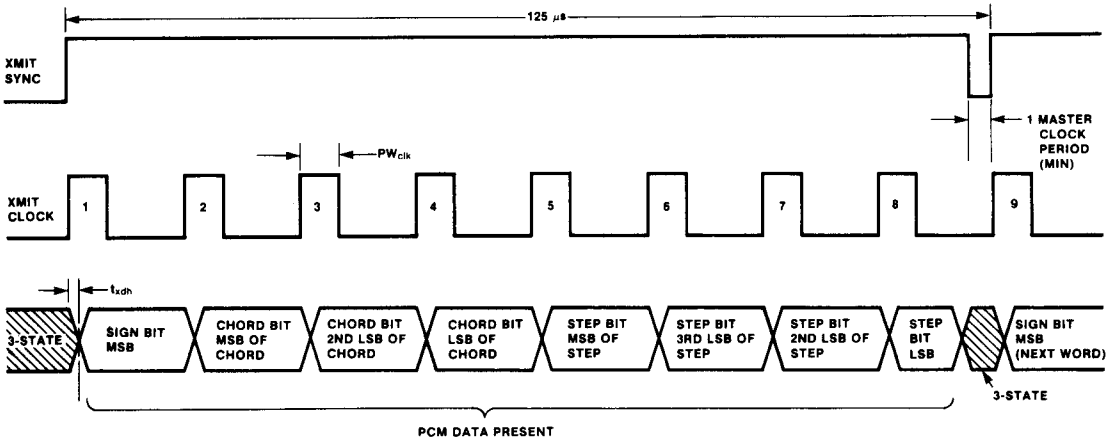


Fig. 10 64 kHz Operation, Transmitter Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

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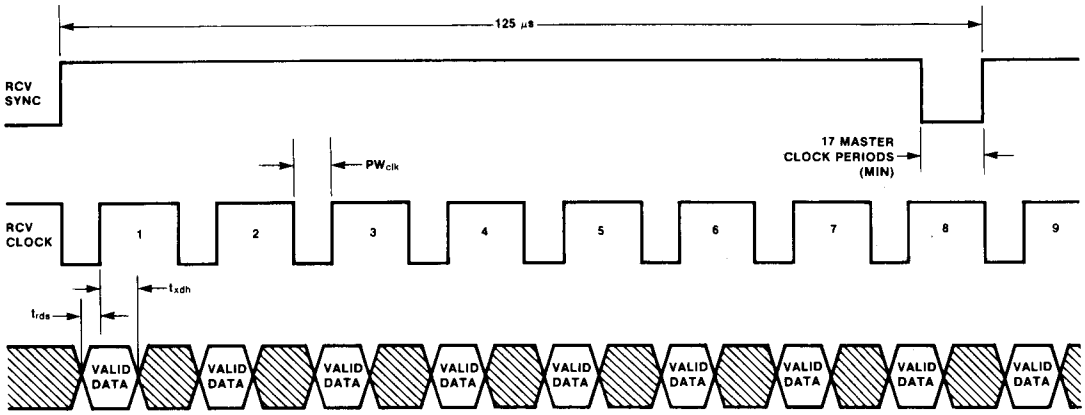
Fig. 11 64 kHz Operation, Receiver Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

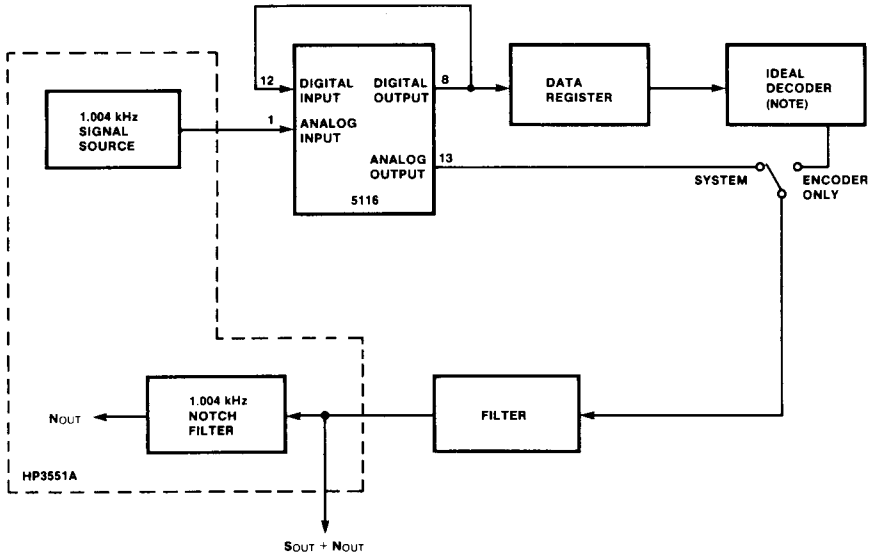
Performance Evaluation
The equipment connections shown in *Figure 12* can be used to evaluate the performance of the 5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the 5116. The Digital Output of the codec is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the 5116 are connected as follows:

1. RCV SYNC is tied to XMIT SYNC.
2. XMIT Clock is tied to Master Clock. The signal is inverted and tied to RCV Clock.

The following timing signals are required:
1. Master Clock = 2.048 MHz
2. XMIT SYNC repetition rate = 8 kHz
3. XMIT SYNC width = 8 XMIT Clock periods

When all the above requirements are met, the set-up of *Figure 12* permits the measurement of synchronous system performance over a wide range of Analog Inputs. The data register and ideal decoder provide a means of checking the encoder portion of the 5116 independently of the decoder section. To test the system in the asynchronous mode, Master Clock should be separated from XMIT Clock, and Master Clock should be separated from RCV Clock. XMIT Clock and RCV Clock are separated also.

Fig. 12 System Characteristics Test Configuration



Note

The ideal decoder consists of a digital decompander and a 13-bit precision DAC.