Data Sheet
March 1996

AT&T Microelectronics

T7234 Single-Chip NT1 (SCNTI) Euro-LITE Transceiver

Features

- U- to S/T-interface conversion for ISDN basic rate (2B+D) systems
  - — Integrated U- and S/T-interfaces
  - — Operates in stand-alone mode to provide U- and S/T-interface activation, control, and maintenance functions
  - — Automatic embedded operations channel (eoc) processing for ANSI T1.601 systems
  - — Low power consumption (270 mW typical) supporting line-powered NT1
  - — Idle mode support (35 mW typical)
  - — Board-level testability support
- U-interface
  - — Conforms to ANSI T1.601 standard and ETSI DTR/TM 3002 technical report
  - — 2B1Q four-level line code
  - — Automatic ANSI maintenance functions (quiet mode and insertion loss mode)
- S/T-interface
  - — Conforms to ANSI T1.605 standard, ITU-T (formerly CCITT) I.430 recommendation, and ETSI ETS 300 012 for NT operation
- Other
  - — 0.9 µm linear CMOS technology
  - — Single +5 V (±5%) supply
  - — –40 °C to +85 °C
  - — 44-pin PLCC

Description

The AT&T T7234 Single-Chip NT1 (SCNT1) Transceiver integrated circuit provides data (2B+D) and control information conversion between 2-wire (U-interface) and 4-wire (S/T-interface) digital subscriber loops on the integrated services digital network (ISDN). The T7234 conforms to the ANSI T1.601 standard and ETSI DTR/TM 3002 technical report for the U-interface and the ITU-T I.430 recommendation, ANSI T1.605 standard, and ETSI ETS 300 012 for the S/T-interface. The T7234 also supports digital pair gain and terminal adapter applications. The single +5 V CMOS device is packaged in a 44-pin, plastic, leaded chip carrier (PLCC).

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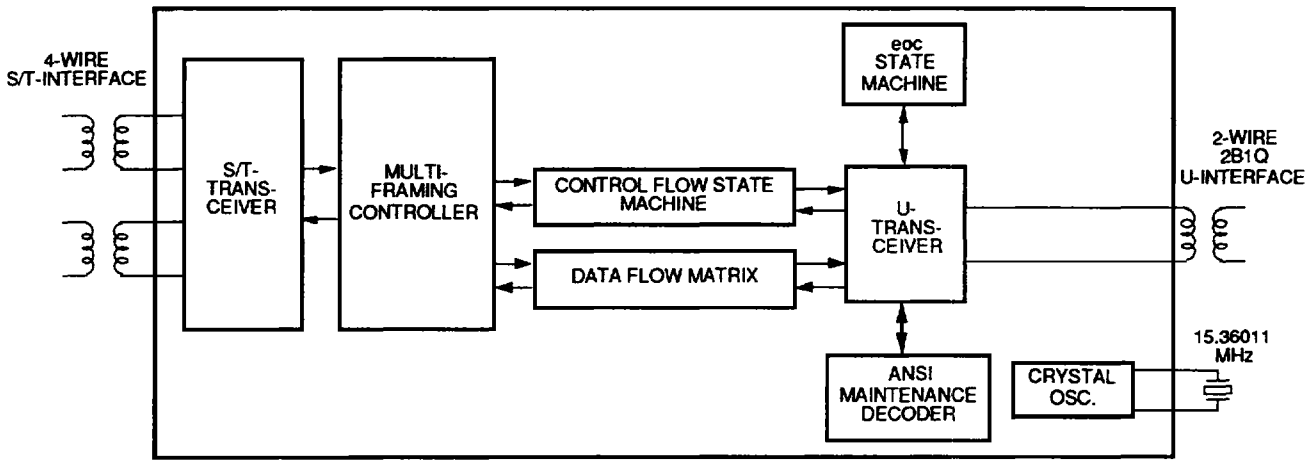
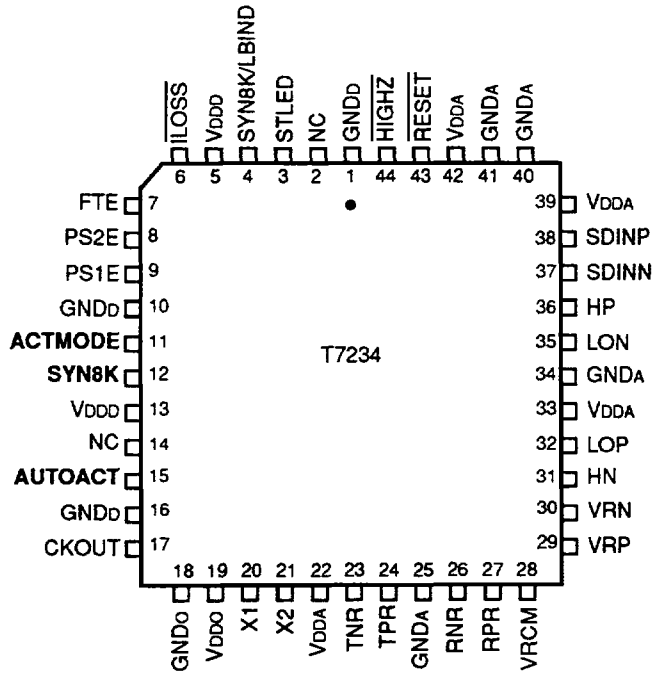


Figure 1. Block Diagram

Pin Information



Note: Controls shown in bold (pins 11, 12, and 15) are configured by the state of these pins when exiting xto(RESET).

Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type*	Name/Function
1, 10, 16	GND_D	—	**Digital Ground.** Ground leads for digital circuitry.
2	NC	—	No Connect.
3	STLED	O	**Status LED Driver.** Output pin for driving an LED (source/sink 4.0 mA) that indicates the device status. The four defined states are low, high, 1 Hz flashing, and 8 Hz flashing (flashing occurs at 50% duty cycle). See the STLED Description section for a detailed explanation of these states. Also, this pin indicates device sanity upon poweron/RESET, as follows: ■ If SCK = 0 (pin 15) after a device RESET (which sets AUTOACT = 0 in register GR0 bit 6, turning on autoactivation), STLED will toggle at an 8 Hz rate for at least 0.5 s, signifying an activation attempt. If the activation attempt succeeds, it will continue to flash per the normal start-up sequence (see STLED Description section). ■ If SCK = 1 (pin 15) after a device RESET, STLED will go low for 1 s ("flash of life"), indicating that the device is operational, and no activation attempt will be made.
4	SYN8K/LBIND	O	**Synchronous 8 kHz Clock or Loopback Indicator.** Pin function is selected via SDI pin state at end of external RESET. As SYN8K, this pin can be used as a reference clock or for synchronization in device performance testing (i.e., it reflects the recovered timing from the U-interface). As LBIND, this pin indicates a 2B+D loopback: 0 — No loopback. 1 — eoc requested 2B+D loopback in progress.
5, 13	V_{DDD}	—	**Digital Power.** 5 V ± 5% power supply pins for digital circuitry.

* I^U = input with internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
6	$\overline{\text{ILOSS}}$	I^u	**Insertion Loss Test Control (Active-Low).** The $\overline{\text{ILOSS}}$ pin is used to control SN1 tone transmission for maintenance. This pin would typically be used if an external ANSI maintenance decoder is being used, in which case the decoder output drives the $\overline{\text{ILOSS}}$ pin. The $\overline{\text{ILOSS}}$ pin is ignored, and the functionality is controlled by the ILOSS bit (register CFR0, bit 0) if AUTOCTL = 0 (register GR0, bit 3). Internal 100 kΩ pull-up resistor on this pin. 0 — U transmitter sends SN1 tone continuously. 1 — No effect on device operation.
7	FTE	I^u	**Fixed/Adaptive Timing Mode Select.** Selects S/T-interface timing recovery mode: 0 — Fixed timing recovery mode. 1 — Adaptive timing recovery mode.
8	PS2E	I^d	**Power Status #2.** See PS2 bit description (register GR1, bit 1) for PS1 and PS2 message definition. If the PS2E functionality is not used, this input must be pulled up externally with a 10 kΩ or less resistor to set the U-interface PS2 bit to the inactive state. An internal 100 kΩ pull-down resistor is on this pin.
9	PS1E	I^d	**Power Status #1.** See PS2 bit description (register GR1 bit 1) for PS1 and PS2 message definition. If the PS1E functionality is not used, this input must be pulled up externally with a 10 kΩ or less resistor to set the U-interface PS1 bit to the inactive state. An internal 100 kΩ pull-down resistor is on this pin.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
11	ACTMODE	I^U	**ACT Bit Mode.** Upon exiting $\overline{\text{RESET}}$, the state of $\overline{\text{INT}}$ is read and if $\overline{\text{INT}}$ = 1 (default), bit ACTSEL = 1 (register GR2, bit 6). If $\overline{\text{INT}}$ = 0 (externally pulled down), then ACTSEL = 0. An internal 100 kΩ pull-up resistor is on this pin.
12	SYN8K	I^d	**Synchronous 8 kHz Clock.** If pin is held low during an external $\overline{\text{RESET}}$, the SYN8K/LBIND/FS pin performs the SYN8K function. If held high during an external $\overline{\text{RESET}}$, the pin performs the LBIND function. An internal 100 kΩ pull-down resistor is on this pin.
14	NC	—	**No Connect.**
15	AUTOACT	I^d	**Automatic Activation.** If pin is held low during an external $\overline{\text{RESET}}$, the AUTOACT bit is written to 0, creating an activation attempt (see AUTOACT [register GR0, bit 6] description in Table 6). If pin is held high during external $\overline{\text{RESET}}$, no activation is attempted. An internal 100 kΩ pull-down resistor is on this pin.
17	CKOUT	O	**Clock Output.** Clock output function to drive other board components. Powerup default state is high-impedance to minimize power consumption. Programmable via microprocessor register (register GR0, bits 1 and 2) to provide 15.36011 MHz output or 10.24 MHz output. If U-interface is active, the 10.24 MHz output is synchronous with U-interface timing.
18	GND_O	—	**Crystal Oscillator Ground.** Ground lead for crystal oscillator.
19	V_{DDO}	—	**Crystal Oscillator Power.** Power supply lead for crystal oscillator.
20	X1	I	**Crystal #1.** Crystal connection #1 for 15.36011 MHz oscillator.
21	X2	I	**Crystal #2.** Crystal connection #2 for 15.36011 MHz oscillator.
22, 33, 39, 42	V_{DDA}	—	**Analog Power.** 5 V ± 5% power supply leads for analog circuitry.
23	TNR	O	**Transmit Negative Rail for S/T-Interface.** Negative output of S/T-interface analog transmitter. Connect to transformer through a 121 Ω ± 1% resistor.
24	TPR	O	**Transmit Positive Rail for S/T-Interface.** Positive output of S/T-interface analog transmitter. Connect to transformer through a 121 Ω ± 1% resistor.

* I^U = input with internal pull-up; I^d = input with internal pull-down.

Pin Information (continued)

Table 1. Pin Description (continued)

Pin	Symbol	Type*	Name/Function
25, 34, 40, 41	GND_A	—	**Analog Ground.** Ground leads for analog circuitry.
26	RNR	I	**Receive Negative Rail for S/T-Interface.** Negative input of S/T-interface analog receiver. Connect to transformer through a 10 kΩ ± 10% resistor.
27	RPR	I	**Receive Positive Rail for S/T-Interface.** Positive input of S/T-interface analog receiver. Connect to transformer through a 10 kΩ ± 10% resistor.
28	VRCM	—	**Common-Mode Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
29	VRP	—	**Positive Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
30	VRN	—	**Negative Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
31	HN	I	**Hybrid Negative Input for U-Interface.** Connect directly to negative side of U-interface transformer.
32	LOP	O	**Line Driver Positive Output for U-Interface.** Connect to the U-interface transformer through a 16.9 Ω ± 1% resistor.
35	LON	O	**Line Driver Negative Output for U-Interface.** Connect to the U-interface transformer through a 16.9 Ω ± 1% resistor.
36	HP	I	**Hybrid Positive Input for U-Interface.** Connect directly to positive side of U-interface transformer.
37	SDINN	I	**Sigma Delta A/D Negative Input for U-Interface.** Connect via an 820 pF ± 5% capacitor to SDINP.
38	SDINP	I	**Sigma Delta A/D Positive Input for U-Interface.** Connect via an 820 pF ± 5% capacitor to SDINN.
43	$\overline{RESET}$	I^d	**Reset (Active-Low).** Asynchronous Schmitt trigger input. Reset halts data transmission, clears adaptive filter coefficients, resets the U-transceiver timing recovery circuitry, resets the S/T-interface transceiver, and sets all microprocessor register bits to their default state. During reset, the U-interface transmitter produces 0 V and the output impedance is 135 Ω at tip and ring. The $\overline{RESET}$ pin can be used to implement quiet mode maintenance testing (refer to pin 2 description). The states of SCK, SDI, and $\overline{INT}$ are read upon exiting reset state. See SCK, SDI, and $\overline{INT}$ pin descriptions. An internal 100 kΩ pull-down resistor is on this pin. $\overline{RESET}$ must be held low for 1.5 ms after power on. Device is fully functional after an additional 1 ms.
44	$\overline{HIGHZ}$	I^u	**High-Impedance Control (Active-Low).** Control of the high-impedance function. An internal 100 kΩ pull-up resistor is on this pin. **Note:** This pin does not tristate the analog outputs. 0 — All digital outputs enter high-impedance state. 1 — No effect on device operation.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Application Overview

The T7234 is intended for use in ISDN networks as part of a 2-wire to 4-wire converter (NT1).

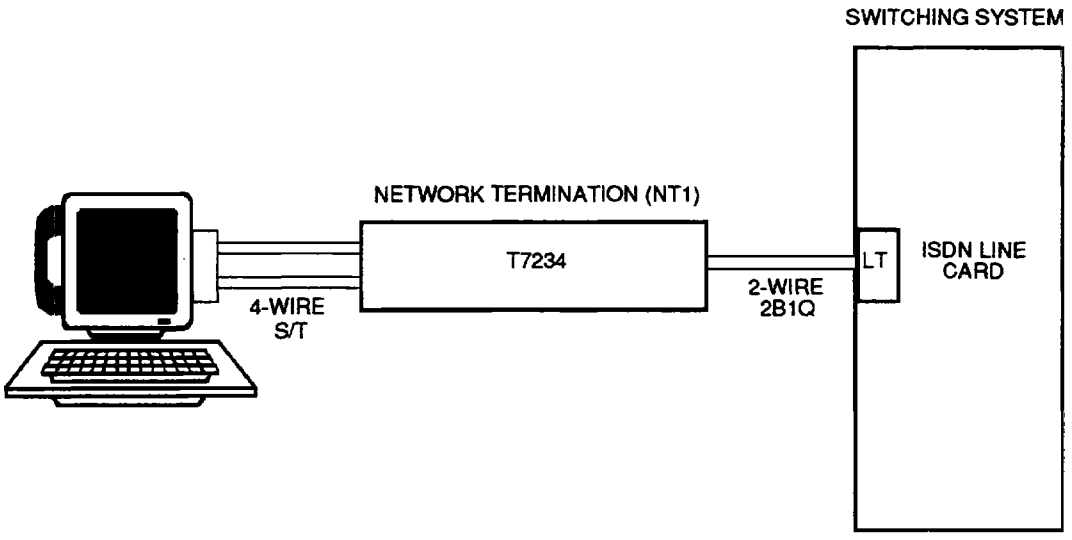


Figure 3. Application of T7234

Functional Overview

The T7234 device provides two major interfaces for information transfer: the U-interface and the S/T-interface. The data flow matrix circuitry routes 2B+D information to the interface.

The architecture of the T7234 allows for a flexible combination of automatically and manually controlled functions. A control flow state machine, eoc state machine, and multiframing controller can be independently enabled or disabled. When enabled, these circuit blocks automatically perform their functions.

At the U-interface, the T7234 conforms to ANSI T1.601 and ETSI DTR/TM 3002. The 2B1Q line code provides a four-level (quaternary) pulse amplitude modulation code with no redundancy. Data is grouped into pairs of bits for conversion to quaternary (quat) symbols. Figure 4 shows an example of this coding method.

The U-interface transceiver section provides the 2B1Q line coder (D/A conversion), pulse shaper, line driver, first-order line balance network, clock regeneration, and sigma-delta A/D conversion. The line driver, when connected to the proper transformer and interface circuitry, generates pulses which meet the required 2B1Q templates. The A/D converter is implemented by using a double-loop, sigma-delta modulator.

The U-transceiver block also takes input from the data flow matrix and formats this information for the U-interface (see Figure 1). During this formatting, synchronization bits for U framing are added and a scrambling algorithm is applied. This data is then transferred to the 2B1Q encoder for transmission over the U-interface. Signals received from the U-interface are first passed through the sigma-delta A/D converter and then sent to the digital signal processor for more extensive signal processing. The block provides decimation of the sigma-delta output, linear and non-linear echo cancellation, automatic gain control, signal detection, phase shift interpolation, decision feedback equalization, timing recovery, descrambling, and line-code polarity detection. The decision feedback equalizer circuit provides the functionality necessary for proper operation on subscriber loops with bridged taps.

A crystal oscillator provides the 15.36011 MHz master clock for the device. The on-chip phase-locked loop provides the ability to synchronize the chip to the line rate.

The U-interface provides rapid cold start and warm start operation. From a cold start, the device is typically operational within 3 seconds. The interface supports activation/deactivation and, when properly deactivated, it stores the adaptive filter coefficients, permitting a warm start on the next activation request. A warm start typically requires 200 ms for the device to become operational.

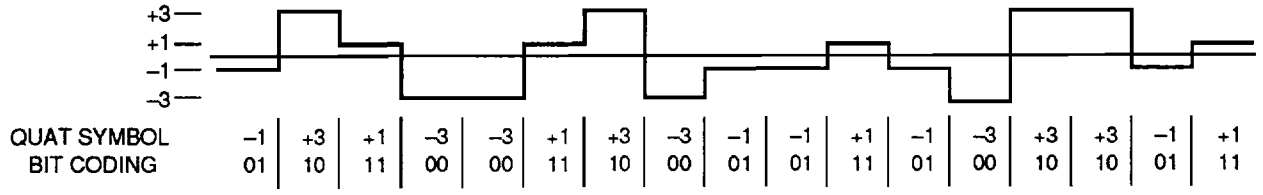


Figure 4. U-Interface Quat Example

Functional Overview (continued)

At the S/T-interface, the four-wire line transceiver meets the ANSI T1.605 standard, ITU-T I.430 recommendation, and ETSI ETS 300 012. At this interface, alternate space inversion (ASI) coding represents a logical 1 by the absence of a pulse and a logical 0 by alternating positive and negative pulses. Figure 5 illustrates the ASI coding method.

The S/T-transceiver provides a voltage-limited current driver at the transmit interface, a self-adjusting voltage threshold comparator at the receive interface, and a digital timing recovery circuit employing either adaptive or fixed timing modes. Transmit pulses meeting the required templates can be achieved with the connection of appropriate transformers and interface components. In the adaptive timing mode, extended passive bus and point-to-point configurations are supported. The fixed timing mode supports the short passive bus configuration. The timing mode is programmed via the external FTE pin.

The S/T- transceiver also interprets the frames received from the line and generates frames to be transmitted onto the S/T link. It exchanges full-duplex 2B+D information with the data flow matrix.

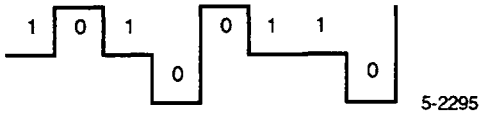


Figure 5. S/T-Interface ASI Example

The eoc state machine, when enabled, automatically performs the eoc channel functions as described in the ANSI requirements. When disabled, control of the eoc channel is passed to the microprocessor via the appropriate microprocessor register bits.

The ANSI maintenance controller can operate in fully automatic or in fully manual mode. In automatic mode, the device decodes and responds to maintenance states according to the ANSI requirements. In manual mode, the device is controlled by an external maintenance decoder that drives the $\overline{\text{RESET}}$ and $\overline{\text{ILOSS}}$ pins to implement the required maintenance states.

The multiframing controller, when enabled, allows the S and Q channels on the S/T-interface to be manipulated by the microprocessor. When disabled, the S and Q channel bits are automatically loaded with their default values for applications not supporting multiframing.

The control flow state machine performs the functions of reserved bit insertion, automatic implementation of the ANSI maintenance state machine, and automatic prioritization of multiple requests, such as reset, activation, maintenance, etc. Some bits which are normally controlled by the control flow state machine can be forced to their active state by writing the appropriate register (i.e., register GR1). When the control flow state machine is disabled (via the AUTOCTL bit in register GR0), the only change in the operation is that reserved bit control and ANSI maintenance control are passed directly to the microprocessor via register CFR0.

When the T7234 is powered on and there is no activity on the S/T- or U-interfaces (i.e., no pending activation request), it automatically enters a low power IDLE mode in which it consumes an average of 35 mW. This mode is exited automatically when an activation or U maintenance request occurs from either the microprocessor or the S/T- or U-interfaces.

The T7234 provides a board-level test capability that allows functional verification. Finally, an LED driver output indicates the status of the device during operation.

T7234 Reference Circuit

A reference circuit illustrating the T7234 in a stand-alone NT1 application is shown Figures 6 and 7. This depicts a complete stand-alone NT1 design with the exception of power supply circuitry and power status monitoring circuitry. A bill of materials for the schematic is shown in Table 2.

T7234 Reference Circuit (continued)

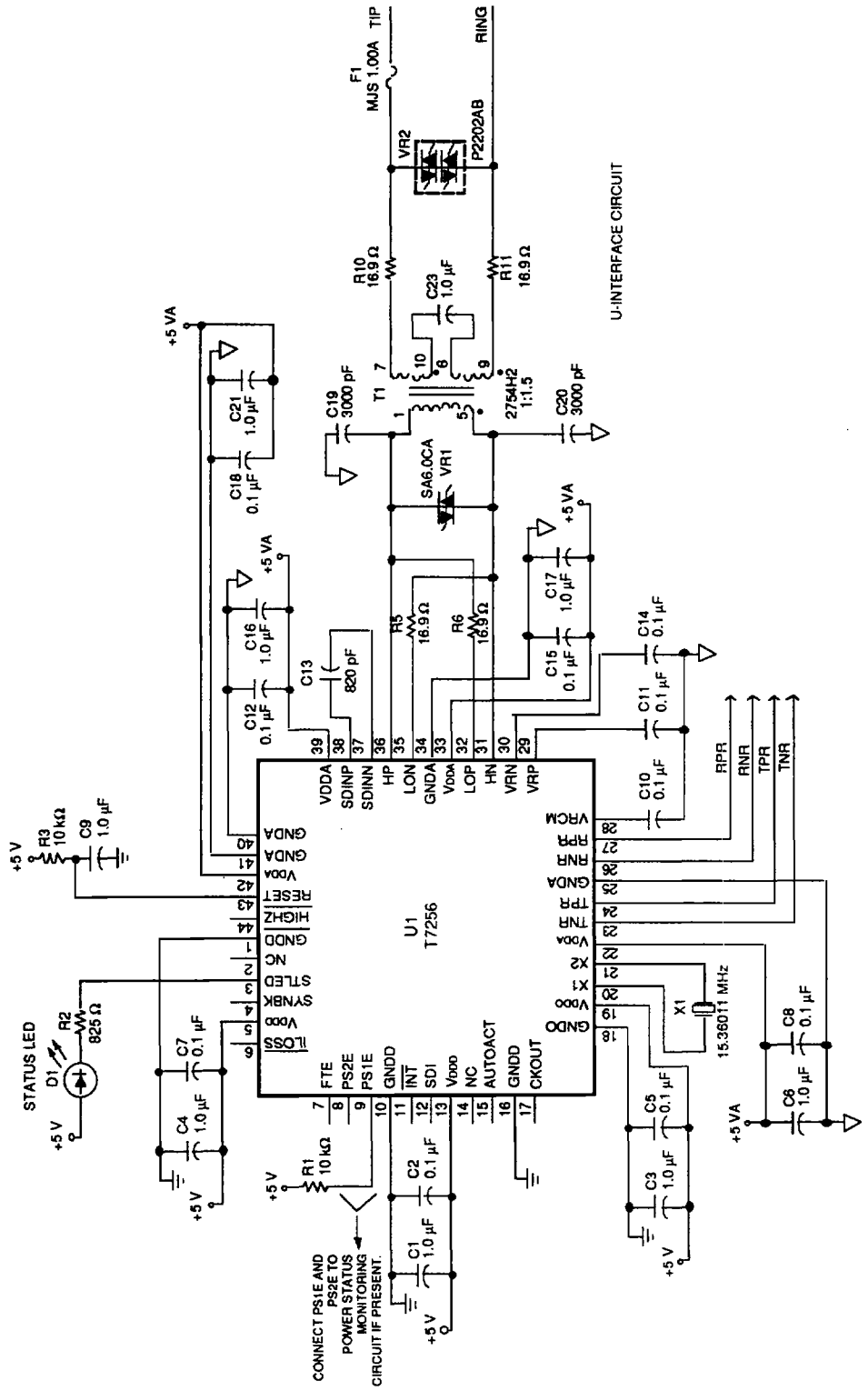


Figure 6. T7234 Stand-Alone Reference Circuit-A

T7234 Reference Circuit (continued)

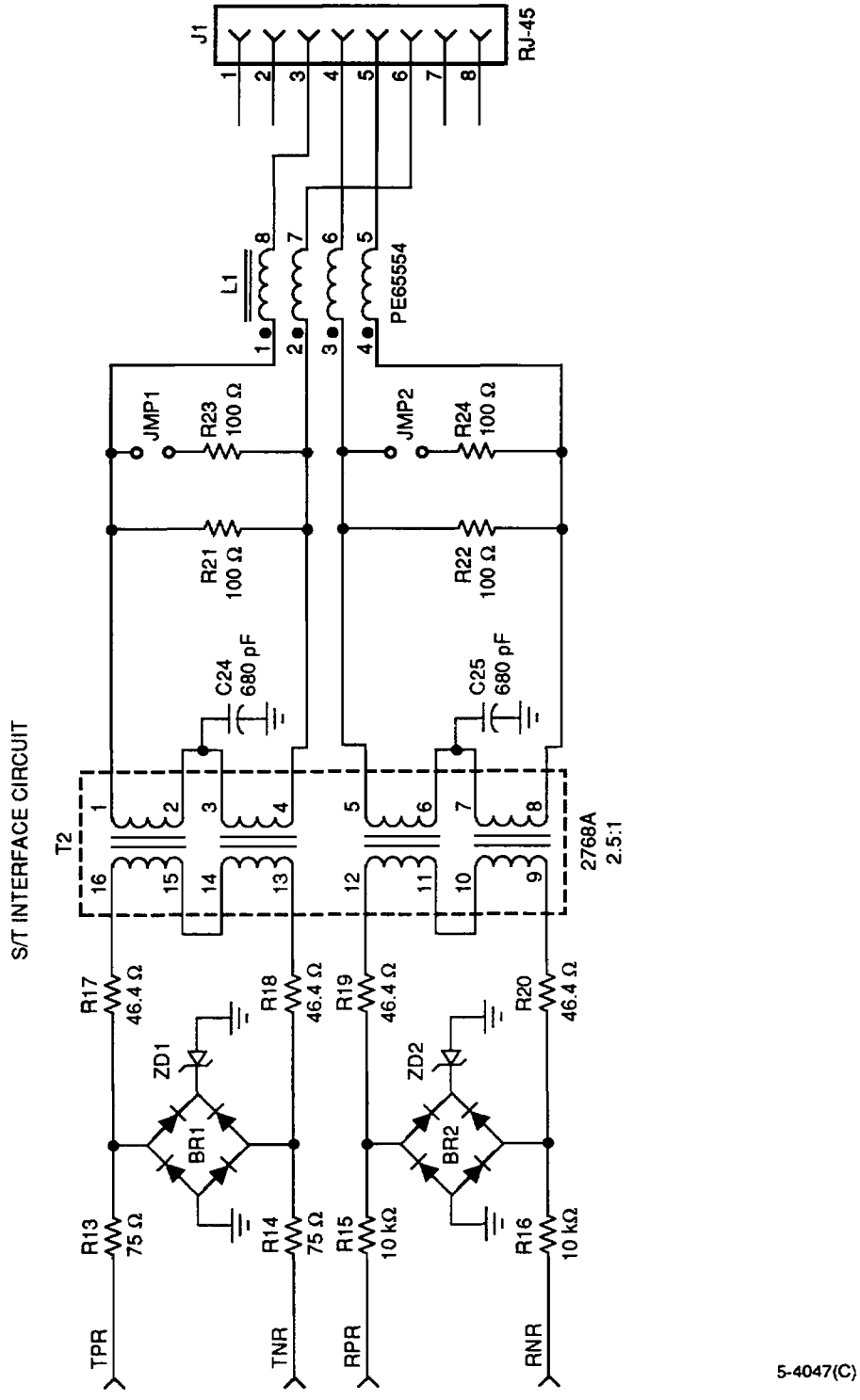


Figure 7. T7234 Stand-Alone Reference Circuit-B

T7234 Reference Circuit (continued)

Table 2. T7234 Reference Schematic Parts List

Reference Designator	Description	Source	Alternate Part
U1	T7234 IC	AT&T-ME	—
X1	crystal, 15.36011 MHz	Multiple	Examples: 2B Elettronica S.D.L. (Italy) P/N: TP0648 Tel: +39 6 6622432 Fax: +39 6 6632956 MTRON P/N: 4044-001 (605) 665-9321 SaRonix P/N: SRX5144 (415) 856-6900
T1	2754H2 transformer (1 kVRMS isolation)	AT&T-ME See notes at end of Table 2	AT&T 2754K2 (1.5 kVRMS) - pin compatible with 2754H2 Valor PT4084 (2 kVRMS) (619) 537-2500
T2	2768A transformer	AT&T-ME	Pulse Engineering, Inc. P/N: PE-65498 - pin compatible with 2754H2 (619) 674-8100 For applications requiring reinforced insulation: Advanced Power Components LTD (UK) P/N: APC2050S (single transformer) US Man Rep: Terry Manton Inc. (201) 447-8821 European office: 44 634 290588 VACUUMSCHMELZE (VAC) (Germany) P/N: T60403-L4097-X017-80 (single transformer) US: (908) 494-3530 Europe: 49 6181 38 2026 Pulse Engineering, Inc. P/N: PE-68998 (single transformer) (619) 674-8100P/N: PE-68998 (single transformer) (619) 674-8100

T7234 Reference Circuit (continued)

Table 2. T7234 Reference Schematic Parts List (continued)

Reference Designator	Description	Source	Alternate Part
F1	BEL MJS 1.00 A fuse	BEL Fuse, Inc. (201) 432-0463 See notes at end of Table 2	Raychem TR600-150 PTC (800) 272-9243
VR1	SA6.0CA secondary protector (thru-hole)	*Motorola**	*SGS Thomson*† 6T6V8CA (surface mount)
VR2	P2202AB *SIDACtor*‡ primary protector	Teccor (214) 580-1515	—
L1	PE65554 HF common-mode choke	Pulse Engineering (619) 674-8100	—
ZD1, ZD2	1.5SMC8.2AT3 8.2 V transient surge suppressor	*Motorola*	—
BR1, BR2	Diode bridge - use (x4) *Motorola* diodes 1N-4151	*Motorola*	—
D1	LED	multiple	—
J1	RJ45 connector	multiple	—
JMP1, JMP2	2-position jumper	multiple	—
C1, C3, C4, C6, C9, C16, C17, C21	1.0 µF decoupling capacitor	multiple	—
C2, C5, C7, C8, C10, C11, C12, C14, C15, C18	0.1 µF decoupling capacitor	multiple	—
C13	820 pF ± 5% capacitor (ceramic)	multiple	—
C19, C20	3000 pF ± 10% capacitors	multiple	
C22	1.0 µF 15 V ± 10% capacitor (**Note:** insulation resistance of this part must be >10 GΩ)	multiple	—

* *Motorola* is a registered trademark of Motorola, Inc.
† *SGS-Thomson* is a registered trademark of SGS-Thomson Microelectronics, Inc.
‡ *SIDACtor* is a trademark of Teccor, Inc.

T7234 Reference Circuit (continued)

Table 2. T7234 Reference Schematic Parts List (continued)

Reference Designator	Description	Source	Alternate Part
C23	1.0 µF 250 V ± 10% polyester capacitor	multiple	Example: Illinois Capacitor 105MWR250K1UF (708) 675-1760 ASC Capacitors Type X665 (818) 710-8555
C24, C25	680 pF ± 10% capacitors	multiple	—
R1, R3, R8, R15, R16	10 kΩ ± 10%, 1/8 W resistor	multiple	—
R2	825 Ω ± 10% , 1/4 W resistor	multiple	—
R4	17.8 kΩ ± 10%, 1/8 W resistor	multiple	—
R5, R6	16.9 Ω ± 1%, 1/4 W resistor	multiple	—
R7	2.2 MΩ ± 10%, 1/8 W resistor	multiple	—
R9	68.1 Ω ± 1% , 1/4 W resistor	multiple	—
R10, R11	16.9 Ω ± 1%, 1/4 W resistor	multiple	—
R12	2.2 kΩ ± 5%, 4 W resistor	multiple	—
R13, R14	75 Ω ± 1%, 1/8 W resistor	multiple	—
R17, R18, R19, R20	46.4 Ω ± 1%. 1/8 W resistor	multiple	—
R21, R22, R23, R24	100 Ω ± 1%, 1/8 W resistor	multiple	—

Note: The AT&T 2754K2 and the Valor PT4084 have different winding resistances than the AT&T 2754H2, and therefore require a change to the line side resistors (R10 and R11). In addition, if the Raychem TR600-150 PTC is used in place of the BEL fuse at location F1 to provide more robust protection (at a slightly higher cost), the line side resistors must be adjusted to compensate for the added PTC resistance of 12 Ω. The following table lists the necessary resistor values for these cases. Note that R10 and R11 are specified at 1%. This is due to the fact that the values were chosen from standard 1% resistor tables. When a PTC is used, the overall tolerance will be greater than 1% and R10 and R11 won't necessarily be matched. This is acceptable, as long as the total line side resistance is kept as close as possible to the ideal value. See Questions and Answers #11 for more details.

Table 3. Line Side Resistor Requirements

Transformer	When BEL Fuse Is Used	When TR600-150 Is Used	
	R10, R11	R10	R11
AT&T 2754H2	16.9 Ω	4.87 Ω	16.9 Ω
AT&T 2754K2	13.7 Ω	1.69 Ω	13.7 Ω
Valor PT4084	5.36 Ω	0 Ω	0 Ω

U-Interface Description

The T7234 U-interface transceiver circuitry is designed to allow systems to meet the loop-range requirements of ANSI standard T1.601 and ETSI technical report DTR/TM 3002 when the interface is used with the proper external circuitry.

Analog Interface

At the U-interface, proper line termination is required to meet the 2B1Q pulse templates and to achieve maximum loop range performance. Figures 6 and 7 show typical circuits for connecting the T7234 to the 2-wire loop; however, a specific application may vary depending on the system requirements.

The transmit outputs of the T7234 (LOP, LON) are connected to the interface transformer through 16.9 Ω ± 1% resistors, while the internal hybrid connections (HP, HN) are made directly to the device side of the transformer. A 1.5:1 turns ratio transformer, such as the AT&T 2754H2, is used to isolate the device from the loop plant. The center tap of the line side of the transformer is connected through a 1.0 µF ± 10% dc blocking capacitor.

The transformer line side is connected to the loop through 16.9 Ω ± 1% resistors. Secondary overvoltage protection is typically required on the device side of the transformer to protect the device. Primary overvoltage and overcurrent protection at the line interface is required for protecting the device and the equipment as well as providing safety to equipment users. The protection scheme shown in Figure 6 should be adequate for meeting *UL**1459 and FCC part 68 surge and safety requirements. For an in-depth discussion of surge protection issues when interfacing to the subscriber loop, the following application notes are available.

1. Overvoltage Protection of Solid-State Subscriber Loop Circuits, Chapter 2, pg 11, *Analog Line Card Products* Data Book (CA94-007ALC).
2. *Protection of Telecommunications Customer Premises Equipment*, Raychem Corporation, 800-272-9243.

Superframe Structure

Data is transmitted over the U-interface in 240-bit groups called U-frames. Each U-frame consists of an 18-bit synchronization word or inverted synchronization word (SW or ISW), 12 blocks of 2B+D data (216 bits), and six overhead bits (M bits). A U-interface superframe consists of eight U frames grouped together. The beginning of a U superframe is indicated by the inverted sync word (ISW). The six overhead bits (M1—M6) from each of the eight U frames, when taken together, form the 48 M bits. Figure 8 shows how U frames, superframes, and M bits are arranged.

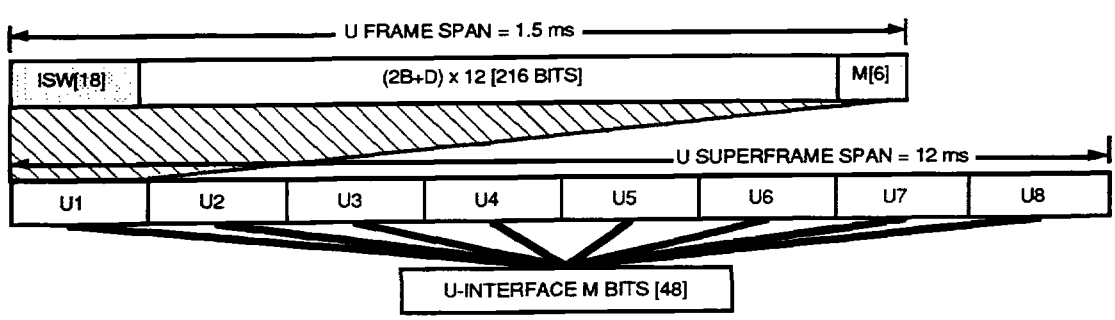


Figure 8. U-Interface Frame and Superframe

* *UL* is a registered trademark of Underwriters Laboratories, Inc.

U-Interface Description (continued)

Of the 48 M bits, 24 bits form the embedded operations channel (eoc) for sending messages from the LT to the NT and responses from the NT to the LT. There are two eoc messages per superframe with 12 bits per eoc message (eoc1 and eoc2). Another 12 bits serve as U-interface control and status bits (UCS). The last 12 bits form the cyclic redundancy check (CRC) which is calculated over the 2B+D data and the M4 bits of the previous superframe. Figure 9 and Table 4 show the different groups of bits in the superframe.

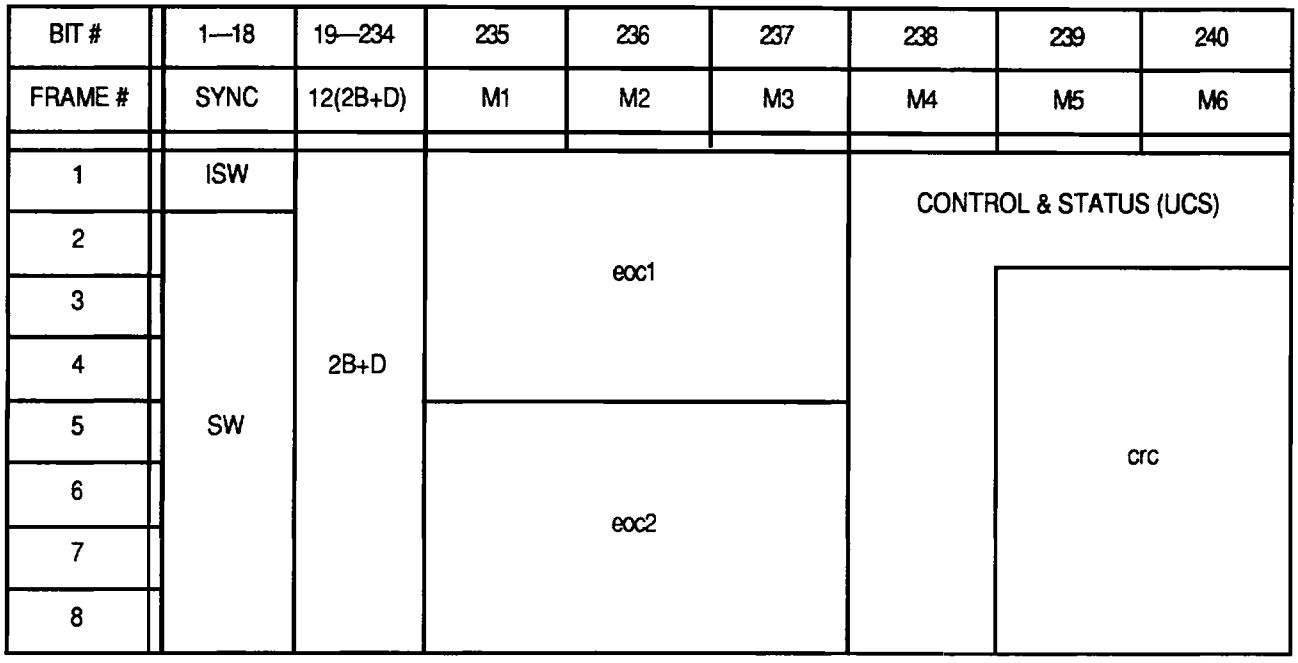


Figure 9. U-Interface Superframe Bit Groups

Bit Assignments

Table 4. U-Interface Bit Assignment

Bit #	1—18	19—234	235	236	237	238	239	240
Frame #	Sync	12(2B+D)	M1	M2	M3	M4	M5	M6
1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	$R_{1,5}$	$R_{1,6}$
2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea (ps1)*	$R_{2,5}$	febe
3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	$R_{3,4}$ (ps2)*	crc_1	crc_2
4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	$R_{4,4}$ (ntm)*	crc_3	crc_4
5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	$R_{5,4}$ (cso)*,†	crc_5	crc_6
6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	$R_{6,4}$	crc_7	crc_8
7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa (sai)*	crc_9	crc_{10}
8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib (nib)*,‡	crc_{11}	crc_{12}

* LT(NT). Values in parentheses () indicate meaning at the NT.
† cso is fixed at 0 by the device to indicate both cold and warm start capability.
‡ nib is fixed at 1 by the device to indicate the link is normal.

S/T-Interface Description

The T7234 S/T-interface is designed to allow systems to meet the requirements of the ANSI T1.605 standard, ITU-T I.430 recommendation, and ETSI ETS 300 012 when used with the proper external circuitry. The connection of a T7234 NT endpoint to a TE is shown in Figure 7. For an in-depth discussion of ISDN S/T line interface issues refer to the November 1993 *Design of ISDN S/T Line Interface Circuitry Using the T7250C/ T7259* Application Note (AP93-008TCOM).

Analog Interface

The S/T-interface consists of two sections. The line transmitter and the line receiver are essentially standalone designs, except for limited sharing of timing and control circuits. The transmitter-receiver pair connects to 2.5:1 transformers. The transmitter connects to the transformer through 121 Ω ± 1% resistors. The receiver connects to the transformer through 10 kΩ ± 10% resistors.

The line transmitter is a voltage-limited current source that conforms to the I.430/T1.605 specifications. The transmitted bits are timed by an internal 192 kHz clock derived from the U-interface. Table 5 summarizes the mechanism used by the transmitter to send the alternate space inversion (ASI) code through the transmit transformer.

ASI is a differential strategy, with positive and negative rails connecting to the transformer. Current flows through the transformer only when there is a voltage difference on the two rails. When a logical one or mark is being sent, meaning no current is desired, both rails go to a high-impedance condition. When a positive logical zero (space) is transmitted, the positive rail forces current to the negative rail through the transformer. The reverse occurs for a negative zero.

The line receiver is more complex. Since the loop length to the subscriber(s) is variable, as is the number of TEs on the loop (1 to 8), the receiver must be sufficiently intelligent to adjust for widely varying input waveforms. The S/T receiver is designed to use a single adaptive timing mode to synchronize to all signals conforming to the I.430 templates. This mode can be used on any loop configuration (point-to-point, extended passive bus, short passive bus) in which round trip delays are between 0 µs and 42 µs and differential delays between TEs are between 0 µs and 3.1 µs. This means that if the line transmitter and the line receiver are directly connected externally in a loopback configuration, the receiver can extract the 2B+D information correctly from the transmitted stream.

A short passive bus configuration permits TEs to be connected anywhere along the full length of the cable, with the restriction that the total round trip delay must be between 10 µs and 14 µs for all TEs. Thus, worst-case differential delay between TEs can be as much as 4 µs. If the differential delay is more than 3.1 µs, adaptive timing mode cannot be used. A fixed timing mode is available for this case. The fixed timing mode is invoked through the FTE pin. When the T7234 uses fixed timing, the input stream is sampled 4.2 µs after the leading edge of each 192 kHz transmit bit interval.

The interval required for the receiver to synchronize to the received stream is 5 to 60 S/T frames (1.25 ms to 15 ms). The receiver can achieve framing only when the INFO 3 pattern appears on the loop. Three frames are required to recognize new INFO patterns.

Table 5. Line Transmission Code

Positive Rail	Negative Rail	Current	Logic
Z*	Z*	0	1
1	0	+1	0
0	1	−1	0

* Z = high impedance.

Frame and Multiframe Bit Assignments

The S/T-interface transfers its subscriber line 2B+D information as a 192 kbits/s full-duplex signal grouped into frames of 48 bits with a period of 250 µs, as specified in the ITU-T I.430/ANSI T1.605 standard. Thirty-six of the 48 bits sent in each direction convey user information (two 8-bit occurrences of each of the two B channels, and four D-channel bits). The remaining 12 bits per frame are used for framing, control, dc balance, and maintenance. The frame structures are shown in each direction in Figure 10.

In the bit stream transmitted from the terminal endpoint (TE) to the network termination (NT), 4 bits are used for framing (F and FA, each with a dc balancing bit L), eight L bits are used to balance the 32 B-channel bits, and 4 bits are D-channel bits.

S/T-Interface Description (continued)

For the NT-to-TE transmission, 4 bits (F with dc balancing bit L, FA, and N) are used for framing, one M bit marks the start of a 20-frame multiframe, four E bits form an echo channel for retransmission of the D-channel bits received from the TE, one L bit is used to balance the contents of the entire frame, and 1 bit (A) is set to one when bit synchronization is achieved between TE and NT as part of the INFO 4 state. One S bit is used for transmitting S subchannel messages in an NT-to-TE multiframe.

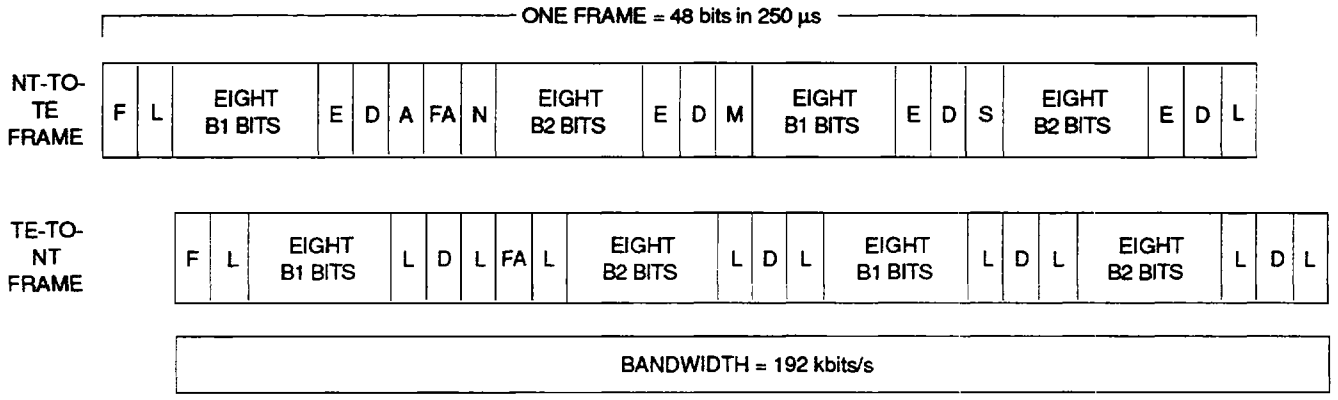
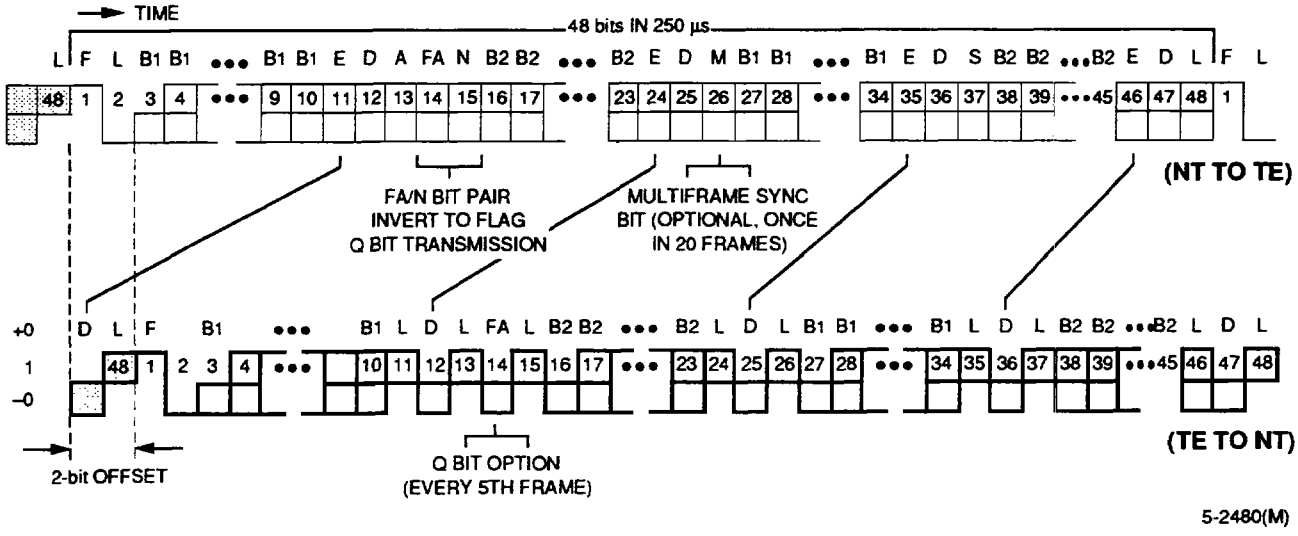


Figure 10. Frame Structures of NT and TE Frames

S/T-Interface Description (continued)

The framing procedure uses bipolar line-code violations to establish synchronization. Since the last binary 0 of any frame is a positive pulse and the F bit is also defined to be a positive pulse (see Figure 11), the first bit of each frame represents a coding violation. In addition, the second bit of each frame, a balance bit, is a negative pulse, and the next binary 0 in the frame is forced to be negative, causing another violation. Both bipolar violations allow framing and provide dc balance. All other pulses follow the alternating convention.

In the TE-to-NT direction, in at least four of five frames, this second violation occurs within 13 bits of the F bit. If this coding algorithm is not maintained, the receiver loses synchronization, but the T7234 continues transmitting.



F = Framing bit
L = DC balancing bit
D = D channel bit
E = Echo D channel bit
FA = Auxiliary framing bit or Q channel bit
N = Bit set to binary value N = FA
A = Activation bit
S = S channel bit
M = Multiframe synchronization bit
B1 = Bit within B channel 1
B2 = Bit within B channel 2

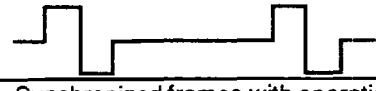
Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal.	INFO 0	No signal.
INFO 2	Frame with all bits of B, D, and D echo (E) channels set to binary ZERO; bit A set to binary ZERO; N and L bits set according to the normal coding rules.	INFO 1	A continuous signal with the following pattern: positive ZERO, negative ZERO, six ONEs. 
INFO 4	Frames with operational data on B, D, and E channels; bit A set to binary ONE.	INFO 3	Synchronized frames with operational data on B and D channels.

Figure 11. Details of NT and TE Frames

S/T-Interface Description (continued)

If multiframing is enabled, the M bit in the NT-to-TE direction is set to a one every 20 frames and the FA bit is set to one every five frames. The TE recognizes these states and, in returned frames immediately corresponding to those in which the NT set the FA bit, replaces the FA bit it sends to the NT with a Q bit (Q1 through Q4). Q1 is returned for each frame in which both the M and FA bits were set to one by the NT, with Q2 through Q4 following at five-frame intervals. (See Figure 12.)

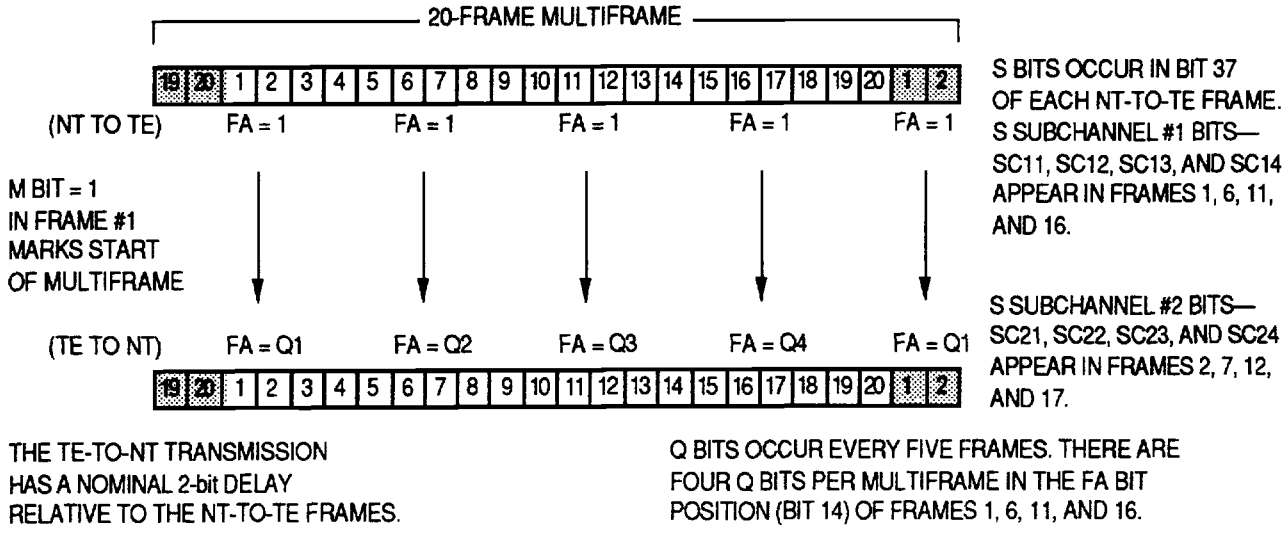


Figure 12. Multiframing—S Subchannels and Q Subchannels

Data Flow Matrix Description

B1, B2, D Channel Routing

The T7234 supports extremely flexible B1, B2, and D channel routing among major circuit blocks in order to accommodate multiple applications. Channel routing is controlled via the data flow control registers. Figure 13 below shows a block diagram of the device and the channel paths to and from the U-transceiver and S/T-transceiver. Channel flow is determined by specifying the source of channel data at the two points shown in the figure: (1) U-transceiver transmit input and (2) S/T-transceiver transmit input. A switch matrix within the data flow matrix block routes channels to and from the specified points.

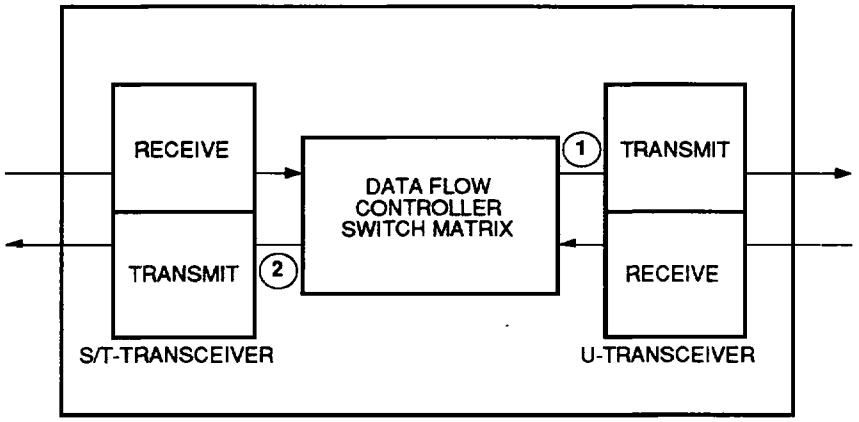
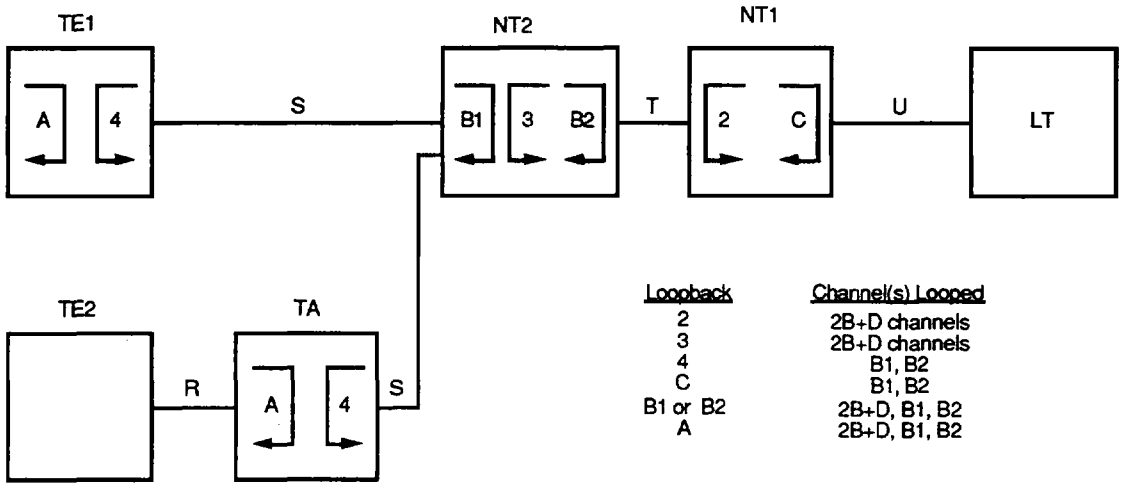


Figure 13. B1, B2, D Channel Routing

Loopbacks

The figure below shows the Layer-1 loopbacks that are defined in ITU-T I.430, Appendix I and ANSI Specification T1.605, Appendix G. A complete discussion of these loopbacks is presented in ITU-T I.430, Appendix I.



TE1 = ISDN terminal
TE2 = Non-ISDN terminal
TA = Terminal adapter
NT2 = Network termination 2
NT1 = Network termination 1
LT = Line termination

R = R reference point
S = S reference point
T = T reference point
U = U reference point

Figure 14. Location of the Loopback Configurations (Reference ITU-T I.430 Appendix I)

If a U-interface transparent B1 or B2 loopback is requested via an eoc message, the proper channel is looped upstream of the data flow matrix. All other device functions are unaffected.

If a U-interface transparent 2B+D loopback is requested via an eoc message (loop 2 in Figure 14), the 2B+D data will be looped as close to the S/T-interface as possible. In stand-alone mode, the device overrides the SXE bit to force all 0s in the echo channel and also overrides the SXB1, SXB2, SXD, UXB10, UXB11, UXB21, UXB20, and UXD data flow matrix bits to force a U- to S/T-interface data path.

Modes of Operation

To provide flexibility in the system architecture, the T7234 transceiver can operate in stand-alone mode to provide basic NT1 functionality. In stand-alone mode, the T7234 automatically handles U- and S/T-interface activation, control, and maintenance according to the ANSI T1.601 and ITU-T I.430/ANSI T1.605 standards. The device is configured for this mode via internal pull-ups and pull-downs. Table 6 shows the transceiver control pins that may be relevant in stand-alone mode.

Table 6. Stand-Alone Mode

Pin	Symbol	Function
4	SYN8K/LBIND	Performs the SYN8K or LBIND depending on the state of SDI (pin 12) during an external $\overline{\text{RESET}}$.
7	FTE	Performs the FTE function. Selects the S/T-interface timing recovery mode.
8	PS2E	Performs the PS2E function. Controls the PS2 bit in the transmit U-interface data stream.
9	PS1E	Performs the PS1E function. Controls the PS1 bit in the transmit U-interface data stream.
11	ACTMODE	Performs the ACTMODE function. Controls the act bit in the transmit U-interface data stream during 2B+D loopbacks.
12	SYN8K	Held high or low on powerup or RESET to control SYN8K/LBIND/FS (pin 4).
15	AUTOACT	Held high or low on powerup or RESET to control automatic activation attempt.
43	$\overline{\text{RESET}}$	Resets the device.

STLED Description

The STLED pin is used to drive an LED and provides a visual indication of the current state of the T7234. The STLED control is typically configured to illuminate the LED when STLED is LOW. This convention will be assumed throughout this section.

The following table (Table 7) describes the four states of STLED, the list of system conditions that produce the state, and the corresponding ANSI states, as defined in ANSI T1.601-1992 (Tables C1 and C4) and ETSI DTR/TM 3002-1992 (Tables A3 and I2).

Note: The ETSI state names begin with the letters NT instead of H. Also, the ETSI state tables do not include a state NT11 because it is considered identical to state NT6. Table A3 of the ETSI standard contains the additional states NT6A, NT7A, and NT8A to describe states related to the eoc loopback 2 (2B+D loopback). The most likely ANSI state for each STLED state is shown in bold typeface.

Table 7. STLED States

STLED State	List of System Conditions that Can Cause STLED State	Corresponding ANSI States
High (LED off)	RESET (pin 43) = 0 AUTOCTL = 0 (register GR0, bit 3), or AUTOEOC = 0 (register GR0, bit 4), or STOA = 0 (register GR2, bit 7)	NA
	U and S/T not active	H0, **H1**, H10, H12
8 Hz Flashing	RESET = 0 (register GR0, bit 0) Quiet mode active, or ILOSS mode active	NA
	U activation attempt in progress	H2, H3, H4
	AIB = 0 (register CFR1, bit 6)	H7, **H8**
	eoc-initiated 2B+D loopback active	NT6A*, NT7A*, **NT8A***
1 Hz Flashing	U active, S/T not fully active	H6, H6(a), **H7**, H11, H8(a)†, H8(b), H8(c)
Low (LED on)	U and S/T fully active	H8

* These are ETSI DTR/TM-3002 states not yet defined in ANSI T1.601, although they are defined in revised ANSI tables which are currently on the living list (i.e., not yet an official part of the standards document).
† State H8(a) is most likely when U-interface bit uoa = 0.

The flow chart in Figure15 illustrates the priority of the logic signals which control the STLED pin. In the decision diamonds, those names in all capital letters denote T7234 register bit names. The XACT, OOF, and AIB bits are read-only bits determined by the internal logic based on system events. Other names in the decision diamonds (quiet mode, ILOSS mode, Loop2, INFO 2, INFO 4) represent system conditions that cannot be directly monitored or controlled by the microprocessor interface.

STLED Description (continued)

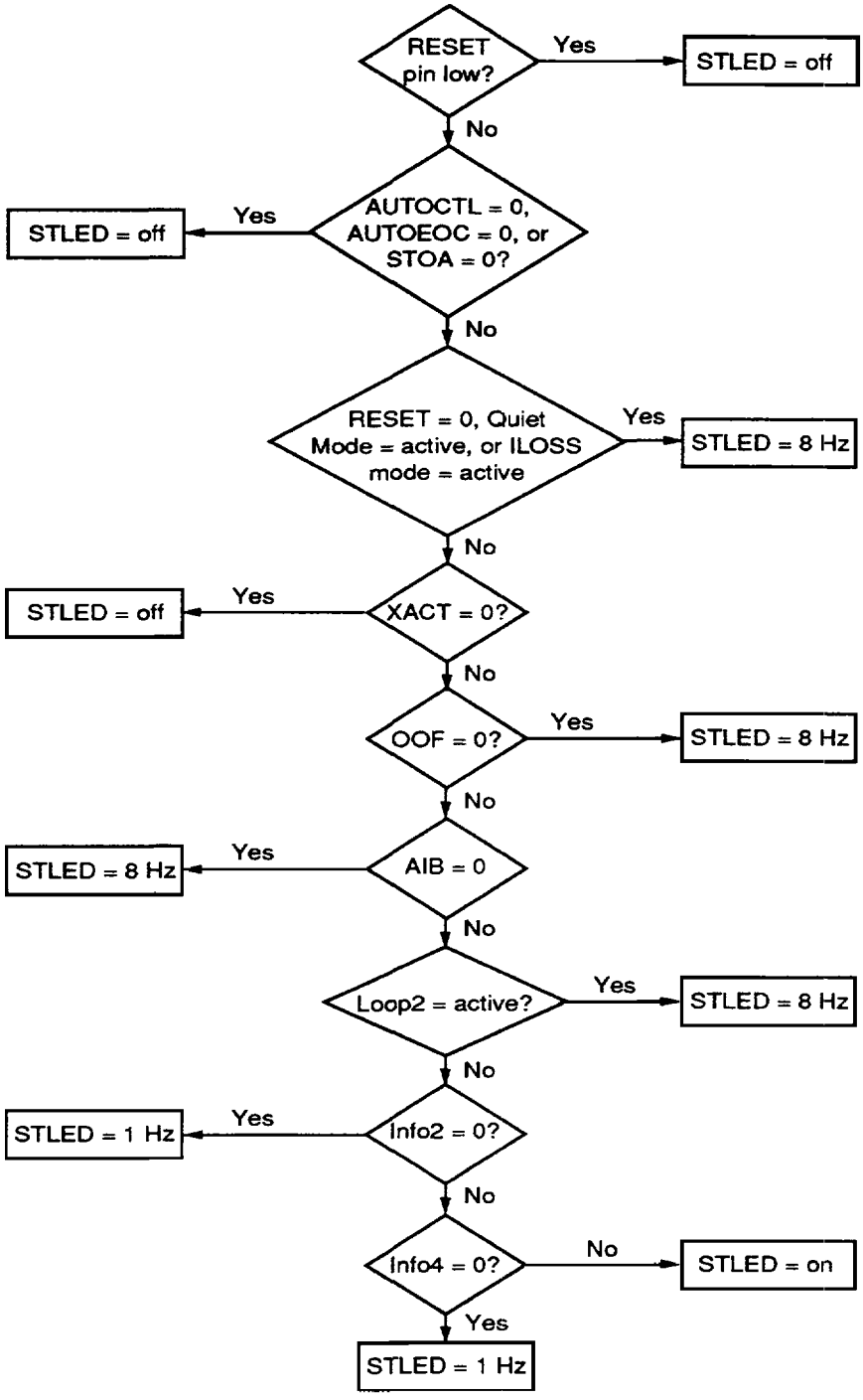


Figure 15. STLED Control Flow Diagram

eoc State Machine Description

The following list shows the eight eoc states defined in ANSI T1.601 and ETSI DTR/TM 3002.

01010000 — Operate 2B+D loopback.
01010001 — Operate B1 channel loopback.
01010010 — Operate B2 channel loopback.
01010011 — Request corrupt CRC.
01010100 — Notify of corrupted CRC.
11111111 — Return to normal (default).
00000000 — Hold state.
10101010 — Unable to comply.

Normally, the T7234 automatically handles the eoc channel processing per the ANSI and ETSI standards.

ANSI Maintenance Control Description

The ANSI maintenance controller of the T7234 can operate in manual mode.

Manual mode can be used in applications where an external maintenance decoder is used to drive the $\overline{\text{RESET}}$ and $\overline{\text{ILOSS}}$ pins of the T7234. In this mode, the $\overline{\text{RESET}}$ pin places the device in quiet mode and the $\overline{\text{ILOSS}}$ pin controls SN1 tone transmission.

Board-Level Testing

In order to reduce board-level test cost and development time, and to simplify field diagnostic procedures, the T7234 supports board-level testability. The configuration is described below. For board-level testing during manufacturing, the $\overline{\text{HIGHZ}}$ pin tristates all digital outputs.

External Stimulus/Response Testing

Input a known, well characterized data pattern at the U-interface and monitor the S-interface output.

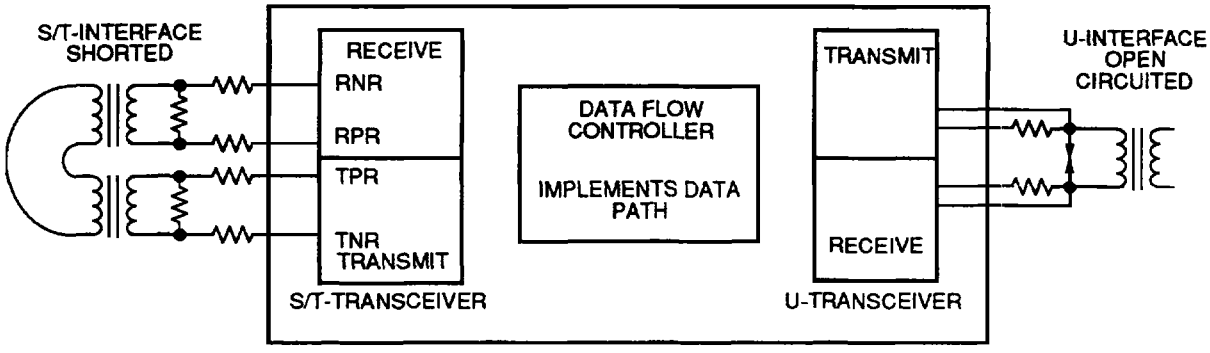
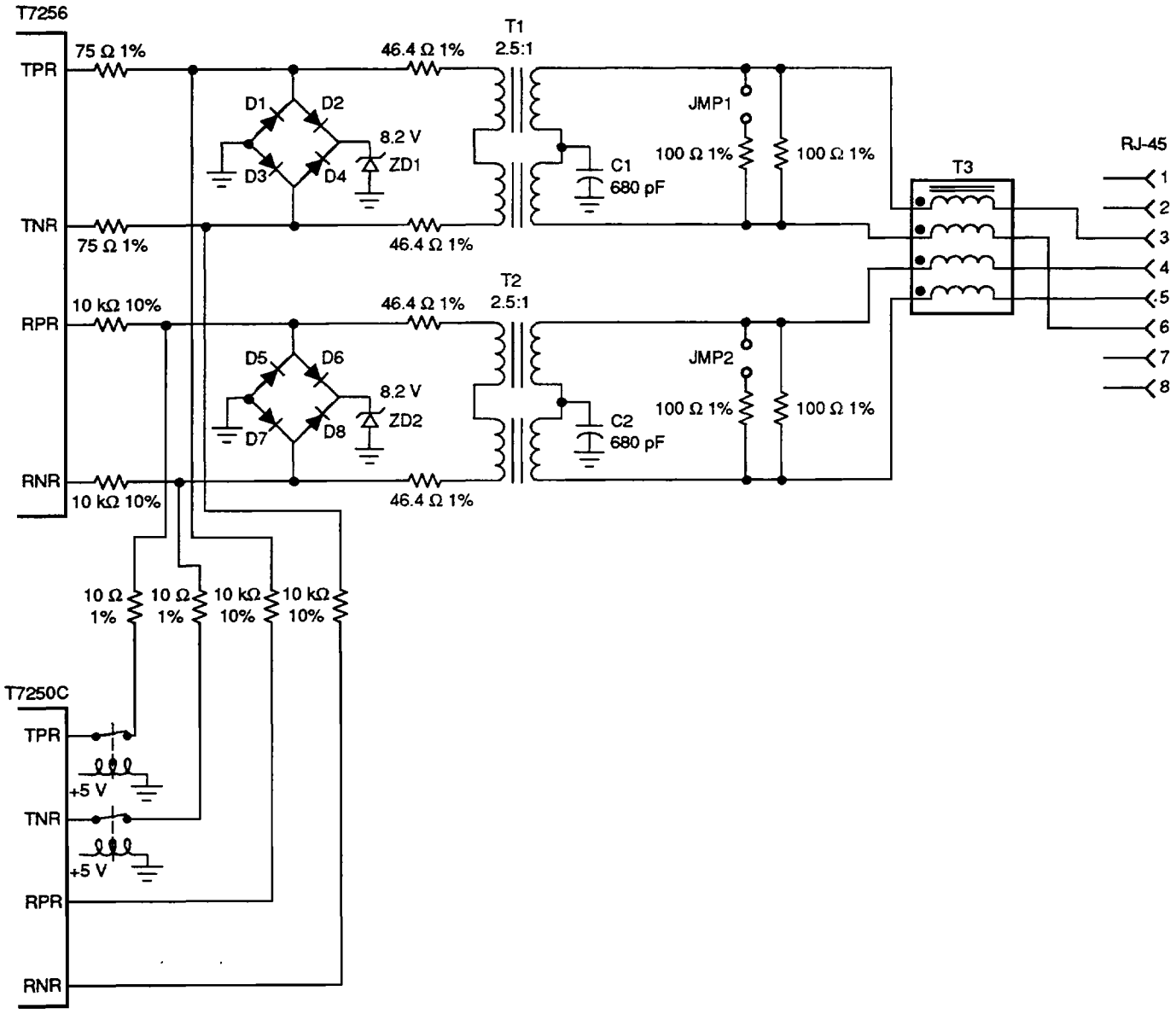


Figure 16. External Stimulus/Response Configuration

Application Briefs

Using the T7234 in a Combination TE/TA Environment

The approach is to use the AT&T T7250C TE chip as a local TE on the NT1/TA and connect it to the T7234 S/T-interface as shown in Figure 17. A standard short passive bus connection can be used for external TEs (the bus configuration is by definition a short passive bus, since there is a TE connected locally). The analog phone circuitry (codecs, battery feeds, etc.) connects to the system side of the T7250C using the TDM interface to transfer 2B+D data. A microprocessor interface on the T7250C provides access to the internal HDLC formatter (see the T7250C data sheet, DS95-029ISDN). This solution is ideal if a terminal adapter based on the T7250C already exists, because the hardware and software are identical. The external HDLC formatters are eliminated in this solution because the T7250C internal HDLC formatter provides this function.



Notes:
Install JMP1 and JMP2 if no external TE is a attached.
Remove JMP1 and JMP2 if external TE with 100 Ω termination is attached.

Figure 17. Local TE Connection, Option #2

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

External leads can be soldered safely at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V_{DD}	–0.5	6.5	V
Power Dissipation (package limit)	P_D	—	800	mW
Storage Temperature	T_{stg}	–55	150	°C
Voltage (any pin) with Respect to GND	—	–0.5	6.5	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters:

ESD Threshold Voltage

Device	Voltage
T7234-ML2	>1000

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Ambient Temperature	T_A	V_{DD} = 5 V ± 5%	–40	—	85	°C
Any V_{DD}	V_{DD}	—	4.75	5.0	5.25	V
GND to GND	V_{GG}	—	–10	—	10	mV

Electrical Characteristics

All characteristics are for a 15.36011 MHz crystal, 135 Ω line load, random 2B+D data, T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, GND = 0 V, and output capacitance = 50 pF.

Power Consumption

Table 8. Power Consumption

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Consumption	Operating, Random Data	—	270	350	mW
Power Consumption	Powerdown Mode	—	35	50	mW

Pin Electrical Characteristics

Table 9. Digital dc Characteristics (over operating ranges)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current:					
Low	I_{ILPU}	V_{IL} = 0 (Pins 2, 6, 7, 11, 44)	–52	–10	µA
High	I_{IHPU}	V_{IH} = V_{DD} (Pins 2, 6, 7, 11, 44)	—	–10	µA
Low	I_{ILPD}	V_{IL} = 0 (Pins 8, 9, 12, 15, 43)	–10	—	µA
High	I_{IHPD}	V_{IH} = V_{DD} (Pins 8, 9, 12, 15, 43)	–10	–52	µA
Input Voltage:					
Low	V_{IL}	All pins except 2, 6, 43	—	0.8	V
High	V_{IH}	All pins except 2, 6, 43	2.0	—	V
Low-to-High Threshold	V_{ILS}	Pin 43	V_{DD} – 0.5	—	V
High-to-Low Threshold	V_{IHS}	Pin 43	—	0.5	V
Low	V_{ILC}	Pins 2, 6	—	0.2 V_{DD}	V
High	V_{IHC}	Pins 2, 6	0.7 V_{DD}	—	V
Output Leakage:					
Low	I_{OZL}	V_{OL} = 0, Pin 44 = 0 (Pins 3, 14)	—	10	µA
High	I_{OZH}	V_{OH} = V_{DD}, Pin 44 = 0 (Pins 3, 14)	–10	—	µA
Low	I_{OZLPU}	V_{OL} = 0, Pin 44 = 0 (Pins 11)	–52	–10	µA
High	I_{OZHPU}	V_{OH} = V_{DD}, Pin 44 = 0 (Pins 11)	—	10	µA
Low	I_{OZLPD}	V_{OL} = 0, Pin 44 = 0 (Pins 4, 8, 9, 17)	–10	—	µA
High	I_{OZHPD}	V_{OH} = V_{DD}, Pin 44 = 0 (Pins 4, 8, 9, 17)	10	52	µA
Output Voltage:					
Low, TTL	V_{OL}	I_{OL} = 4.5 mA (Pin 3)	—	0.4	V
		I_{OL} = 19.5 mA (Pins 4, 9)	—	0.4	V
		I_{OL} = 8.2 mA (Pins 8, 17)	—	0.4	V
		I_{OL} = 6.5 mA (Pin 14)	—	0.4	V
		I_{OL} = 3.3 mA (Pin 11)	—	0.4	V
High, TTL	V_{OH}	I_{OH} = 32.2 mA (Pins 4, 9)	2.4	—	V
		I_{OH} = 13.5 mA (Pins 8, 17)	2.4	—	V
		I_{OH} = 10.4 mA (Pins 3, 14)	2.4	—	V
		I_{OH} = 5.1 mA (Pin 11)	2.4	—	V

Electrical Characteristics (continued)

S/T-Interface Receiver Common-Mode Rejection

Table 10. S/T-Interface Receiver Common-Mode Rejection

Parameter	Symbol	Specifications	Unit
Common-Mode Rejection (at device pins)	CMR	400	mV

Crystal Characteristics

Table 11. Fundamental Mode Crystal Characteristics

These are the characteristics of a crystal for meeting the ±100 ppm requirements of T1.601 for NT operation. The parasitic capacitance of the PC board to which the T7234 crystal is mounted must be kept within the range of 0.6 pF ± 0.4 pF.

Parameter	Symbol	Test Conditions	Specifications	Unit
Center Frequency	Fo	With 25.0 pF of loading	15.36011	MHz
Tolerance Including Calibration, Temperature Stability, and Aging	TOL	—	±60	ppm
Drive Level	DL	Maximum	0.5	mW
Series Resistance	Rs	Maximum	20	Ω
Shunt Capacitance	Co	—	3.0 ± 20%	pF
Motional Capacitance	Cm	—	12 ± 20%	fF

Electrical Characteristics (continued)

Crystal Characteristics (continued)

Table 12. Internal PLL Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Total Pull Range	—	±250	—	—	ppm
Jitter Transfer Function	–3 dB point (NT), 18 kft 26 AWG	—	5*	—	Hz
Jitter Peaking	1.5 Hz typical	—	1.0*	—	dB

* Set by digital PLL; therefore, variations track U-interface line rate.

Timing Characteristics

Table 13. Clock Timing (See Figure 30.)

Symbol	Parameter	Min	Typ	Max	Unit
SYN8K	8 kHz Duty Cycle	49.8	—	50.2	%
CKOUT	Duty Cycle: In 15.36011 MHz Mode In 10.24 MHz Mode	 40 23*	 — —	 60 52*	 % %
tR1, tF1	Rise or Fall Time	—	30	—	ns
tCOLFH	CKOUT Clock to Frame Sync (SYN8K)	—	—	50	ns
tR2, tF2	CKOUT Clock Rise or Fall	—	15	—	ns

* Includes the effect of phase steps generated by the digital phase-locked loop.

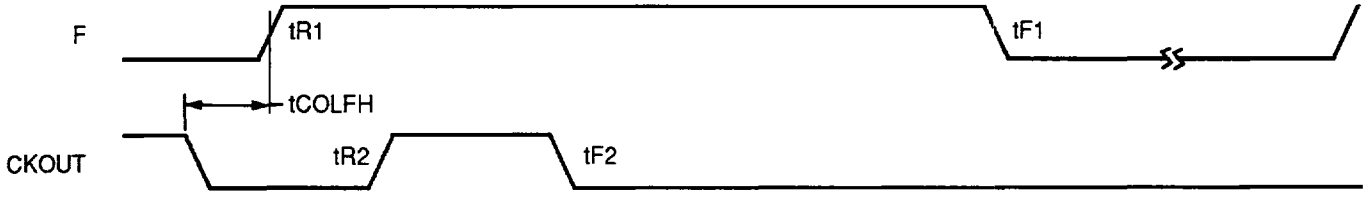


Figure 18. Timing Diagram Referenced to F

Table 14. RESET Timing

Parameter	Description	Min	Max	Unit
tRSLFL, tFLRSH	RESET Setup and Hold Time	60	—	ns
tRSLRSH	RESET Low Time: From Idle Mode or Normal Operation From Power-on	 375 1.5	 — —	 µs ms

Timing Characteristics (continued)

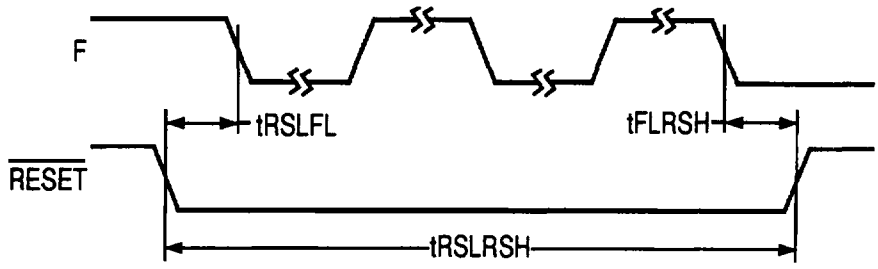


Figure 19. RESET Timing Diagram

Switching Test Input/Output Waveform

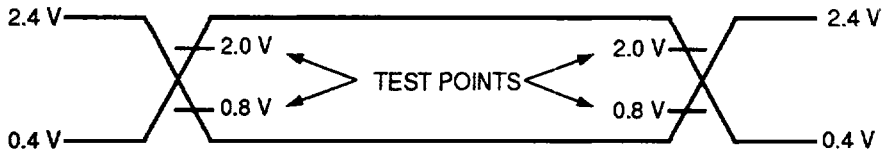


Figure 20. Switching Test Waveform for RESET Timing

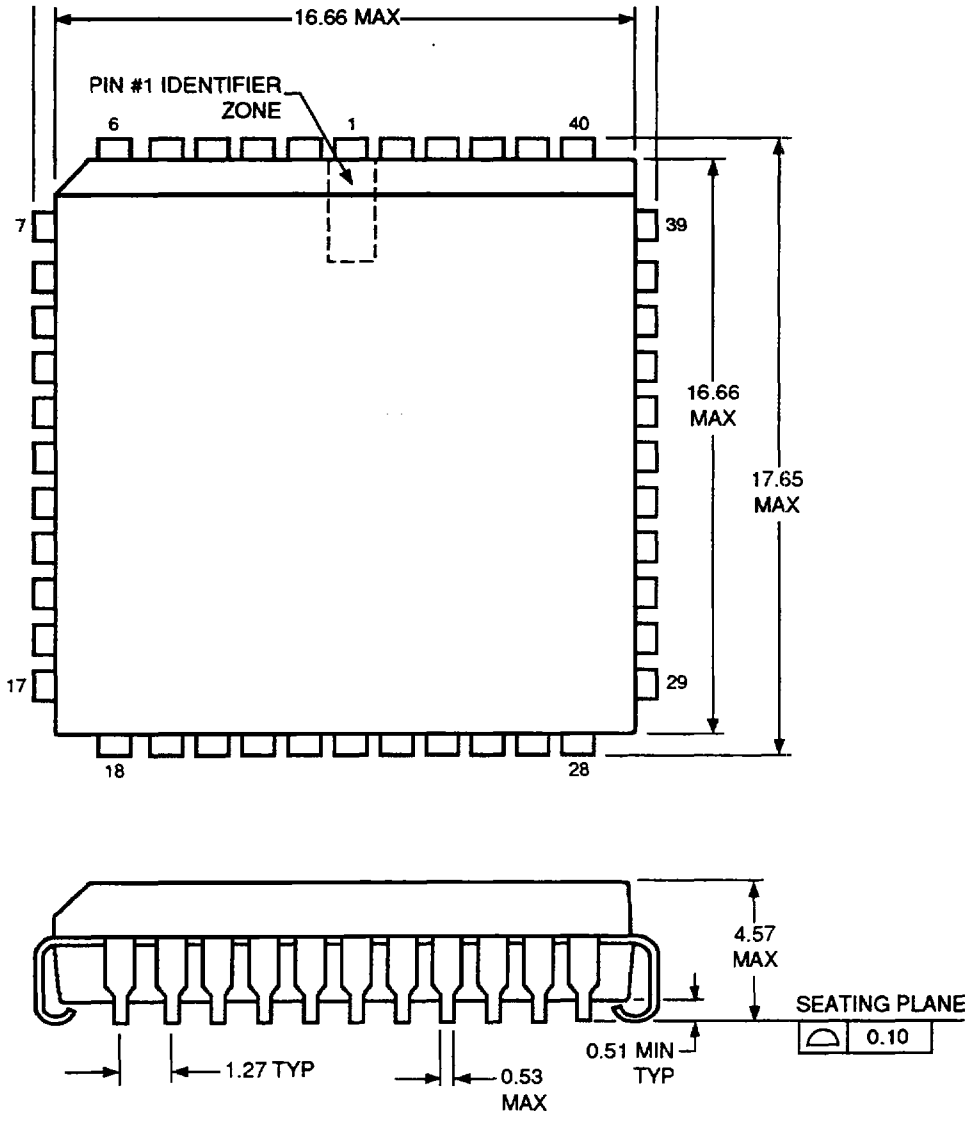
Propagation Delay

The maximum propagation delay from the S/T-interface to the U-interface (upstream direction) is 750 µs. The maximum propagation delay from the U-interface to the S/T-interface (downstream direction) is 550 µs.

Outline Diagram

44-Pin, PLCC

Controlling dimensions are in inches.



Ordering Information

Device Code	Package	Temperature
T-7234- - ML2	44-Pin PLCC	–40 °C to +85 °C

Questions and Answers

Introduction

This section is intended to answer questions that may arise when using the T7234 Single-Chip NT1 Transceiver.

The questions and answers are divided into three categories: U-interface, S/T-interface, and miscellaneous.

U-Interface

Q1: Is the line interface for the T7234 the same as for the T7264?

A1: Yes. The U-interface section on these chips is identical, so their line interfaces are also identical.

Q2: Can the T7234 be used with a transformer that has a magnetizing inductance of 20 mH?

A2: Yes.

Q3: Are the AT&T U-interface transformers available as surface-mount components?

A3: TBD.

Q4: The line interface components' specifications require 16.9 Ω resistors on the line side of the transformer when using the 2754H2. For our application, we would like to change this value. Can the U-interface line-side circuit be redesigned to change the value of the line-side resistors?

A4: Yes. For example, the line-side resistances can be reflected back to the device side of the transformer so that, instead of having 16.9 Ω on each side of the transformer, there are no resistors on the line side of the transformer and 24.4 Ω resistors on the device side (16.9 + $16.9/N^2$, where N is the turns ratio of the transformer). However, there may be a slight performance penalty in this case since the on-chip hybrid network is optimized for 16.9 Ω of resistance on the device side of the transformer.

Q5: The dc blocking capacitor specified is 1 µF. Can it be increased to at least 2 µF?

A5: This value can be increased to 2 µF without an effect on performance. However, for an NT1 to be compliant with T1.601-1992 Section 7.5.2.3, the dc blocking capacitor must be 1.0 µF ± 10%.

Q6: What is the purpose of the 3000 pF capacitors in the U-line interface figure in the data sheet?

A6: The capacitors are for common-mode noise rejection. The ANSI T1.601 specification contains no requirements on longitudinal noise immunity. Therefore, these capacitors are not required in order to meet the specification. However, there are guidelines in IEC 801-6 which suggest a noise immunity of up to 10 Vrms between 150 kHz and 250 MHz. At these levels, the 10 kHz tone detector in the T7234 may be desensitized such that tone detection is not guaranteed on long loops. The 3000 pF was selected to provide attenuation of this common-mode noise so that tone detector sensitivity is not adversely affected. Since the 3000 pF capacitor was selected based only on guidelines, it is not mandatory, but it is recommended in applications which may be susceptible to high levels of common-mode noise. The final decision depends on the specific application.

As for the size of the capacitors, lab tests indicate the following:

1. The performance of the system suffers no degradation until the values are increased to about 0.1 µF.
2. The return loss at 25 kHz increases with increasing capacitor value.
3. The capacitor value has no effect on longitudinal balance.
4. A large unbalance in the capacitor values did not affect return loss, longitudinal balance, or performance.

Questions and Answers (continued)

Q7: Are there any recommended common filtering parts for the U-interface? I suspect that our product may have emissions problems, and I want to include a provision for common-mode filtering on the U-interface.

A7: The only common-mode filtering parts we have any data on are two common-mode chokes from Pulse Engineering, (619) 674-8100, that are intended to help protect against external common-mode noise. The part numbers are PE-68654 (12.5 mH) and PE-68635 (4.7 mH), and in lab experiments, no noticeable degradation in transmission performance was observed. These chokes are typically effective in the frequency range 100 kHz—1 MHz.

As far as emissions are concerned, we don't have a lot of data. We have seen some success with the use of RJ-45 connectors that have integral ferrite beads such as those from Corcom, Inc., (708) 680-7400. These provide some flexibility in that they have the same footprint as some standard RJ-45 connectors.

Q8: I am planning on using a Raychem PTC (p/n TR600-150) on the U-interface of the T7234. The device is rated at 6 Ω—12 Ω. I plan on using this resistor and a 4.87 Ω resistor in place of one of the 16.9 Ω line side resistors. I am concerned about the loose tolerance on the PTC resistance. Will I be able to pass the return loss requirements in ANSI T1.601 Section 7.1?

A8: The NT1 impedance limits looking into tip/ring are derived from the T1.601 return loss requirements (Figure 19 in T1.601). At the narrowest point in the templates, the permissible range is between 111 Ω to 165 Ω. The tolerance on the PTC will reduce the impedance margin somewhat, but should still be acceptable.

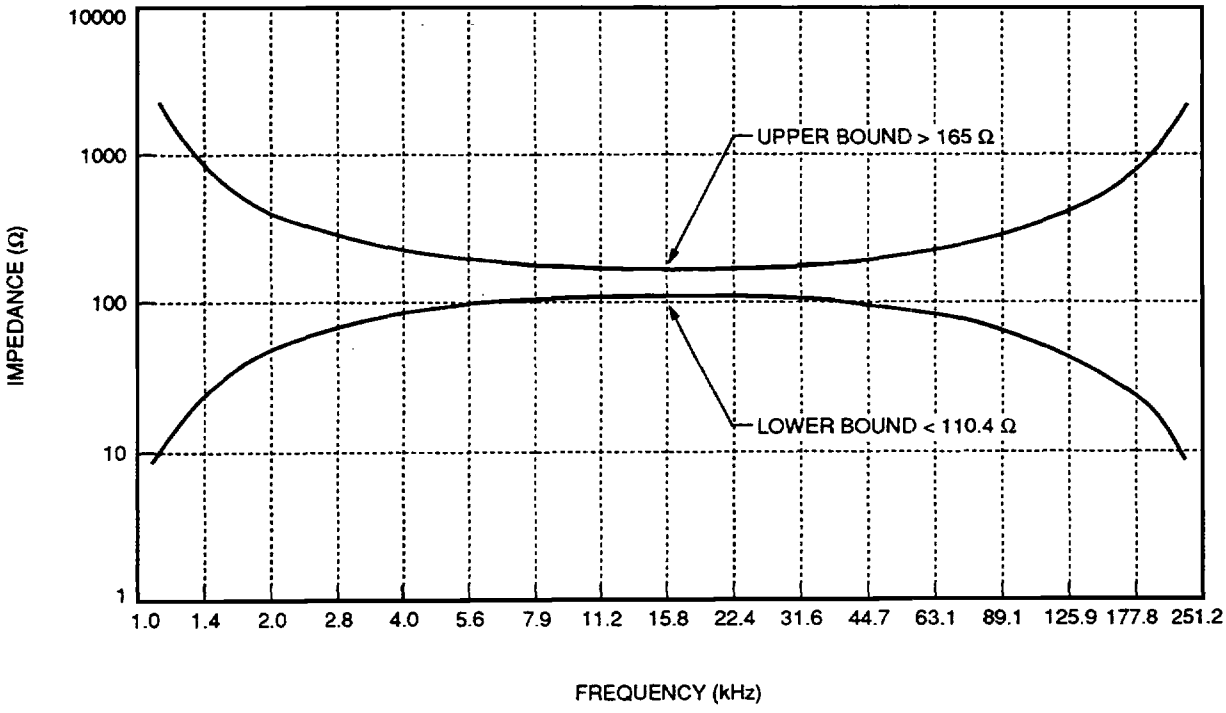


Figure 21. Transceiver Impedance Limits

Figure 21 is derived from the return loss template in ANSI T1.601. Return loss is a measure of the match between two impedances on either side of a junction point. The following equation is an expression of return loss in terms of the complex impedances of the two halves of the circuit Z_1, Z_2.

$$RL\ (dB) = 20 \log \left| \frac{Z_1 + Z_2}{Z_1 - Z_2} \right|$$

Questions and Answers (continued)

A8: (continued)

When the impedances are not matched, the junction becomes a reflection point. For a perfectly matched load, the return loss is infinite, whereas for an open or short circuit, the return loss is zero. The return loss expresses the ratio of incident to reflected signal power and should consequently be fairly high.

It is desirable to express the return loss in terms of impedance bounds, since an impedance measurement is relatively simple to make. From the above equation, upper and lower bounds on impedance magnitude can be derived as follows:

Z_O = Return Loss Reference Impedance = 135 Ω

Z_U = Upper Impedance Curve

Z_L = Lower Impedance Curve

Upper Bound ($Z_U > Z_O$):

$$RL\ (dB) = 20 \log \left| \frac{Z_O + Z_U}{Z_U - Z_O} \right|$$

Lower Bound ($Z_L < Z_O$):

$$RL\ (dB) = 20 \log \left| \frac{Z_O + Z_L}{Z_U - Z_L} \right|$$

Note that the higher the minimum return loss requirement, the tighter the impedance limits will be around Z_O, and vice versa.

So, for the upper bound, solve for Z_U:

$$Z_U = Z_O \frac{10^{\frac{RL}{20}} + 1}{10^{\frac{RL}{20}} - 1} = \left| Z_O \right| \frac{1 + 10^{\frac{-RL}{20}}}{1 - 10^{\frac{-RL}{20}}}$$

For the lower bound, solve for Z_L:

$$Z_L = Z_O \frac{10^{\frac{RL}{20}} - 1}{10^{\frac{RL}{20}} + 1} = \left| Z_O \right| \frac{1 - 10^{\frac{-RL}{20}}}{1 + 10^{\frac{-RL}{20}}}$$

Plotting the above equations (using 135 for Z_O and Figure 19 in T1.601 for the RL values) results in the graph shown in Figure 21, which shows the return loss expressed in terms of impedance upper and lower bounds.

Q9: Why must secondary protection, such as a *Motorola* SA6.0CA protection diode, be used?

A9: The purpose of the diode is to protect against metallic surges below the breakdown level of the primary protector.

Such metallic surges can be coupled through the transformer and could cause device damage if the currents are high. The protector does not provide absolute protection for the device, but it works in conjunction with the built-in protection on the device leads.

The breakdown voltage level for secondary protection devices must be chosen to be above the normal working voltage of the signal and typically below the breakdown voltage level of the next stage of protection. The SA6.0CA has a minimum breakdown voltage level of 6.7 V and a maximum breakdown voltage of 7.4 V (for detailed information, refer to the *Motorola TVS/ Zener Device* Data Book, # DL150/D, 1994).

The chip pins that the SA6.0CA protects are pins 36 (HP), 31 (HN), 32 (LOP), and 35 (LON). The 16.0 Ω resistors will help to protect pins 32 and 35, but pins 31 and 36 will be directly exposed to the voltage across the SA6.0CA. The on-chip protection on these pins consists of output diodes and a pair of polysilicon resistors. These pins have been thoroughly tested to ensure that a 7.4 V level will not damage them; therefore, no third level of protection is needed between the SA6.0CA and the HP and HN pins.

The SA6.0CA has a maximum reverse surge voltage level of 10.3 V at 48.5 A. Sustained currents this large on the device side of the transformer are not a concern in this application. Thus, there should never be more than 7.4 V across the SA6.0CA, except for possibly an ESD or lightning hit. In these cases, the T7234 is able to withstand at least ±1000 V (human-body model) on its pins.

Questions and Answers (continued)

Q10: Where can information be obtained on lightning and surge protection requirements for 2B1Q products?

A10: Requirements vary among applications and between countries. ANSI T1.601, Appendix B, provides a list of applicable specifications to which you may refer. Also, there are many manufacturers of overvoltage protection devices who are familiar with the specifications and would be willing to assist in surge protection design. The ITU-T K series recommendations are also a good source of information on protection, especially recommendation K.11, "Principles of Protection Against Overvoltages and Overcurrents," which presents an overview of protection principles. Also refer to the application notes mentioned in the U-interface Description section of this data sheet.

Q11: ITU-T specification K.21 describes a lightning surge test for NT1s (see Figure 1/K.21 and Table 1/K.21, Test #1) in which both Tip and Ring are connected to the source and a 1.5 kV voltage surge is applied between this point and the GND of the NT1. What are the protection considerations for this test? Are the HP and HN pins susceptible to damage?

A11: The critical component in this test is the transformer since its breakdown voltage must be greater than 1.5 kV. Assuming this is the case, the only voltage that will make it through to the secondary side of the transformer will be primarily due to the interwinding capacitance of the transformer coils. This capacitance will look like an impedance to the common-mode surge and will therefore limit current on the device side of the transformer. The device-side voltage will be clamped by the SA6.0CA device. The maximum breakdown voltage of the SA6.0CA is 7.4 V. The 16.9 Ω resistors will help protect the LOP and LON pins on the T7234 from this voltage. However, this voltage will be seen directly on pins 36 and 31 (HP and HN) on the T7234. The on-chip protection on these pins consists of output diodes and a pair of polysilicon resistors. These pins have been thoroughly tested to ensure that a 7.4 V level will not damage them; therefore, no third level of protection is needed between the SA6.0CA and the HP and HN pins.

Q12: Can the range of the T7234 on the U-interface be specified in terms of loss? What is the range over straight 24 AWG wire?

A12: ANSI Standard T1.601, Section 5.1, states that transceivers meeting the U-interface standard are intended to operate over cables up to the limits of 18 kft (5.5 km), 1300 Ω resistance design. Resistance design rules specify that a loop (of single- or mixed-gauge cable; e.g., 22 AWG, 24 AWG, and 26 AWG) should have a maximum dc resistance of 1300 Ω, a maximum working length of 18 kft, and a maximum total bridged tap length of 6 kft.

The standard states that, in terms of loss, this is equivalent to a maximum insertion loss of 42 dB @ 40 kHz. AT&T has found that, for assessing the condition of actual loops in the field in a 2B1Q system, specifying insertion loss as 33.4 dB @ 20 kHz more closely models ANSI circuit operation. This is equivalent to a straight 26 AWG cable with 1300 Ω dc resistance (15.6 kft).

The above goals are for actual loops in the outside loop plant. These loops may be subjected to noise and jitter. In addition, as mentioned above, there may be bridge taps at various points on the loop. The T1.601 standard defines 15 loops, plus the null, or 0 length loop, which are intended to represent a generic cross section of the actual loop plant.

A 2B1Q system must perform over all of these loops in the presence of impairments with an error rate of <1E-7. Loop #1 (18 kft, where 16.5 kft is 26 AWG cable and 1.5 kft is 24 AWG cable) is the longest, so it has the most loss (37.6 dB @ 20 kHz and 47.5 dB @ 40 kHz). Note that this is more loss than discussed in the preceding paragraph. The difference is based on test requirements vs. field deployment. The test requirements are somewhat more stringent than the field goal in order to provide some margin against severe impairments, complex bridged taps, etc.

Questions and Answers (continued)

A12: (continued)

If a transceiver can operate over Loop #1 error-free, it should have adequate range to meet all the other loops specified in T1.601. Loop #1 has no bridged taps, so passing Loop #1 does not guarantee that a transceiver will successfully start up on every loop. Also, due to the complex nature of 2B1Q transceiver start-up algorithms, there may be shorter loops which could cause start-up problems if the transceiver algorithm is not robust. The T7234 has been tested on all of the ANSI loops per the T1.601 standard and passes them all successfully. Two loops commonly used in the lab to evaluate the performance of the T7234 silicon are as follows:

Loop Configuration	Bridge Taps (BT)	Loss @ 20 kHz (dB)	Loss @ 40 kHz (dB)
18 kft 26 AWG	None	38.7	49.5
15 kft 26 AWG	2 at near end, each 3 kft 22 AWG	37.1	46.5

The T7234 is able to start up and operate error-free on both of these loops. Neither of these loops is specified in the ANSI standard, but both are useful for evaluation purposes. The first loop is used because it is simple to construct and easy to emulate using a lumped parameter cable model, and it is very similar to ANSI Loop #1, but the loss is slightly worse. Thus, if a transceiver can start up on this loop and operate error-free, its range will be adequate to meet the longest ANSI loop. The second loop is used because, due to its difficult bridge tap structure and its length, it stresses the transceiver start-up algorithms more than any of the ANSI-defined loops. Therefore, if a transceiver can start up on this loop, it should be able to meet any of the ANSI-defined loops which have bridge taps. Also, on a straight 26 AWG loop, the T7234 can successfully start up at lengths up to 21 kft. This fact, combined with reliable start-up on the 15 kft 2BT loop above, illustrates that the T7234 provides ample start-up sensitivity, loop range, and robustness on all ANSI loops.

Another parameter of interest is pulse height loss (PHL). PHL can be defined as the loss in dB of the peak of a 2B1Q pulse relative to a 0 length loop. For an 18 kft 26 AWG loop, the PHL is about 36 dB, which is 2 dB worse than on ANSI Loop #1. A signal-to-noise ratio (SNR) measurement can be performed on the received signal after all the signal processing is complete (i.e., at the input to the slicer in the decision feedback equalizer). This is a measure of the ratio of the recovered 2B1Q pulse height vs. the noise remaining on the signal. The SNR must be greater than 22 dB in order to operate with a bit error rate of <1E-7. With no impairments, the T7234 SNR is typically 32 dB on the 18 kft/26 AWG loop. When all ANSI-specified impairments are added, the SNR is about 22.7 dB, still leaving adequate margin to guarantee error-free operation over all ANSI loops.

Finally, to estimate range over straight 24 AWG cable, the 18 kft loop loss can be used as a limit (since the T7234 can operate successfully with that amount of loss) and the following calculations can be made:

Loss of 18 kft 26 AWG loop @ 20 kHz	38.7 dB
Loss per kft of 24 AWG cable @ 20 kHz	1.6 dB

$$\frac{38.7\ \text{dB}}{1.6\ \text{dB/kft}} = 24\ \text{kft}$$

Thus, the operating range over 24 AWG cable is expected to be about 24 kft.

Q13: What cable simulator is used for evaluating the T7234 U-interface?

A13: Real cable is used for ANSI loop performance measurements. We have evaluated several commercial cable simulators, but were not satisfied with their accuracy in loop emulation and impairments generation.

Q14: What does the energy spectrum of a 2B1Q signal look like?

A14: Figure A1 (curve P1) in the ANSI T1.601 standard illustrates what this spectrum looks like.

Questions and Answers (continued)

Q15: Please clarify the meaning of ANSI Standard T1.601, Section 7.4.2, Jitter Requirement #3.

A15: The intent of this requirement is to ensure that after a deactivation and subsequent activation attempt (warm start), the phase of the receive and transmit signals at the NT will be within the specified limits relative to what they were prior to deactivation. This is needed so that the LT, upon a warm-start attempt, can make an accurate assumption about the phase of the incoming NT signal with respect to its transmit signal. Note that the T7234 meets this requirement by design because the NT phase offset from transmit to receive is always fixed.

Q16: I need a way to generate a scrambled 2B1Q data stream from the T7234 for test purposes (e.g., ANSI T1.601 section 5.3.2.2, total power and section 7.2, longitudinal output voltage). How can I do this?

A16: A scrambled 2B1Q data stream (the "SN1" signal described in ANSI T1.601 Table 5) can be generated by pulling ILOSS (pin 6) low on the T7234.

Q17: We are trying to do a return loss measurement on the U-interface of the T7234 per ANSI T1.601 section 7.1. We are using a circuit similar to the one you recommend in the data sheet. We have observed the following. When the chip is in IDLE mode (powered on but no activity on the U- or S/T-interfaces), the return loss is very low, i.e., the termination impedance appears to be very large relative to 135 Ω and falls outside the boundaries of Figure 19 of ANSI T1.601. However, if we inject a 10 kHz tone before making a measurement, the return loss falls within the template. Why is it necessary to inject the 10 kHz tone in order to get this test to pass? Shouldn't a 135 Ω impedance be presented to the network regardless of the state of the T7234 once it is powered on?

A17: The return loss is only relevant when the transmitter section is powered on. When the transmitter is powered, it presents a low-impedance output to the U-interface. The transmitter must be held in this low-impedance state when the return loss *and* longitudinal balance tests are performed. This can be accomplished by pulling RESET low (pin 43). In the RESET state, the transmitter is held in a low impedance state and not able to transmit, and won't respond to any incoming wake-up tones. This is different than the IDLE state that the chip enters after power on or deactivation. In IDLE, the transmitter is powered down and in a high-impedance state, with only the tone detector powered on and looking for a far-end wake-up tone. The transmitter powers down when in IDLE state to save power and maximize the tone detector sensitivity. The reason that the chip behaves as it does in your tests is that your test begins with the transmitter in its IDLE state, causing the return loss to be very low. If a 10 kHz signal is applied, the tone detector senses the applied signal and triggers. This causes the transmitter to enter its low-impedance state, where it will remain until the T7234 start-up state machine times out (typically 480 ms for this case due to Loss of Signal > 480 ms, see Table C1 State H4 in ANSI T1.601).

Q18: Is there some way to generate single U-interface pulses from the T7234 for pulse template testing?

A18: This is possible, but only with an external test board that AT&T-ME is willing to lend to customers for conformance test purposes. This board is called the SPEC (Single Pulse Eye Control) board, and supports several test modes. It will produce a single U-interface pulse of programmable magnitude and polarity every 125 µs. The SPEC board also supports reading and writing of T7234 registers and can display the eye pattern of the received data. If you intend to use this board, please request a copy of the SPEC manual. It explains which T7234 signals must be made available on your product in order to interface to this board, and which signals should not be tied directly to ground or Vcc. The SPEC manual also contains enough schematic and software information to allow you to produce your own version of this board.

Questions and Answers (continued)

Q19: What are the average cold start and warm start times?

A19: Lab measurements have shown the average cold start time to be about 3.3 s—4.2 s over all loop lengths, and the average warm start time to be around 125 ms—190 ms over all loop lengths.

Q20: What is the U-interface's response time to an incoming wake-up tone from the LT?

A20: Response time is about 1 ms.

Q21: What is the minimum time for a U-interface reframe after a momentary (<480 ms) loss of synchronization?

A21: Five superframes (60 ms).

Q22: Where is the U-interface loopback 2 (i.e., eoc 2B+D loopback) performed in the T7234?

A22: It is performed just inside the chip at the S/T-interface. The S/T receiver is disconnected internally from the chip pins, and the S/T transmit signal is looped back to the receiver inputs so the S/T section synchronizes to its own signal. This ensures that as much of the data path as possible is being tested during the 2B+D loopback.

Q23: Are the embedded operations channel (eoc) initiated B1 and B2 channel loopbacks transparent?

A23: Yes, the B1 and B2 channel loopbacks are transparent, as is the 2B+D loopback.

Q24: How can proprietary messages be passed across the U-interface?

A24: The embedded operations channel (eoc) provides one way of doing this. ANSI standard T1.601 defines 64 8-bit messages which can be used for nonstandard applications. They range in value from binary 00010000 to 01000000.

There is also a provision for sending bulk data over the eoc. Setting the data/message indicator bit to 0 indicates the current 8-bit eoc word contains data that is to be passed transparently without being acted on. Note that there is no response time requirement placed on the NT in this case (i.e., the NT does not have to echo the message back to the LT). Also note that this is currently only an ANSI provision and is not an ANSI requirement. The T7234 does support this provision.

Q25: What is the value of the ANSI T1.601 cso and nib bits in the 2B1Q frame?

A25: cso and nib are fixed at 0 and 1, respectively, by the device. This is because the device always has warm start capability (CSO = 0), and NT1s are required to have nib = 1 per T1.601-1992.

Q26: It looks like the U-interface sai and act bits that the T7234 transmits towards the LT always track one another. If this is the case, I don't understand why they are both needed. Can you explain the purpose of the sai bit and how it relates to the act bit?

A26: The sai bit is equal to 1 when there is activity (INFO 1 or INFO 3) on the S/T-interface. The act bit is 1 whenever layer 1 transparency is established. Most of the time these bits are the same, but there are two situations where they will be different.

1. The sai bit can be used in conjunction with the uoa bit from the LT to support DSL-only activation as described in the ANSI and ETSI standards. The LT can request a U-only activation by setting uoa =0, which will cause the S/T-interface to remain in a deactivated state. If the TE requests an activation under these conditions by transmitting INFO 1 to the T7234, the sai bit will change from 0 to 1, indicating to the LT that there is activity on the S/T-interface so that the LT can respond accordingly. Typically, this means that LT will set uoa = 1 to exit the DSL-only condition so that layer 1 transparency can be established from TE to LT. Thus, in the case of a DSL-only activation, the T7234's sai bit is 1 and its act bit is 0 from the time a TE requests an activation until the following events occur:
   A. LT sets uoa = 1 towards the NT.
   B. The T7234 detects uoa = 1 and transmits INFO 2 on the S/T-interface.
   C. The TE synchronizes and transmits INFO 3 on the S/T-interface.
   D. Upon reception of the INFO 3 signal, the T7234 sets act = 1.

Questions and Answers (continued)

A26: (continued)

2. If a link is fully active, then the LT detects a transition of the NT act bit from 1 to 0, and it is an indication of loss of layer-1 transparency. This can be caused by either a) S/T loss of sync or b) NT1 received INFO 0. Case a) will result in an act = 0 / sai = 1 combination, i.e., S/T sync is lost but there is still activity on the S/T-interface, meaning the TE is having trouble staying synchronized. Case b) will result in an act = 0 / sai = 0 combination, i.e., no activity on the S/T-interface (INFO 0), meaning the TE has been disconnected. There is no way the TE can legally send INFO 0 when the link is fully active because the TE is not allowed to initiate deactivation—only the LT is—so the only other possibility is that it has been disconnected or has failed. Note that this procedure allows the CO to determine whether the cause of loss of layer 1 transparency is a TE that is having synchronization problems or a TE that has been disconnected, based on the state of the sai bit when act = 0.

The ANSI T1.601 and ETSI DTR/TM 3002 standards contain finite state matrices that describe DSL-only operation. The T7234 follows the behavior described in the matrices. Refer to those tables for detailed information on each of the states.

S/T-Interface

Q27: What is the S/T transformer's inductance?

A27: For AT&T transformers 2768A or 2776, a minimum inductance of 22 mH is guaranteed.

Q28: Can the S/T-interface leads be short-circuited together without harming the device?

A28: Yes, this will not cause any harm to the device.

Q29: What is the common-mode rejection of the S/T receiver?

A29: The common-mode rejection of the S/T receiver is 400 mV. Refer to the Electrical Characteristics described in the data sheet.

Q30: I notice that the Application Note entitled *Design an S/T Line Interface Circuitry Using the T7250C/T7259* recommends relays on both the transmitter and receiver outputs that disconnect the device when power is removed from the chip. Is this necessary for an NT using the T7234?

A30: The relay on the TE transmitter output is necessary to pass the peak current test (ITU-T I.430 Section 8.5.1.2 and ANSI T1.605-1991, section 9.5.1.2) when the TE is powered down. For the NT, there is no equivalent test, so the relay is not necessary. The relay on the TE receiver input is also necessary to pass the peak current test (ITU-T I.430 sections 8.5.1.2 and 8.6.1.1, and ANSI T1.605-1991 sections 9.5.1.2 and 9.6.1.1). For the NT, however, there is enough margin in the line interface capacitance circuitry such that the peak current requirement (ITU-T I.430 section 8.6.1.2 and ANSI T1.605-1991 section 9.6.1.2) can be met without using relays. This assumes, of course, that sound layout practices have been applied to keep parasitic capacitance of the line interface circuitry to a minimum (of primary importance is making sure there is no ground plane under the S/T line interface). The reason the TE needs a relay on its receiver is that the TE tests assume a 350 pF cord connected to the line, and this extra capacitance can cause the peak current requirement to be exceeded. So even though the NT peak current requirement is slightly more stringent (0.5 mA as opposed to 0.6 mA), the TE peak current test is the most difficult to meet due to the 350 pF cord capacitance.

Q31: The T7234 reference design in Figure 6 shows 100 Ω termination resistors in parallel with a second pair of optional 100 Ω resistors that can be inserted or removed by installing/removing jumpers from JMP1 and JMP2. What is the purpose of this second pair of resistors?

A31: Typically, a TE or group of TEs connected to an NT1 will have a 100 Ω termination located at the interface point of the TE farthest from the NT1 (refer to ITU-T I.430 Figure 2 and section 4 or T1.605 Figure 2 and section 5). However, in some cases it may be desirable to operate an NT1 with a TE that does not provide the 100 Ω termination impedance. In this case, the provisional 100 Ω resistors shown in Figure 6 may be installed to provide the extra termination impedance required.

Questions and Answers (continued)

Q32: I would like to integrate an NT1 onto my T7250C-based 4-wire ISDN product. Is there a way I can avoid having to use two sets of S/T transformers, protection diodes, etc., to convert the S/T-interface (i.e., one set on the T7250C and one set on the T7234)?

A32: If no external S/T-interface connection is required, the T7250C and T7234 can be directly connected as shown in the following diagram. If it is required to be able to connect an external TE, the circuit shown in Figure 22 can be used.

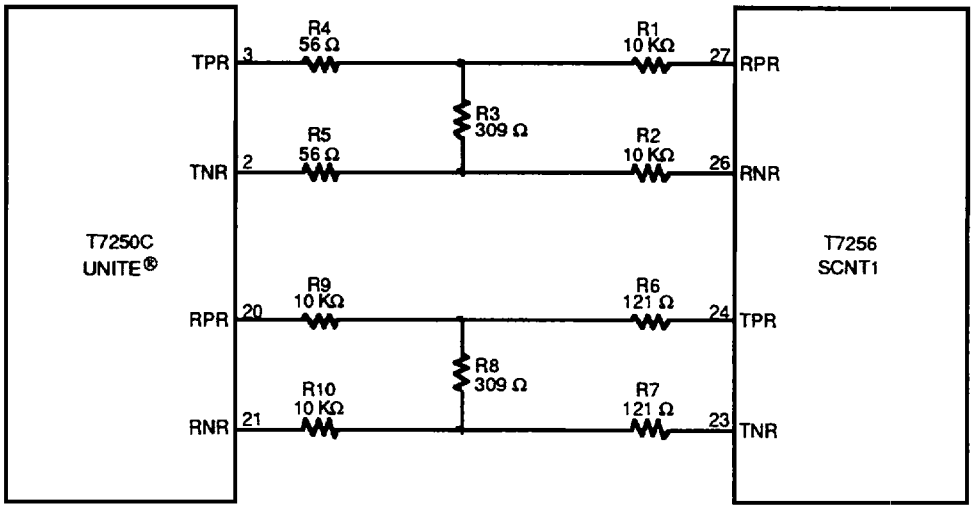


Figure 22. T7234 to T7250C Direct Connection

Q33: In the Analog Interface section of the S/T-interface Description in the data sheet, where does the value of 0 ms — 3.1 ms max. differential delay in adaptive timing mode come from?

A33: The minimum value of 0 ms is necessary so that the NT's transmitter and receiver can be directly connected in a loopback and still synchronize.

The maximum value of 3.1 ms comes about because the "window" size needed in the adaptive timing algorithm is 2.1 ms. The window size is the time during each bit period in which no transitions may occur. Since a period is 5.2 ms, the time during which there may be transitions is 5.2 ms – 2.1 ms, or 3.1 ms. This is the same as the maximum differential delay, since the earliest and latest bit transitions represent the nearest and farthest TEs relative to the NT receiver.

Miscellaneous

Q34: Is the ±100 ppm free-run frequency recommendation met in the T7234?

A34: In the free-run mode, the output frequency is primarily dependent on the crystal, not the silicon design. For low-cost crystals, initial tolerance, temperature, and aging effects may account for two-thirds of this budget, and just a couple of pF of variation in load capacitance will use up the rest; therefore, the ±100 ppm goal can be met if the crystal parameters are well controlled. See the Crystal Characteristics section in the data sheet.

Questions and Answers (continued)

Q35: It has been noted in some other designs that the crystal has a capacitor from each pin to ground. Changing these capacitances allows the frequency to be adjusted to compensate for board parasitics. Can this be done with the T7234 crystal? Also, can we use a crystal from our own manufacturer?

A35: The crystal for the T7234 is tuned to a particular load capacitance that does not include external capacitors. The advantage to this is that no external components are required. The disadvantage is that board parasitics must be very small. The crystal characteristics section of the data sheet notes that the board parasitics must be within the range of 0.6 pF ± 0.4 pF. AT&T does not require that a particular crystal be used, but we strongly recommend adhering to the crystal parameters specified in the data sheet. A crystal which deviates from these parameters may work under most conditions, but we cannot guarantee that it will start up and/or meet the ±100 ppm requirement under all operating conditions.

Q36: What clocks are available on the T7234?

A36: The following clocks are available:

1. SYN8K, pin 4 (8 kHz clock) is enabled by holding SDI (pin 12) low during an external RESET.
2. TDMCLK, pin 9 (2.048 MHz clock) is enabled by writing TDMEN = 0 (register GR2, bit 5).
3. CKOUT, pin 17 (10.24 MHz or 15.36011 MHz clock) is enabled by writing register GRO bit 2 or 1, respectively, to 0. Normally tristated.

Note that using clocks 2 or 3 above requires a microprocessor for setting the appropriate configuration.

Q37: I plan to program the T7234 to output 15.36 MHz from its CKOUT pin. Is this clock a buffered version of the 15.36 MHz oscillator clock? I am concerned that if it is not buffered, the capacitive loading on this pin could affect the system clock frequency.

A37: The 15.36 MHz output is a buffered version of the XTAL clock and therefore hanging capacitance on it will not affect the T7234's system clock frequency.

Q38: Can the T7234 operate with an external 15.36011 MHz clock source instead of using a crystal?

A38: No.

Q39: What is the effect of ramping down the power supply voltage on the device? When will it provide a valid reset? This condition can occur when a line-powered NT1's line cord is repeatedly plugged in and removed and plugged in again before the power supply has had enough time to fully ramp up.

A39: The device's reset is more dependent on the RESET pin than the power supply to the device. As long as the proper input conditions on the RESET pin (see Table 14) are met, the device will have a valid reset. Note that this input is a Schmitt-trigger input.

Q40: Is there a recommended method for powering the T7234? For example, is it desirable to separate the power supplies, etc.?

A40: The T7234 is not extremely sensitive to power supply schemes. Following standard practices of decoupling power supplies close to the chip and, if power and ground planes are not used, keeping power traces away from high-frequency signals, etc., should yield acceptable results. Separating the T7234 analog power supplies from the digital power supplies near the chip may yield a small improvement, and the same holds true for using power and ground planes vs. discrete traces.

Note that if analog and digital power supplies are separated, the crystal power supply (V_{DDO}) should be tied to the digital supplies (V_{DDD}).

Q41: What are the filter characteristics of the PLL at the NT?

A41: The –3 dB frequency is approximately 5 Hz; peaking is about 1.2 dB.

Q42: Can the T7234 operate in the LT mode?

A42: No, the T7234 is optimized for the NT side of the loop and cannot operate in the LT mode.

Questions and Answers (continued)

Q43: Can you provide detailed information on the active and idle power consumption of the T7234?

A43: The IDLE power of the T7234 is typically 35 mW. The IDLE power will be increased if CKOUT or the TDM highway are active. The discussion below presents accurate numbers for adding in the effects of CKOUT and the TDM highway.

When considering active power measurement figures, it is important to note that the conditions under which power measurements are made are not always completely stated by 2B1Q IC vendors. For example, loop length is not typically mentioned in the context of power dissipation, yet power dissipation on a short loop is noticeably greater than on a long loop. There are two reasons for the increased power dissipation at shorter loop lengths:

1. The overall loop impedance is smaller, requiring a higher current to drive the loop.
2. The far-end transceiver is closer, requiring the near-end transceiver to sink more far-end current in order to maintain a virtual ground at its transmitter outputs.

The following lab measurements provide an example of how power dissipation varies with loop length for a specific T7234 with its 15.36011 MHz CKOUT output disabled (see the following table for information on CKOUT). Note that power dissipation on a 0 length loop (the worst-case loop) is about 35 mW higher than on a loop of >3 kft length—a significant difference. Thus, loop length needs to be considered when determining worst-case power numbers.

Loop Configuration	Power (mW)
18 kft/26 AWG	270
6 kft/26 AWG	270
3 kft/26 AWG	274
2 kft/26 AWG	277
1 kft/26 AWG	285
0.5 kft/26 AWG	293
0 kft	305
135 Ω load, $\overline{\text{ILOSS}}$ or lpbk active, no far-end transceiver*	278

* This is the configuration used by some IC manufacturers.

Also, in the case of the T7234, the use of the output clock CKOUT (pin 17) needs to be considered since its influence on power dissipation is significant. Some applications may make use of this clock, while others may leave it tristated. The power dissipation of CKOUT is as follows:

CKOUT Frequency (MHz)	Power Due to CKOUT 40 pF Load (mW)	Power Due to CKOUT No Load (mW)
15.36011	21.3	11.0
10.24	17.7	9.1

Another factor influencing power consumption is the S/T-interface data pattern. For example, when transmitting an INFO 4 pattern with all 1s data in the B and D channels, the power consumption is 25 mW lower than it is when transmitting INFO 2, because INFO 2 is worst-case in terms of the amount of +0 and –0 transitions, and INFO 4 is best-case if the data is all 1s. A typical number would lie about midway between these two. The T7234 TDM highway, when active, can add another 3 mW of power.

Therefore, it is apparent that the conditions under which power is measured must be clearly specified. The methods AT&T has used to evaluate typical and worst-case power consumption are based on our commitment to provide our customers with accurate and reliable data. Measurements are performed as part of the factory test procedure using automated test equipment. Bench top tests are performed in actual T7234-based systems to correlate the automated test data with an actual implementation. A conservative margin is then added to the test results for publication in our data sheets.

Questions and Answers (continued)

A43: (continued)

The following table provides power consumption data for several scenarios so that knowledgeable customers can fairly compare transceiver solutions. A baseline scenario is presented in the Case 1 column, and then adders are listed in the Cases 2—6 columns to account for the worst-case condition listed in each column so that an accurate worst-case figure can be determined based on the conditions that are present in a particular application. Note that the tests were run at 5 V, so changes in the supply voltage will change the power accordingly.

Table 15. Power Consumption

Variables	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
Loop Configuration	>3 kft, 26 AWG	0 kft*	—	—	—	—
S/T State	INFO 4 with all 1s data	—	INFO 2†	—	—	—
CKOUT, MHz (40 pF load)‡	Tristated	—	—	15.36011	—	—
Temperature (°C)	25	—	—	—	85	—
Max. Power Consumption (mW)	277	35	25	22	5	3

* Some 2B1Q silicon vendors specify power using a configuration in which the IC is active and transmitting into a 135 Ω termination, with no far-end transmitter attached. This configuration would cause an increase of 9 mW over the Case 1 column, instead of the 35 mW shown here. This highlights the importance of specifying measurement conditions accurately when making comparisons between chip vendors' power numbers.

† This is a worst-case number representing the state of the S/T-interface where the most +0/–0 transitions occur. In a real application, this will be a transient state, as INFO 4 will occur as soon as synchronization is achieved. The average power consumed during a typical INFO 4, assuming a 50% mix of 1s and 0s in the B and D channels, would be approximately half this number, or 12.5 mW.

‡ See the preceding table for a comparison of power dissipation with negligible capacitive loading on CKOUT. The 40 pF figure chosen here is intended to represent a worst-case condition.

Q44: What would cause the STLED indicator to flash sporadically at an 11 Hz rate?

A44: If the T7234 S/T-interface is operating over a long loop that is outside the range specified in the I.430/T1.605 standard, the T7234 may go into a state where it is constantly going in and out of synchronization. This causes it to cycle between ANSI states H7 and H8, producing STLED state changes between 1 Hz flashing and always on. When the S/T-interface loses synchronization, it takes about 96 ms before synchronization can be reacquired. This 96 ms cycle, coupled with the STLED switching from always on to 1 Hz flashing, can appear as 11 Hz or sporadic flashing, depending on how frequently S/T synchronization is being lost.

Either of these states could cause potential confusion to maintenance personnel in the event that a T7234-based NT1 is connected to an S/T loop that is longer than permitted by the standards. For example, an 11 Hz rate is difficult to visually distinguish from the 8 Hz rate, but the 11 Hz case indicates a problem on the S/T-interface and the 8 Hz case indicates a problem on the U-interface. To troubleshoot the STLED indication, unplug the S/T connector and repower the T7234 and initiate a start-up on the U-interface. If there is no problem on the U-interface, the STLED will reach a 1 Hz flashing state and remain there, indicating that the fast flashing was a result of S/T-interface problems.

Questions and Answers (continued)

Q45: The STLED on my T7234-based NT1 behaves in an unexpected way. When a start-up attempt is received, it flashes at an 8 Hz rate. Then it flashes briefly at 1 Hz, indicating synchronization on the U-interface. This is expected. However, after this, it starts flashing at 8 Hz, and yet it appears as though the system is operating fine (data is being passed end to end, etc.). Shouldn't the STLED signal be always low (i.e., ON) at this point?

A45: Yes it should. Referring to the STLED Control Flow diagram in Figure 15 of the data sheet, it appears as though you may be receiving aib = 0 from the upstream U-interface element. This will cause the behavior you are seeing.

Q46: When I try to activate our T7234-based NT1, it appears as though the U-interface is synchronizing (i.e., STLED flashes at 1 Hz), but the S/T-interface won't activate, and there is not even any signal activity on the S/T-interface (i.e., no INFO 1 or INFO 2). What might the problem be?

A46: The behavior you have observed can be caused if the uoa bit received on the U-interface from the network is set to 0. This causes the T7234 to activate the U-interface only, keeping the S/T-interface quiet, per the ANSI and ETSI standards. We have heard of some network equipment that incorrectly sets this bit low.

Standards Documentation

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.)

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
FAX: 212-302-1286

AT&T Publications

AT&T Customer Information Center (CIC)

Tel: 800-432-6600
FAX: 800-566-9568 (In U.S.A.)
FAX: 317-322-6484 (Outside U.S.A.)

Bellcore (U.S.A.)

Bellcore Customer Service
8 Corporate Plaza
Piscataway, New Jersey 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
FAX: 212-302-1286

ITU-T

International Telecommunication Union-Telecommunication Sector
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
FAX: 41-22-730-5991

ETSI

European Telecommunications Standards Institute
BP 152
F-06561 Valbonne Cedex, France

Tel: 33-92-94-42-00
FAX: 33-93-65-47-16

TTC (Japan)

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsucho-Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
FAX: 81-3-3432-1553

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