

# **HA13524/S/FP**

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## **Voice Coil Motor Driver**

The HA13524/S/FP are VCM driver for HDD and have following functions and features.

### **Functions**

- Input amp
- 4 A BTL output amp(HA13524/S)
- 2 A BTL output amp(HA13524FP)
- Retract circuit
- Independent OP amp
- OTSD & LVI

### **Features**

- Low saturation voltage
- No cross-over distortion
- Few external components
- Wide gain bandwidth

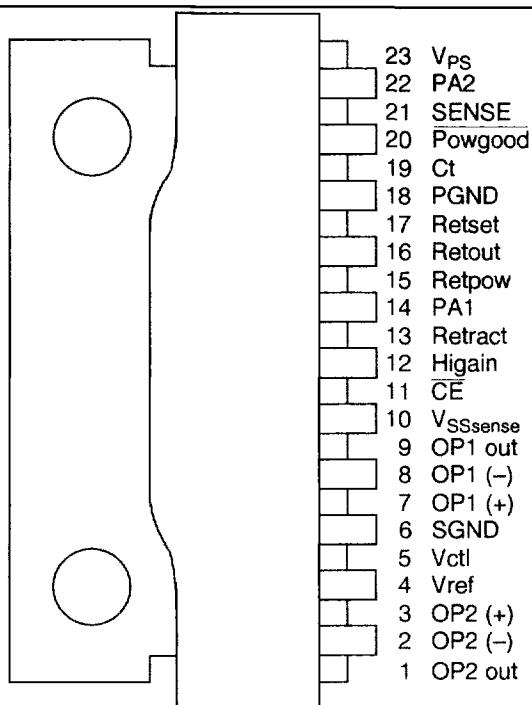
### **Ordering Information**

Type No	Package
HA13524	SP-23TA
HA13524S	SP-23TD
HA13524FP	FP-26DT

# HA13524/S/FP

## Pin Arrangement

• HA13524/S



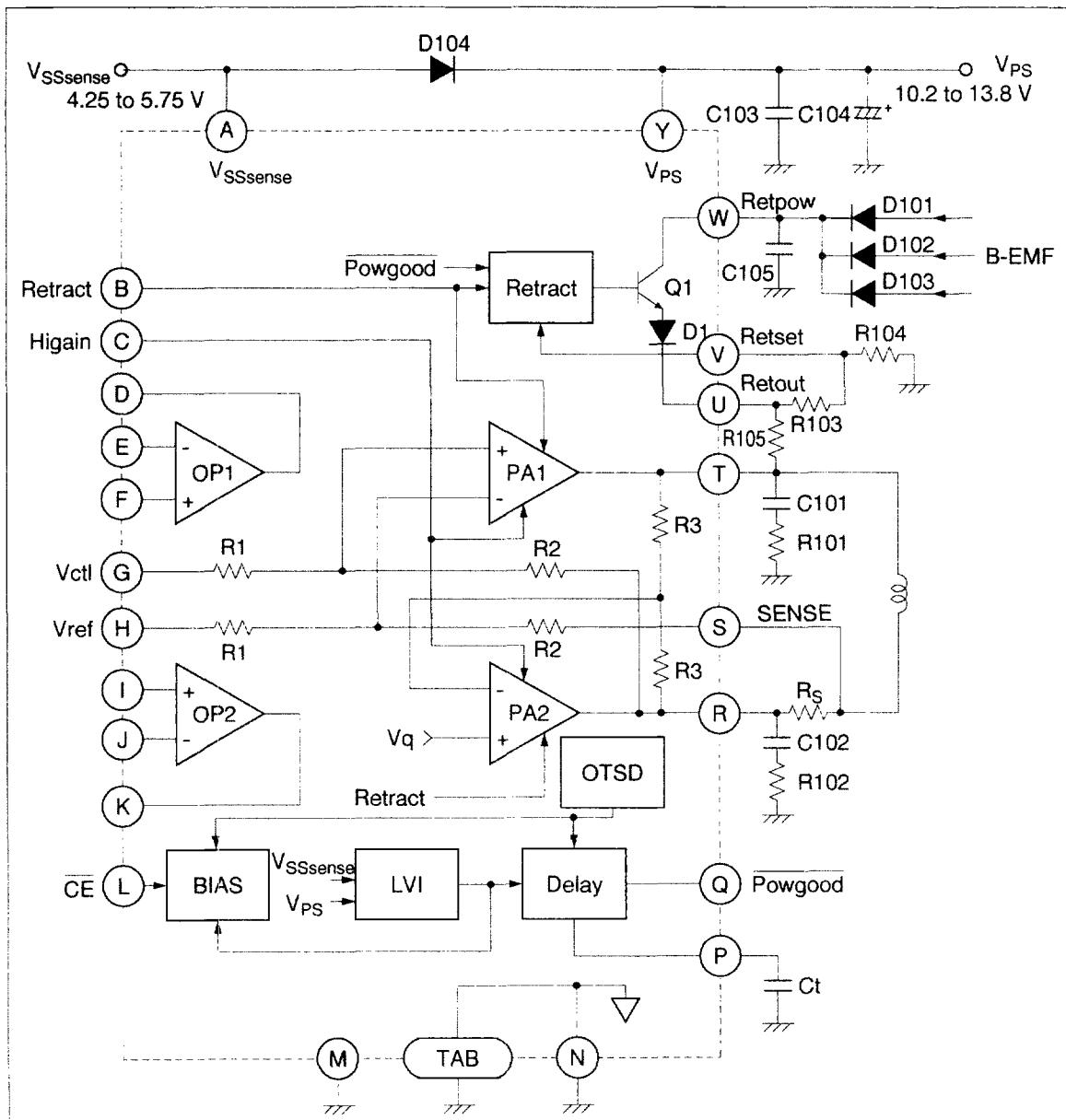
(Top view)

• HA13524FP

NC	1	26	V <sub>PS</sub>
OP2 out	2	25	NC
OP2 (-)	3	24	Powgood
OP2 (+)	4	23	PA2
Vref	5	22	SENSE
Vctl	6	21	Ct
GND	7	20	GND
GND	TAB	TAB	GND
OP1 (+)	8	19	Retout
OP1 (-)	9	18	NC
OP1 out	10	17	PA1
V <sub>SSsense</sub>	11	16	Retpow
CE	12	15	Retset
Higain	13	14	Retract

(Top view)

## Block Diagram



# HA13524/S/FP

## Truth Table

Input				Output				
<b>V<sub>PS</sub></b>	<b>V<sub>Ssense</sub></b>	<b>Retract</b>	<b>CE</b>	<b>Higain</b>	<b>PA1</b>	<b>PA2</b>	<b>Retout</b>	<b>Powgood</b>
0 to 7 V	X <sup>*1</sup>	X	X	X	Disable	L	Vret <sup>*2</sup>	Z
≤Vsd <sup>*3</sup>	≤Vsd <sup>*3</sup>	X	X	X	Disable	L	Vret	Z
≤Vsd	> Vsd							
> Vsd	≤ Vsd							
> Vsd		H	X	X	Disable	L	Vret	Z
		L	H	X	Disable	Disable	Z	Z
		L	H		High gain	High gain	Z	L
		L		Low gain	Low gain	Z	L	
(T <sub>j</sub> > T <sub>sd</sub> )				Disable	L	Vret	Z	

Notes:

- 1. X = Irrelevant
- 2. See external components
- H = High voltage level
- 3. See electrical characteristics
- L = Low voltage level
- Z = High impedance

**External Component**

Parts No.	Recommended value	Purpose	Notes
R101, R102	2.2 Ω	For power amplifire output stabilization	
R103, R104	—	For retract voltage setting	1
R105	—	For retract current setting	1
R <sub>S</sub>	≥ 0.1 Ω	Power amplifire output current detection	2
C101, C102	0.1 μF	For power amplifire output stabilization	
C103	≥ 0.1 μF	Power supply stabilization	
C104	≥ 4.7 μF	Power supply stabilization	
C105	≥ 0.1 μF	For power amplifire output stabilization	
Ct	≤ 0.1 μF	Powgood delay time setting	3
D101, D102, D103	V <sub>F</sub> < 0.8 V (@ I <sub>F</sub> = 1 A)	For retract	
D104	V <sub>F</sub> < 0.75 V (@ I <sub>F</sub> = 0.5 A)	V <sub>SSsense</sub> pin protection	4

Notes: 1. The retract voltage Vretout and current Iret are determined as follows.

$$V_{retout} = V_{retset} \left( 1 + \frac{R_{103}}{R_{104}} \right)$$

$$I_{ret} = \frac{V_{retout} - V_{satL}}{R_L + R_S + R_{105}}$$

Where,

R<sub>L</sub> = Load resistance

Vretset = Reference voltage for retract (See electrical characteristics)

V<sub>satL</sub> = Lo side saturation voltage of PA2 (See electrical characteristics)

2. The relationship between output current I<sub>O</sub> and input voltage Vctl is determined as follows.

$$I_O = \frac{(V_{ctl} - V_{ref}) G_{ctl}}{R_S} = \frac{(V_{ctl} - V_{ref}) g_m \cdot R'_S}{R_S}$$

Where,

G<sub>ctl</sub> = g<sub>m</sub> · R'<sub>S</sub> (See electrical characteristics)

V<sub>ref</sub> = Reference voltage for PA1

3. The Powgood delay time tpor is determined as follows.

t<sub>porhl</sub> = C<sub>t</sub> · V<sub>th</sub> / I<sub>cha</sub>

t<sub>porlh</sub> ≤ C<sub>t</sub> (V<sub>PS</sub> - V<sub>th</sub>) / I<sub>dis</sub>

Where,

I<sub>cha</sub> & I<sub>dis</sub> = Charge & discharge current for pin Ct (See electrical characteristics)

V<sub>th</sub> = Threshold voltage of pin Ct (See electrical characteristics)

4. D104 is unnecessary when V<sub>SSsense</sub> Terminal is not used. In this case, connect V<sub>ps</sub>.

5. Unused input terminals of OP1 and OP2 connect to GND.

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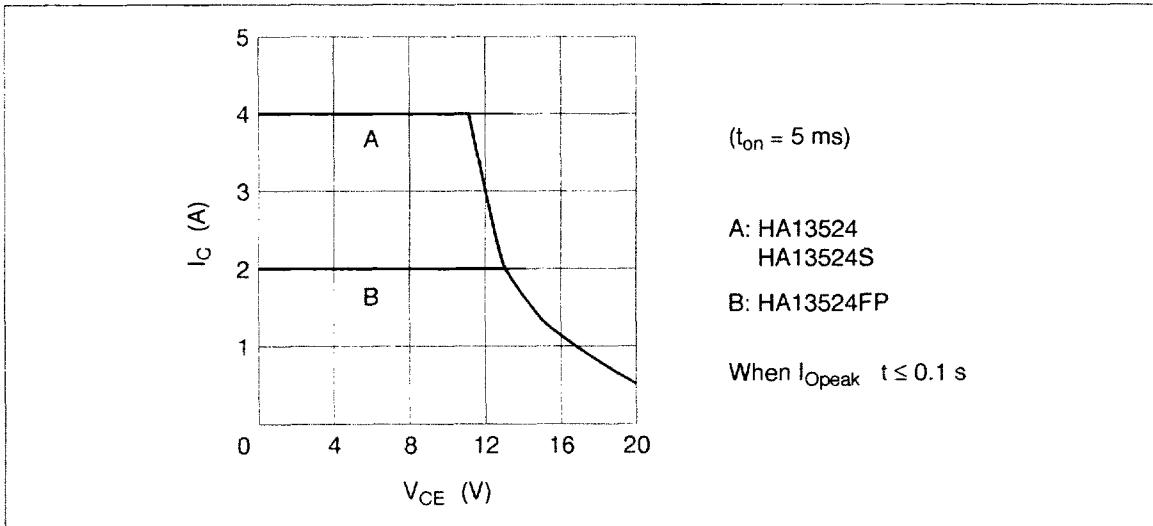
### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Item	Symbol	HA13524	HA13524S	HA13524FP	Unit	Notes
Power supply voltage	$V_{ps}$	15	15	15	V	1
Output current	$I_{Opeak}$	4	4	2	A	2
	$I_O$	2.8	2.8	1.5		
Retract current	$I_{ret}$	1.2	1.2	0.7	A	
Retract voltage	$V_{ret}$	5	5	5	V	
Input voltage	$V_{in}$	$V_{ps}$	$V_{ps}$	$V_{ps}$	V	3
Power dissipation	$P_T$	10 ( $T_c = 120^\circ\text{C}$ )	10 ( $T_c = 120^\circ\text{C}$ )	5 ( $T_c = 115^\circ\text{C}$ )	W	4
Junction temperature	$T_j$	150	150	150	$^\circ\text{C}$	5
Storage temperature range	$T_{stg}$	-55 to +125	-55 to +125	-55 to +125	$^\circ\text{C}$	

Notes: 1. Operating voltage ranges is as follows.

$$V_{ps} = 10.2 \text{ to } 13.8 \text{ V}$$

2. ASO of each output transistor is shown below. Operating locus must be with in the ASO.



3. As for pin Retract and Retset, Maximum input voltage are  $V_{ret}$
4. Thermal resistance is shown below.
  - HA13524  
 $\theta_{j-c} \leq 3^\circ\text{C/W}$ ,  $\theta_{j-a} \leq 40^\circ\text{C/W}$  (When a glass epoxy printed circuit board is used with a wiring density of 20 %)
  - HA13524S  
 $\theta_{j-c} \leq 3^\circ\text{C/W}$ ,  $\theta_{j-a} \leq 40^\circ\text{C/W}$  (When a glass epoxy printed circuit board is used with a wiring density of 20 %)
  - HA13524FP  
 $\theta_{j-c} \leq 7^\circ\text{C/W}$ ,  $\theta_{j-a} \leq 62^\circ\text{C/W}$  (When a glass epoxy printed circuit board is used with a wiring density of 20 %)
5. Operating junction temperature range is 0 to +125°C.

**Electrical Characteristics (Ta = 25°C, Vps = 12 V, VSSsense = 5 V)**

Item	Symbol	Min	Typ	Max	Units	Test conditions	Applicable terminal	Note
Quiescent current	I <sub>PS0</sub>	—	3	5	mA	CE = H, Retract = L	Y	
	I <sub>PS1</sub>	—	45	75	mA	CE = L, Retract = L		
	I <sub>PS2</sub>	—	15	25	mA	CE = L, Retract = H Retpow = 5 V	W	
CE, Higain & Retract Input	Input current	I <sub>in</sub>	—	—	±10	µA	V <sub>in</sub> = 0 to V <sub>PS</sub>	B, C, L
		I <sub>in(ret)</sub>	—	—	±15	µA	V <sub>retpow</sub> = V <sub>PS</sub>	
	Input high voltage	V <sub>IH</sub>	2.0	—	—	V		
	Input low voltage	V <sub>IL</sub>	—	—	0.8	V		
PA1 & PA2	Input resistance	R <sub>in(H)</sub>	23	33	43	kΩ	Higain = H	G, H
		R <sub>in(L)</sub>	35	50	65	kΩ	Higain = L	
	Input common mode voltage range	V <sub>cm(H)</sub>	0	—	V <sub>PS</sub> -2.0	V	Higain = H	
		V <sub>cm(L)</sub>	0	—	V <sub>PS</sub> -5.0	V	Higain = L	
Output quiescent voltage	V <sub>q</sub>	5.45	5.75	6.05	V	V <sub>ctl</sub> = V <sub>ref</sub> = 5.75 V R <sub>L</sub> = 2.5 Ω, R <sub>S</sub> = 0.1 Ω	R, T	
Total output saturation voltage	V <sub>sat1</sub>	—	2.6	3.1	V	I <sub>O</sub> = 3.0 A	HA13524/S	1
	V <sub>sat2</sub>	—	1.5	1.9	V	I <sub>O</sub> = 1.0 A		
Total output saturation voltage	V <sub>sat3</sub>	—	1.8	2.4	V	I <sub>O</sub> = 1.5 A	HA13524FP	1
	V <sub>sat4</sub>	—	1.4	1.7	V	I <sub>O</sub> = 0.5 A		
Output leak current	I <sub>CER</sub>	—	—	±100	µA			2
Output offset voltage (PA2-Sense)	V <sub>ofs(H)</sub>	—	—	±10	mV	Higain = H, R <sub>S</sub> = 0.1 Ω V <sub>ctl</sub> = V <sub>ref</sub> = 5.75 V		
	V <sub>ofs(L)</sub>	—	—	±5	mV	Higain = L, R <sub>S</sub> = 0.1 Ω V <sub>ctl</sub> = V <sub>ref</sub> = 5.75 V		
Transfer gain	g <sub>m(H)</sub>	—	0.8	±20%	A/V	Higain = H	R' <sub>S</sub> = 1 Ω	
	g <sub>m(L)</sub>	—	0.2	±20%	A/V	Higain = L		
Gain bandwidth	B(H)	—	50	—	kHz	Higain = H	R <sub>L</sub> = 2.5 Ω R <sub>S</sub> = 0.1 Ω	
	B(L)	—	80	—	kHz	Higain = L		

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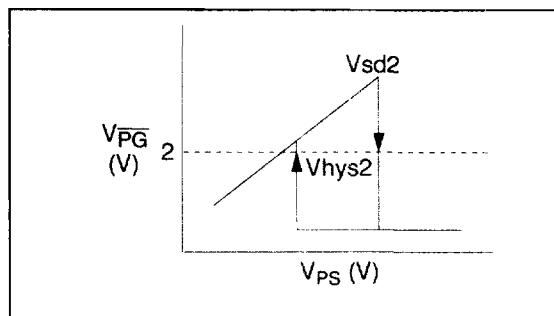
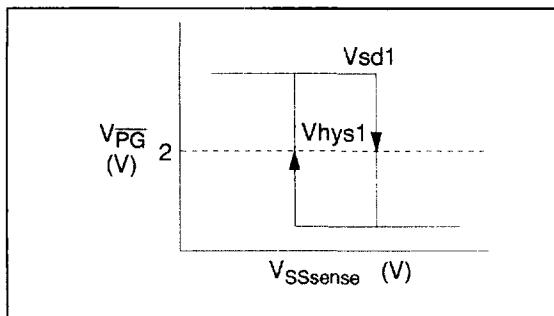
## Electrical Characteristics ( $T_a = 25^\circ\text{C}$ , $V_{ps} = 12 \text{ V}$ , $V_{SSsense} = 5 \text{ V}$ ) (cont)

Item		Symbol	Min	Typ	Max	Units	Test conditions	Applicable terminal	Note
Retract	Retpow voltage	$V_{retpow}$	3.5	—	—	V	$I_{ret} = 0.2 \text{ A}$	W	
	Retset reference voltage	$V_{retset}$	1.30	1.38	1.46	V		V	
	Retset input current	$I_{retset}$	—	—	$\pm 2$	$\mu\text{A}$	$V_{retset} = 1.38 \text{ V}$		
	Retout saturation voltage	$V_{retsat1}$	—	2.7	3.2	V	$I_{ret} = 1.0 \text{ A}$ , HA13524/S	U	
		$V_{retsat2}$	—	2.2	2.6	V	$I_{ret} = 0.5 \text{ A}$ , HA13524FP		
OP1 & OP2	PA2 lowside saturation voltage	$V_{satL}$	—	0.15	0.4	V	$I_{ret} = 0.2 \text{ A}$ $V_{retpow} = 3.5 \text{ V}$	R	
	Input current	$I_{inop}$	—	—	$\pm 500$	nA		E, F, I, J	
	Input offset voltage	$V_{osop}$	—	—	$\pm 10$	mV			
	Input common mode voltage range	$V_{cmop}$	0	—	$V_{ps}$ -1.8	V			
	Output high voltage	$V_{O_{HOP}}$	$V_{ps}$ -1.3	—	—	V	$I_{out} = 1.0 \text{ mA}$	D, K	
$V_{SSsense}$	Output low voltage	$V_{O_{LOP}}$	—	—	1.1	V	$I_{out} = 1.0 \text{ mA}$		
	Open loop gain	$G_{op}$	—	54	—	dB	$f = 10 \text{ kHz}$	2	
	Gain bandwidth	$B_{op}$	—	6	—	MHz	$G_{op} = 0 \text{ dB}$	2	
	Input resistance	$R_{in1}$	36	52	68	k $\Omega$		A	
	Operating voltage	$V_{sd1}$	3.75	4.0	4.25	V	$V_{SSsense}$	A	3
LVI		$V_{sd2}$	9.0	9.6	10.2	V	$V_{ps}$	Y	
	Hysteresis	$V_{hys1}$	—	0.2	—	V	$V_{SSsense}$	A	3
		$V_{hys2}$	—	0.6	—	V	$V_{ps}$	Y	
	Threshold voltage	$V_{th}$	—	2.5	—	V		P	
Delay	Ct charge current	$I_{cha}$	—	20	—	$\mu\text{A}$			
	Ct discharge current	$I_{dis}$	3	—	—	mA			
	Output high current	$I_{OH}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{OH} = 15 \text{ V}$	Q	
Powgood	Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 1.0 \text{ mA}$		

**Electrical Characteristics ( $T_a = 25^\circ\text{C}$ ,  $V_{ps} = 12\text{ V}$ ,  $V_{SSsense} = 5\text{ V}$ ) (cont)**

Item	Symbol	Min	Typ	Max	Units	Test conditions	Applicable terminal	Note
OTSD	Operating temperature	Tsd	125	150	—	°C		2
	Hysteresis	Thys	—	25	—	°C		

Note: 1. Total output voltage is as total as High side saturation voltage and Low side saturation voltage.  
 2. Value for guide only. At the delivery of this characteristic is not tested.  
 3. LVI Operating voltage is shown below.



Total output saturation voltage  $V_{sat}$  and Low side saturation voltage  $V_{satL}$  are shown below.  
 (Value for guide only)

