MULTI-PURPOSE REMOTE CONTROL TRANSMITTER IC
CMOS LSI

DESCRIPTION

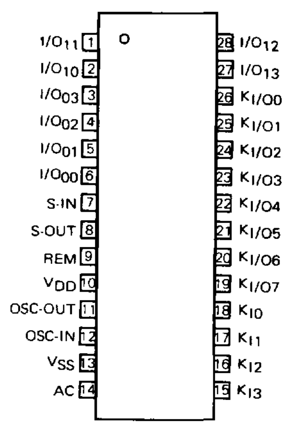
The μPD6126AG is intended for applications in infrared remote-control transmitters for controlling TV, VCR, stereo components, cassette decks, airconditioners, and other appliance.

It consists of a 1 k step ROM (10 bits/step), 32 word RAM (5 bits/word), 4 bit parallel processing ALU, programmable timer, key input/output ports, and a transmission/output port. The remote-control transmitter functions can be programmed.

FEATURES

- Programmable infrared remote-control transmitter
- 19 instructions
- Instruction cycle
  17.6 μs/455 kHz (ceramic resonator)
- Program memory (ROM) size
  1 024 x 10 bits
- Data memory (RAM) size
  32 x 5 bits
- Programmable timer (9 bits)
- I/O: 16 pins
  Input: 4 pins
  Serial input: 1 pin
- Send carrier frequency
  $f_{OSC}/12$, $f_{OSC}/8$
- Standby operation (HALT)
- Ceramic oscillation circuit for system clock
- CMOS
- Low power consumption
- Low operating voltage (2.0 V to 6.0 V)
- PKG, 28 pin mini-flat (375 mil)

PINNING DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply voltage	V_{DD}	7.0	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opt}	−20 to + 75	°C
Storage temperature	T_{stg}	−40 to +125	°C

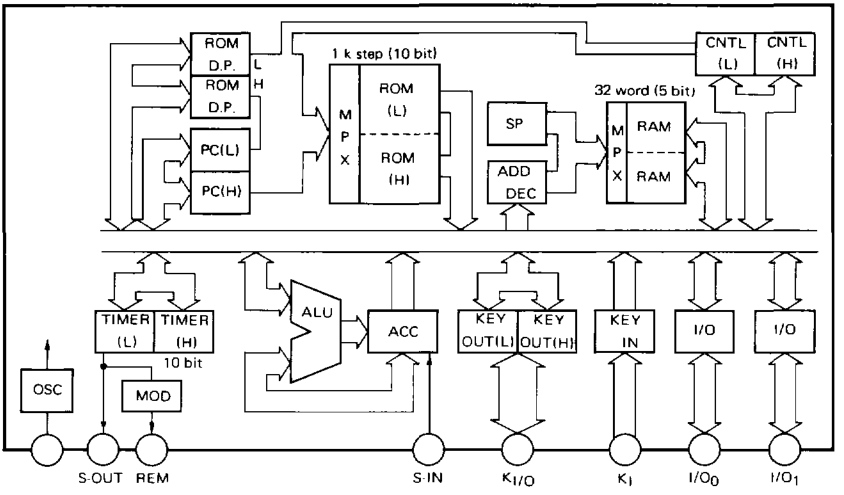
RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	2.0		6.0	V
Oscillation frequency	f_{OSC}	400		500	kHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0 V, f_{OSC} = 455 kHz, T_a = 25 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply voltage	V_{DD}	2.0		6.0	V	
Current consumption 1	I_{DD1}		0.3	1.0	mA	f_{OSC} = 455 kHz
Current consumption 2	I_{DD2}			1.0	μA	f_{OSC} = STOP
REM high-level output current	I_{OH1}	−5	−8		mA	V_O = 1.0 V
REM low-level output current	I_{OL1}	0.5	1.5	2.5	mA	V_O = 0.3 V
S-OUT high-level output current	I_{OH2}	−0.3	−1.0	−2.0	mA	V_O = 2.7 V
S-OUT low-level output current	I_{OL2}	1	1.5		mA	V_O = 0.3 V
K_I high-level input current	I_{IH1}	10		30	μA	V_I = V_{DD}
K_I high-level input current	$I_{IH1'}$			0.2	μA	V_I = V_{DD} (without pull-down resistor)
K_I low-level input current	I_{IL1}			−0.2	μA	V_I = V_{SS}
$K_{I/O}$, I/O high-level input current	I_{IH2}	10		30	μA	V_I = V_{DD}
$K_{I/O}$, I/O high-level input current	$I_{IH2'}$			0.2	μA	V_I = V_{DD} (without pull-down resistor)
$K_{I/O}$, I/O low-level input current	I_{IL2}			−0.2	μA	V_I = V_{SS}
$K_{I/O}$, I/O high-level output current	I_{OH3}	−1.5	−2.0	−4.0	mA	V_O = 2.5 V
$K_{I/O}$, I/O low-level output current	I_{OL3}	25	50	100	μA	V_O = 2.1 V
S-IN high-level input current	I_{IH3}	6		15	μA	V_I = V_{DD}
S-IN high-level input current	$I_{IH3'}$			0.2	μA	V_I = V_{DD} (without pull-down resistor)
S-IN low-level input current	I_{IL3}			−0.2	μA	V_I = V_{SS}
K_I, I/O high-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	
K_I, I/O low-level input voltage	V_{IL1}	V_{SS}		0.3 V_{DD}	V	V_I = V_{DD}
$K_{I/O}$ high-level input voltage	V_{IH2}	1.3			V	
$K_{I/O}$ low-level input voltage	V_{IL2}			0.4	V	
S-IN high-level input voltage	V_{IH3}	1.1			V	
AC pin pull up resistance	R_1	0.3		3.0	kΩ	V_I = V_{SS}
AC pin pull down resistance	R_2	150	400	1500	kΩ	V_I = 2.7 V

BLOCK DIAGRAM



1. INTERNAL BLOCK FUNCTIONS

1.1 PROGRAM COUNTER (PC) · · · 10 bits

This is a 10 bit binary counter for setting the 10 bit address information of the program memory.

PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	PC

Fig. 1.1 Program counter configuration

Each time an instruction is executed, the program counter is automatically incremented by the number of bytes of the instruction.

When a jump instruction (JMP0, JC, JF) is executed, the program counter indicates the jump destination. The immediate data and data memory contents are loaded into some or all bits of the program counter.

When a call instruction (CALL0) is executed, the program counter contents are incremented and saved in the stack memory. Then, values required for each jump instruction are loaded. When a return instruction (RET) is executed, the stack memory contents are loaded into the program counter.

When an all clear command is input, the program counter is initialized to 000.

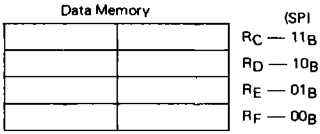
1.2 STACK POINTER (SP) · · · 2 bits

This is a 2-bit register storing the stack area starting address, when the data memory is used as a stack memory.

The stack pointer is incremented when a call instruction (CALL0) is executed and decremented when a return instruction (RET) is executed.

The stack pointer is initialized to 00_B after all-clear operation, and sets the most significant address (F_H) of the data memory.

The relationship between stack pointers and data memory area are as follows:



When a stack pointer overflows, it is assumed that the CPU ran out of control and the program counter is initialized to 000.

1.3 PROGRAM MEMORY (ROM) · · · 1 024 steps x 10 bits

This is a mask programmable ROM (1 024 steps x 10 bits) addressed by the program counter.
The program memory stores a program, table data, and so forth.

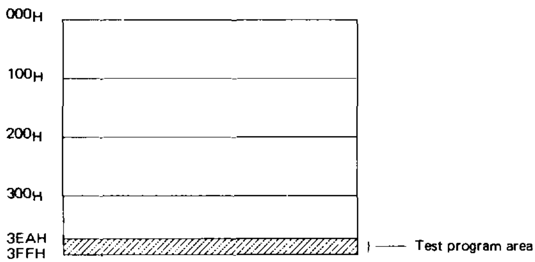


Fig. 1.2 Program memory map

The program memory address is 000H-3FFH.
Users cannot use the test program area.

1.4 DATA MEMORY (RAM) · · · 32 words x 5 bits

This is a static RAM (32 word x 5 bits) used for storing processing data. The data memory may be handled in 8 bit units. R_0 can be used as the ROM data pointer.

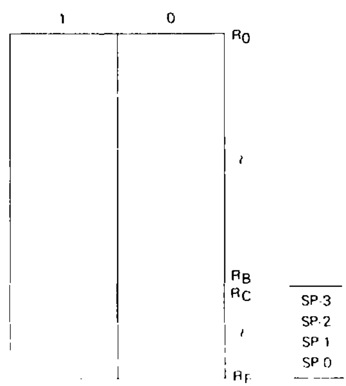


Fig. 1.3 Data memory configuration

1.5 DATA POINTER (R_0)

R_0 (R_{10}, R_{00}) of the data memory can be used as a ROM data pointer.

R_0 specifies eight lower bits of the ROM address, and the two upper bits are specified by the control register.

Setting a ROM address in the data pointer will facilitate reference of a ROM data table.

CNTL REG		R_{10}				R_{00}				
AD_9	AD_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	R_0

Fig. 1.4 Data pointer configuration

1.6 ACCUMULATOR (A) · · · 4 bits

The accumulator is a 4-bit register used for various operations.

A_3	A_2	A_1	A_0	A

Fig. 1.5 Accumulator configuration

1.7 ARITHMETIC LOGIC UNIT (ALU) · · · 4 bits

The arithmetic logic unit is a 4-bit operation circuit used for simple processing such as logical operations.

1.8 FLAG

(1) Status flag

If the port status checked by an STTS instruction matches the condition specified by this instruction, the status flag (F) is set (to 1).

(2) Carry flag

If the accumulator's MSB causes carry when an INC (increment) or RL (rotate shift) instruction is executed, the carry flag (C) is set (to 1).

If the accumulator contents indicate F_H when a SCAF instruction is executed, the carry flag (C) is set (to 1).

1.9 SYSTEM CLOCK GENERATION CIRCUIT

The system clock generation circuit is comprised of a ceramic vibrator (400 to 500 kHz) oscillator.

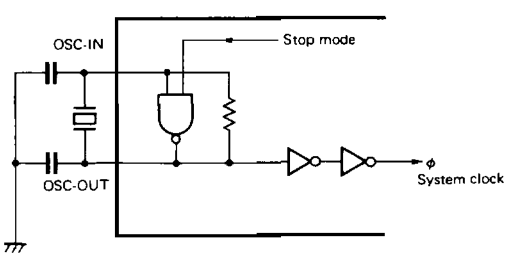


Fig. 1.6 System clock generation circuit

The system clock generation circuit stops the oscillator (system clock ϕ) in the stop mode.

1.10 TIMER

The timer decides transmission output pattern. The timer consists of the 9 bit down-counter block and the 1 bit register to decide whether carrier pulses are output or not. (10 bits in total)

The 9 bit down-counter decrements by 1 every instruction execution ($8/f_{OSC}$) at the timer run mode. When the 9 bit down-counter value becomes 000, the timer operation stops and halt reset signal is out. If CPU operation state is the HALT TIMER mode (waiting for timer up), the halt mode is reset and next instruction is operated.

The count down time is decided by the following expression (set up value (HEX) + 1) x $8/f_{OSC}$. This value is set by timer operation instructions. (MOV T_t, A, MOV T, #data ...)

According to the MSB register value, the REM output signal is selected whether carrier pulses or low level. When the MSB is 1, carrier pulses ($f_{OSC}/12$ or $f_{OSC}/8$) are output until the 9 bit down-counter value goes to 000. When the MSB is 0, the REM output level is low.

At the S-OUT pin the MSB inverted level is output. When carrier pulses are output at the REM output, the S-OUT output level is low. When carrier pulses are not output from the REM output, the S-OUT output level is high.

The OSCILLATION STOP HALT instruction is not executed until the 9 bit down-counter value becomes 000. If the HALT reset condition is match during the timer running, HALT mode is reset immediately then the next instruction is executed.

The timer start/stop is controlled by the control register (P_1). (See the explanation of the control register)

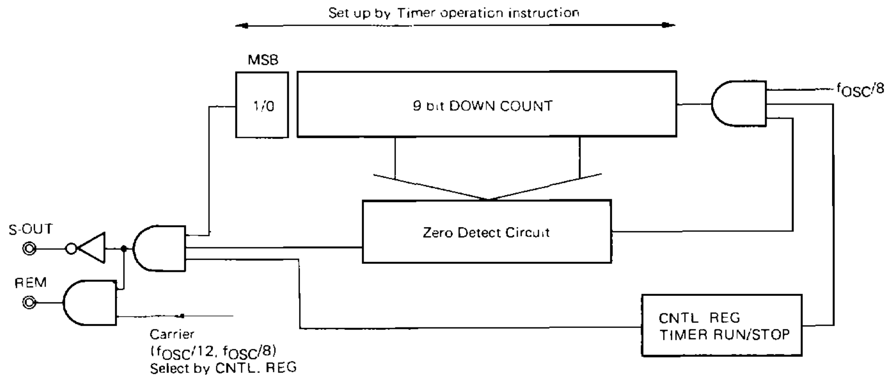


Fig. 1.7 Timer block configuration

1.11 SERIAL INPUT PORT

Serial data is input from a serial input port. When the control register (P_1) is set in the serial input mode, the serial input port is connected to the LSB of the accumulator and the serial input port is pulled down to the V_{SS} level within the LSI chip. If the left shift instruction is executed for the accumulator, the serial input port data is set in the LSB of the accumulator.

If the serial input mode is canceled, the serial input pin impedance is made high.

When the left shift instruction is executed for the accumulator, the MSB data is set in the LSB.

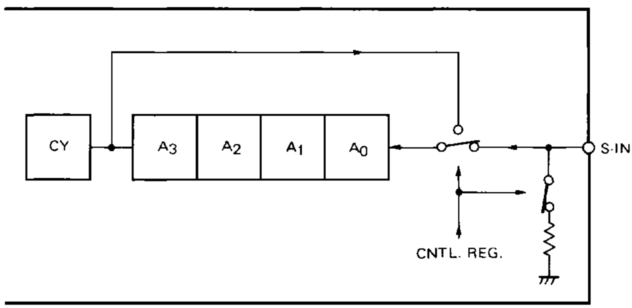


Fig. 1.8 Serial input port configuration

1.12 $K_{I/O}$ PORT (P_0)

This is an 8 bit port for key scan output. When the control register (P_1) is set in the input mode, this port can be used as an 8 bit input port. In this case, all pins are pulled down to the V_{SS} level.

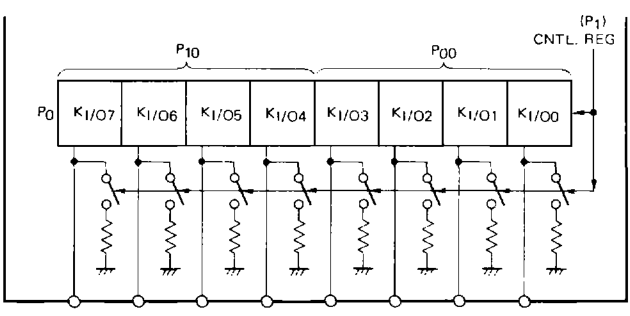


Fig. 1.9 $K_{I/O}$ port configuration

1.13 K_I PORT (P_{12})

This is a 4 bit input port for key input. All pins are pulled down to the V_{SS} level.

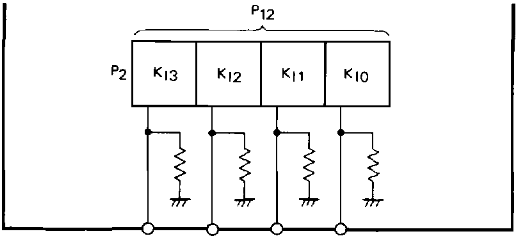


Fig. 1.10 K_I port configuration

1.14 I/O PORTS (P_3, P_4)

These are I/O ports for key matrix extension. Input and output modes are switched by the LSB of the P_{13}, P_{14}.

In the output mode, the pull-down resistances in the LSI chip are disconnected.

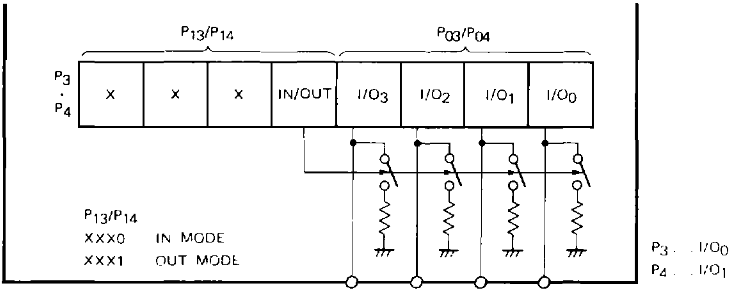
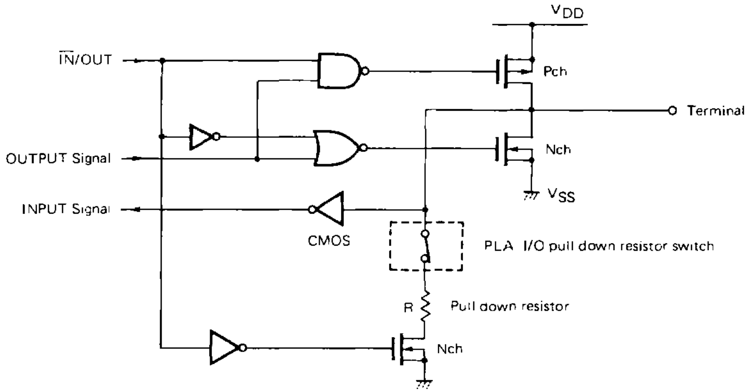


Fig. 1.10 I/O port configuration

1.15 $K_{I/O}$, I/O pull down resistors

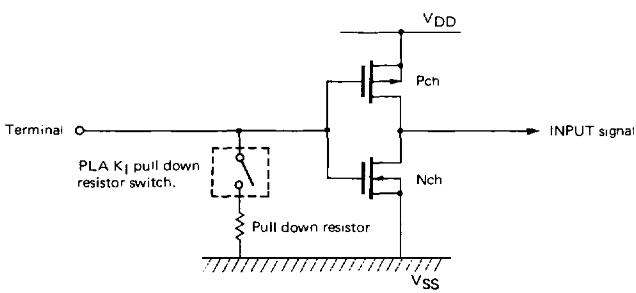


Whether or not I/O port pull-down resistors can be selected in the MASK OPTION.

When the I/O port pull-down resistors switches are ON, pull-down resistors are activated at the input mode.

When the $K_{I/O}$ port is set to the input mode, pull-down resistors are activated.

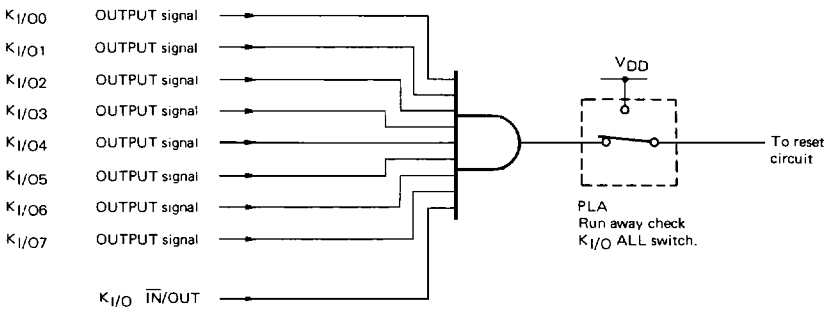
1.16 K_I pull down resistors



There are pull-down resistors.

Whether or not these pull-down resistors can be selected in the MASK OPTION.

1.17 Run away check $K_{I/O}$ ALL (I/O_0 ALL, I/O_1 ALL)



When the $K_{I/O}$ ALL switch is ON, the system reset function will operate by detecting the OSC STOP HALT (stand-by) mode and $K_{I/O}$ output levels (not all "H").

This function is useful for a key matrix application. Because in a stand-by mode, all key sources have to be active. If not, some keys will not operate until their key sources will be set to the active level.

1.18 CONTROL REGISTER

The control register consists of eight bits. The meanings of these bits are described below.

Table

D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
TEST MODE		*	HALT	D.P. AD_9	D.P. AD_8	MOD	TIMER	$K_{I/O}$	RLA_{CC} A_0 ←	
Must be set to "0".		NOP	NOP	*	*	$f_{OSC}/8$	STOP	IN	A_3	0
		NOP	OSC STOP	*	*	$f_{OSC}/12$	RUN	OUT	S_{IN}	1

D_0 : Specifies the data to be input to A_0 when the accumulator is shifted. $0 = A_3$ $1 =$ S-IN

D_1 : Specifies the $K_{I/O}$ state. 0 = Input mode 1 = output mode

D_2 : Specifies the timer state. 0 = Clock stop 2 = Clock in

D_3 : Specifies the REM output carrier frequency. $0 = f_{OSC}/8$ $1 = f_{OSC}/12$

D_4, D_5 : Specifies the two upper bits of the ROM data pointer.

D_6 : Sets the oscillator circuit when a HALT instruction is executed.

0 = Oscillation does not stop

1 = Oscillation stops (stop mode)

D_7 : NOP

D_8, D_9 : Must be set to 0 (test mode setting register).

2. STANDBY FUNCTION (HALT)

The μPD6126AG is provided with a standby mode (HALT) to save power while the program is standby. In addition, the control register can stop the oscillator circuit (stop mode).

When the standby mode is selected, program execution stops. The preceding register and data memory contents are saved in this case.

2.1 STOP MODE (OSCILLATION STOP: HALT)

In the stop mode, the system clock generation circuit (ceramic oscillation, circuit) stops. Therefore, all the operations that require system clock pulses stop.

If a HALT instruction is executed while the timer is operating, the stop mode is set after completion of count-down by the timer.

2.2 HALT MODE (OSCILLATION CONTINUES: HALT)

The CPU stops operation until a halt cancel condition is generated. In this case, the system clock generation circuit continues to operate.

2.3 STANDBY CANCEL CONDITION

(1) S-IN input
(2) $K_{I/O}$ input
(3) K_I input
(4) Timer countdown end
(5) I/O input
(6) K_I, I/O input

*: When setting a standby cancel condition using (1), (2), (3) or (5), either H-level or L-level must be specified.

2.4 AC PIN

Setting the AC pin to the V_{SS} level will reset the program counter.

Watchdog Timer Function:

A power-on-reset and a CR watchdog timer circuit can be constructed by inserting a 0.1 μF capacitor between the AC and V_{SS} pins.

2.5 MASK OPTION (PLA DATA)

Mask option can be used to specify:

(1) K_I, $S\text{-}_{IN}$, I/O_0, and I/O_1 port pull-down resistors selection.

(2) Carrier duty selection (1/2 or 1/3)

(3) Run away check mode selection (note: This function is not supported on μPD6126.)

SW change bit assignments

		MSB							LSB
		7	6	5	4	3	2	1	0
0	K_I	PULL DOWN resistors				0			
1	DUTY, S-IN	0	0	0	DUTY	0	0	S-IN PULL DOWN resistor	0
2	Run away check	$K_{I/O}$ ALL	HALT S-IN	HALT $K_{I/O}$	HALT K_I	HALT I/O_0	HALT I/O_1	I/O_0 ALL	I/O_1 ALL
3	I/O_0	PULL DOWN resistors				0			
4	I/O_1	PULL DOWN resistors				0			

SW for data

(1) PULL DOWN resistor
- 0 ⇒ Non-existent
- 1 ⇒ Existent

(2) Modulation duty (when f/12)
- 0 ⇒ 1/2 Duty
- 1 ⇒ 1/3 Duty

(3) Run away check

(a) $K_{I/O}$ ALL, I/O_0 ALL, I/O_1 ALL

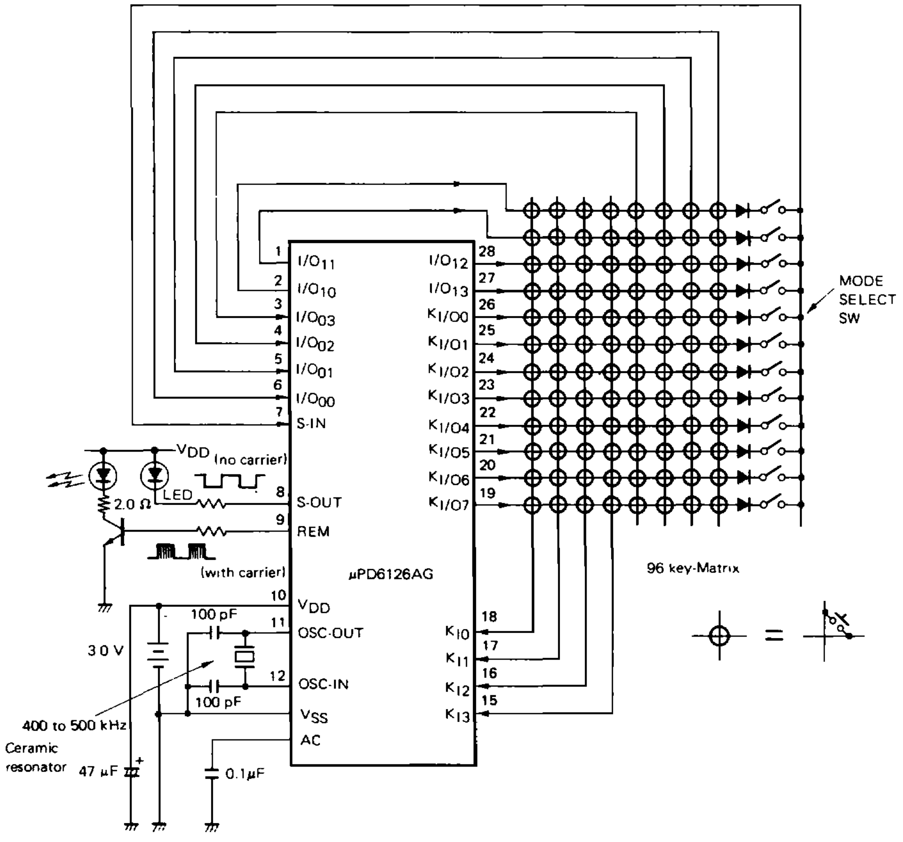
In OSCILLATION STOP HALT, the system reset function operates when the $K_{I/O}$ port (I/O_0 port, I/O_1 port) is a input mode or the $K_{I/O}$ (I/O_0, I/O_1) port output levels are not all H.
- 0 ⇒ Non-reset
- 1 ⇒ Reset

(b) HALT $S\text{-}_{IN}$, HALT $K_{I/O}$, HALT K_I, HALT I/O_0, HALT I/O_1

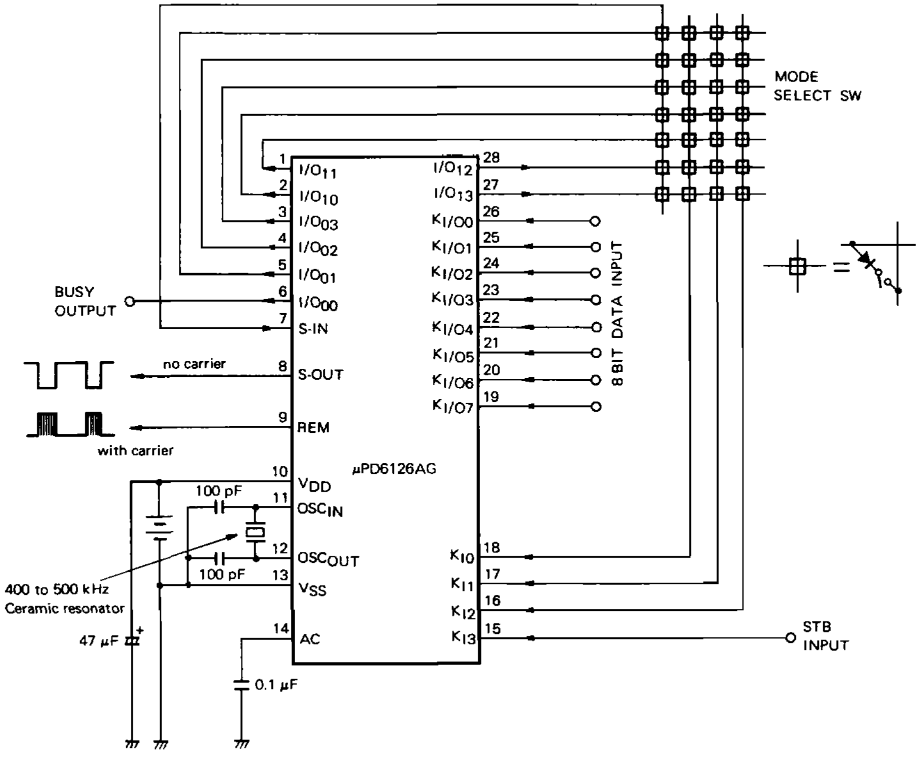
In a HALT mode, the system reset function operates when this HALT mode is specified as no use.
- 0 ⇒ use
- 1 ⇒ no use

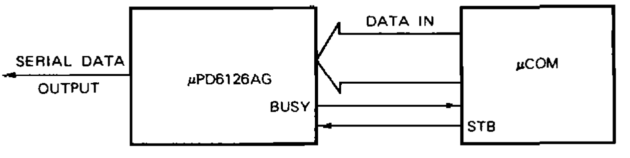
APPLICATION

INFRARED REMOTE CONTROL TRANSMITTER

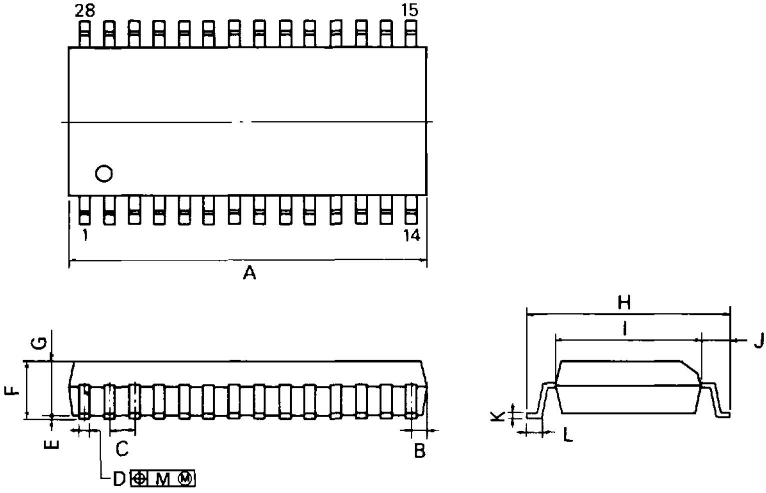


APPLICATION





28 Pin Mini Flat Package



P28GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	$10.3^{\pm 0.3}$	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

ORDERING INFORMATION

Part Number	Package
μPD6126AG	28 PIN MINI FLAT (300 mil)