

## DESCRIPTION

The HDM8516 digital demodulator for direct broadcast satellite (DBS) receivers is a single chip solution fully compliant with the European Telecommunications Standards Institute (ETSI) specification ETS 300 421. This chip integrates an A/D converter, a variable rate matched filter, a variable rate QPSK demodulator with a Viterbi decoder, a Deinterleaver and a Reed Solomon decoder.

The HDM8516, which is implemented in a 0.25um CMOS, Four Layer Metal Process, provides variable rate capability while operating with a fixed frequency sampling clock. Digital samples of baseband I and Q data are generated by an internal A/D converter, then provided to the demodulator at a fixed sample rate. The root raised cosine filter is implemented internally with fully digital techniques. Similarly, the symbol timing recovery and carrier phase tracking functions are performed entirely in the digital domain. This approach provides minimum constraints on external circuits, thus reducing overall system costs.

The HDM8516 may be configured by an external processor for a specific symbol rate, and carrier frequency along with loop gain parameters. The HDM8516 provides an external AGC signal which is used to control the gain of the analog signal which is applied to the down-converters. And it also provides a digital AGC internally which controls the gain of the signal out of the matched filters. In addition, the HDM8516 provides fully programmable sweep circuitry to aid in initial acquisition when large frequency offsets may be present.

The digital frequency translation capability of the HDM8516 permits this part to be used in frequency multiplexing applications. In this application, an entire transponder bandwidth containing many signals is sampled at a fixed rate. The digital oscillator within the HDM8516 is programmed to the specific desired carrier frequency within that band to permit the selected signal to be passed through the baseband filter and processed by the demodulator circuits.

## APPLICATION

Digital Satellite Receiver & Set Top Box

## GENERAL FEATURE

- Fully DVB & DSS compliant
- Multi-standard QPSK, BPSK demodulation
- Dual 6bit A/D converters
- Continuously variable symbol rate from 1Msps to 50Msps
- Internal digital root raised cosine filter with roll-off of 0.35 or 0.20
- Frequency multiplexing capability
- Automated frequency search
- Internal bias cancellation
- Both wideband and narrowband AGC
- Noise calibration for antenna steering
- Output data rate as high as 82Mbps
- Fixed frequency sampling clock
- Simple interface with tuner and analog processing
- I<sup>2</sup>C and parallel control interface
- 22KHz tone and DiSEqC™ support
- Serial and parallel data output
- 100LQFP / 100MQFP

## DEMODULATOR FEATURE

- Sampling Clock Frequency : max 90MHz
- Analog Input Full Scale Range : 0.9Vpp ~ 1.1Vpp
- Symbol Rate : 1Msps ~ 50Msps
- Symbol Rate Margin : Up to  $\pm 2\% \times f_{\text{symbol}}$  (@DVB spec.)
- Viterbi Data Rate : ~ 90Mbps
- Reed Solomon Data Rate : ~ 82Mbps
- Implementation Loss : under 0.5dB
- Symbol Rate Resolution : Clock/2<sup>20</sup>
- Acquisition Sweep Range :  $\pm$  Clock/2
- Carrier Frequency Resolution : Clock/2<sup>20</sup>
- Carrier Tracking Range :  $\pm$  Clock/2

## Ordering Number

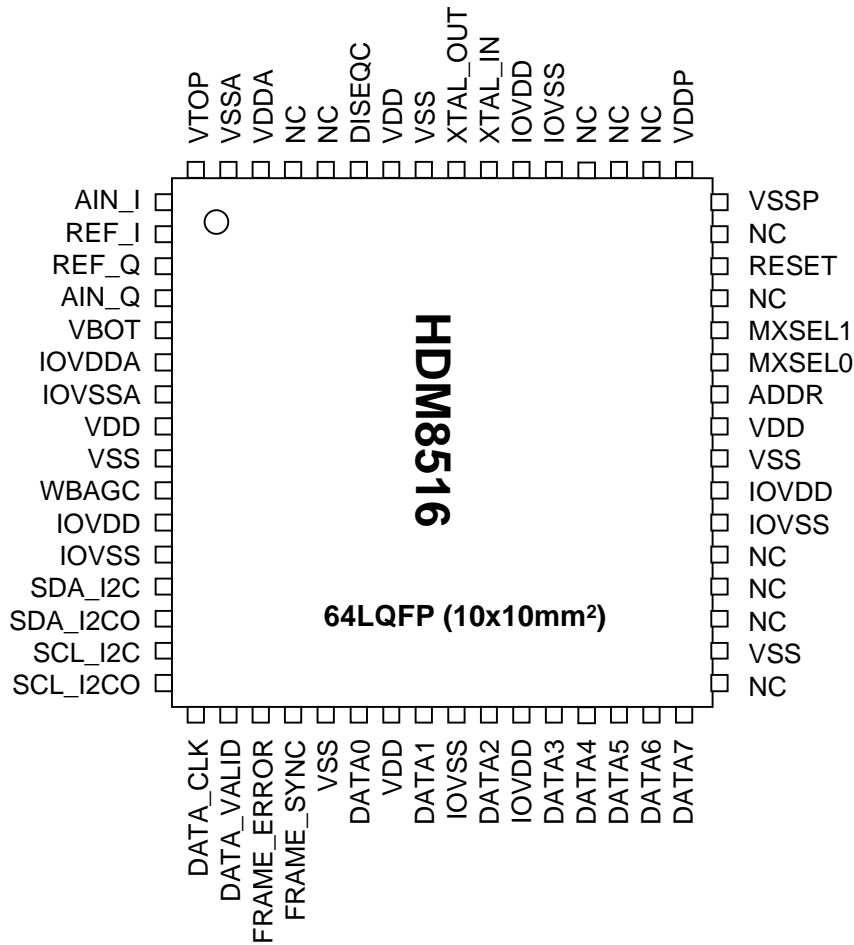
PRODUCT	PKG
HDM8516	64LQFP

## INDEX

<b>NO</b>	<b>ITEM</b>	<b>PAGE</b>
1	PIN INFORMATION	3
2	BLOCK DIAGRAM	5
3	ELECTRICAL CHARACTERISTICS	6
4	TECHNICAL OVERVIEW	8
5	SERIAL PROGRAMMING INTERFACE	13
6	FUNCTIONAL DESCRIPTION	15
7	REGISTER MAP	17
8	APPLICAION CIRCUIT	31
9	PKG DIMENSION	32

**1. PIN INFORMATION**

**1.1 PIN CONFIGURATION**

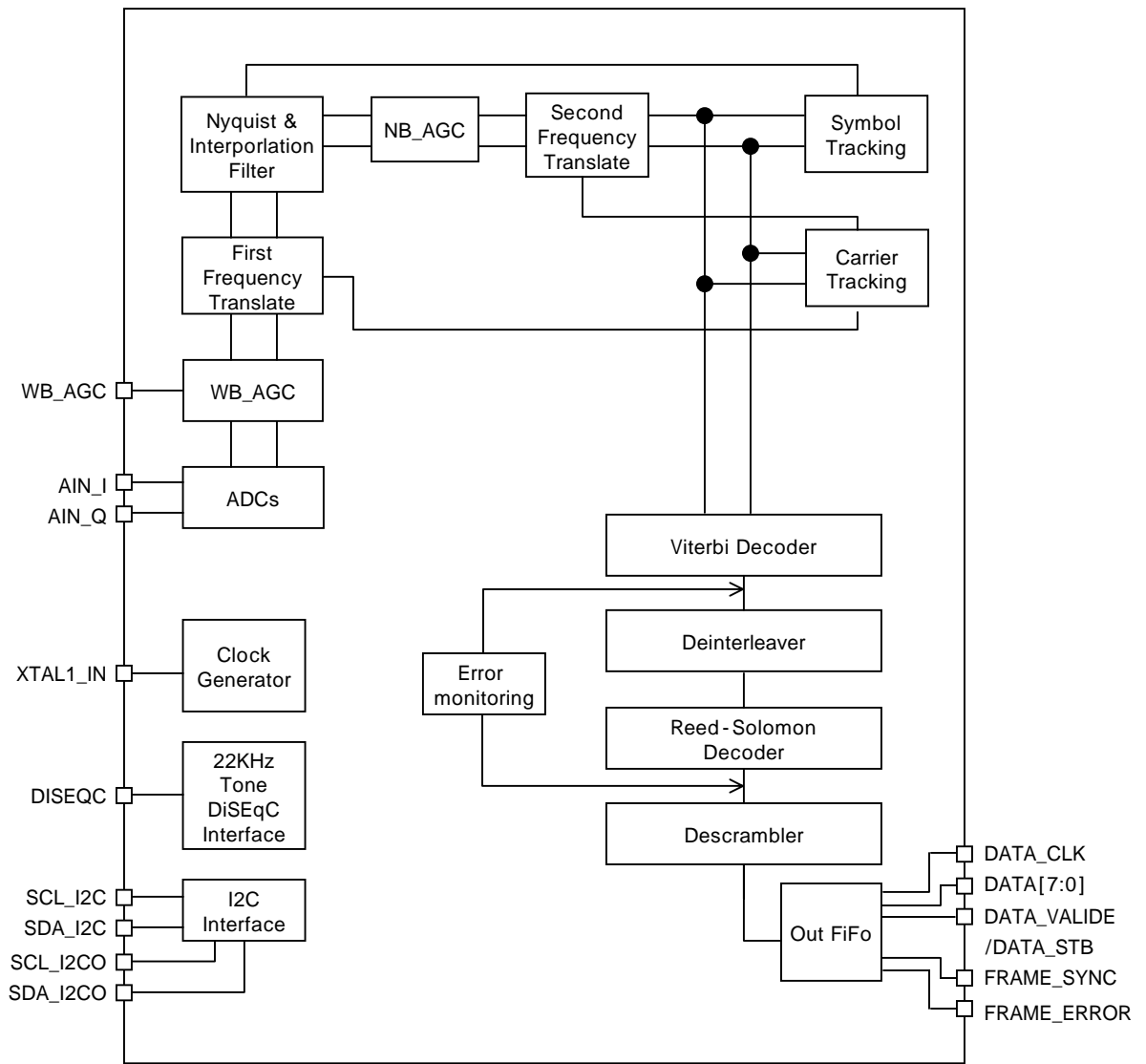


**1. PIN INFORMATION** (continued)

**1.2 PIN DESCRIPTION**

SYMBOL	PIN NUMBER		I/O	DESCRIPTION
	HDM8515(100LQFP)	64 LQFP		
FRAME_SYNC	1	20	O	Output 1 <sup>st</sup> byte Signal ( Synchro Byte Clock )
DISEQC	4	59	O	22kHz Tone.Programmable Output Port
WB_AGC	7	10	O	Control Signal to the Tuner
VTOP	26	64	O	ADC High Voltage Reference
AIN_I	27	1	I	Analog Signal Input(In-Phase Signal)
REF_I	30	2	O	Middle Reference Voltage for I Channel
REF_Q	31	3	O	Middle Reference Voltage for I Channel
AIN_Q	32	4	I	Analog Signal Input(Quadrature-Phase Signal)
VBOT	33	5	O	ADC Low Voltage Reference
XTAL_IN	43	55	I	4MHz Rectangular Pulse Input
XTAL_OUT	43	56	O	4MHz Rectangular Pulse Output
RESET	47	46	I	Reset(Active Low Operation)
ADR	57-59 62-65	42	I	I2C Slave Address Setting(Set"0" h74,Set"1 h75)
SDA_I2CO	74	14	I/O	Tuner Slave Data
SDA_I2C	75	13	I/O	Serial Data(I2C BUS)
SCL_I2CO	76	16	I	Tuner Serial Clock
SCL_I2C	77	15	I	Serial Clock(I2C BUS)
DATA [7:0]	85 ~ 87, 89 , 90 93 ~ 95	32 ~ 28 , 26 , 24 22	O	Output Data (In Case of Serial Data Mode, DATA0 is Data Out Port)
DATA_VALID /DATA_STB	96	18	O	Used to Transfer Data from HDM8515 to MPEG Decoder As MPEG Decoder Interface, Using one of them The Default is "DATA_VALID"
DATA_CLK	99	17	O	Output Byte Clock (In Case of Serial Mode, DATA_CLK is Bit Clock)
FRAME_ERROR	100	19	O	Output Error Signal. Set in case of Uncorrectable Frame.
MXSEL1 / MXSELO		44 / 43	I	Chip Function Selection(Set to "Ground" Only)
VDD	2,15,55 66,71,83	8,23,41 58	-	2.5V : IC Core Supply
VSS	3,16,67 72,79,84	9,21,34 40,57	-	0V : IC Core GND
IOVDD	9,21,45 60,78,91	11,27,39 54	-	3.3 V : I/O PAD Supply
IOVSS	10,22,46 61,92	12,25,38 53	-	0 V : I/O PAD GND
VDDP / VSSP	37 / 38	49 / 48	-	2.5V / GND : Supply and GND only PLL
VDDA / VSSA	24 / 25	62 / 63	-	2.5V / GND : Analog Supply and GND only ADC
IOVDDA / IOVSSA	28 / 29	6 / 7	-	3.3V / GND : Analog Supply and GND only ADC I/O PAD
NC	5,6,8,11,12,13,14 17,18,19,20,23,34 35,36,39,40,41,42 44,48,49,50,51,52 53,54,56,68,69,70 88,98	33,35,36,37,45, 47,50,51,52, 60,61	-	N.C. Pins Use These Pins in Ground status

2. BLOCK DIAGRAM



**3. ELECTRICAL CHARATERISTICS**

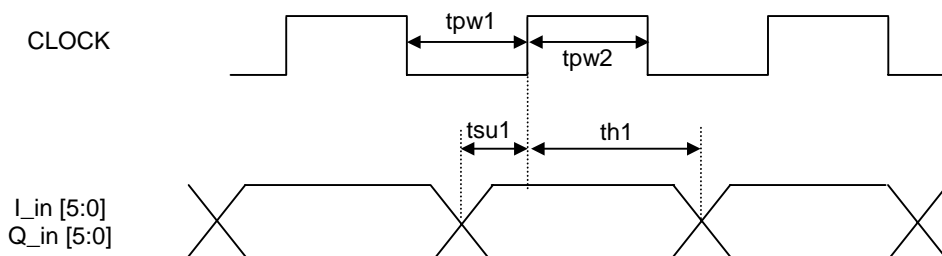
**3.1 DC CHARATERISTICS**

IOVDD = 3.3V, VDD,VDDA,VDDP = 2.5V, Ta = 0 ~ 70 , unless otherwise specified

SYMBOL	PARAMETER	MIN	MAX	UNIT	PARAMETER	
IDD	Dynamic Current	-	?	mA	IOVDD = 3.6, Freq = 90MHz VDD,VDDA,VDDP = 2.7	
IOVDD	Interface Power Supply Voltage	3.0	3.6	V	Normal Operation	
VDD	Core Power Supply Voltage	2.3	2.7			
V	ADC Power Supply Voltage	2.3	2.7			
VIL	Input Low Voltage	-	0.8			
VIH	Input High Voltage	2.0	-			
VOL	Output Low Voltage	-	0.4			IOL = 4mA
VOH	Output High Voltage	2.4	-			IOH = -4mA
IIL	Input Low Current	-10	10	uA	VIN = 0, IOVDD = 3.3	
IIH	Input High Current	-10	10		VIN=3.6,IOVDD = 3.3	
CIN	Input Capacitance	-	10	pF	Typical 5.75pF	
COUT	OUtput Capacitance	-	10		Typical 5.97pF	

**3.2 AC CHARATERISTICS**

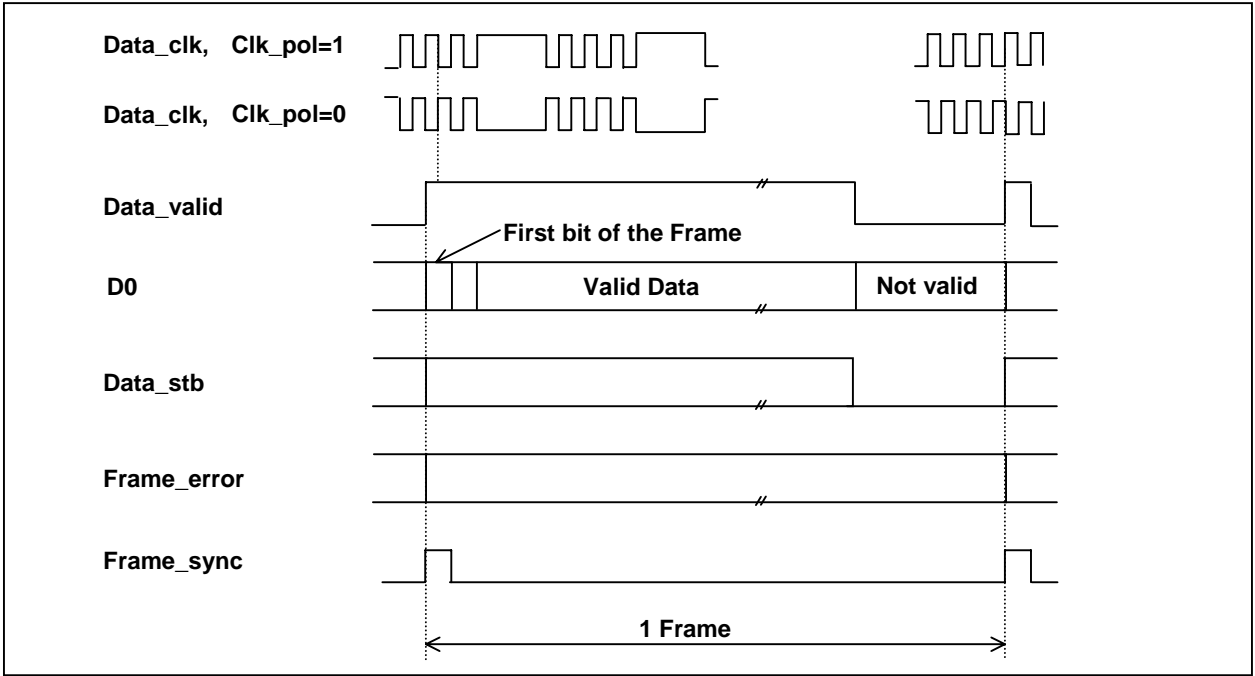
SYMBOL	PARAMETER	MIN	MAX	UNIT
tsu1	Input Data Setup before Clock	6.0	-	ns
th1	Input Data Hold after Clock	2.0	-	
tpw1	Low Pulse Width of Clock	8.7	-	
tpw2	High Pulse Width of Clock	8.1	-	



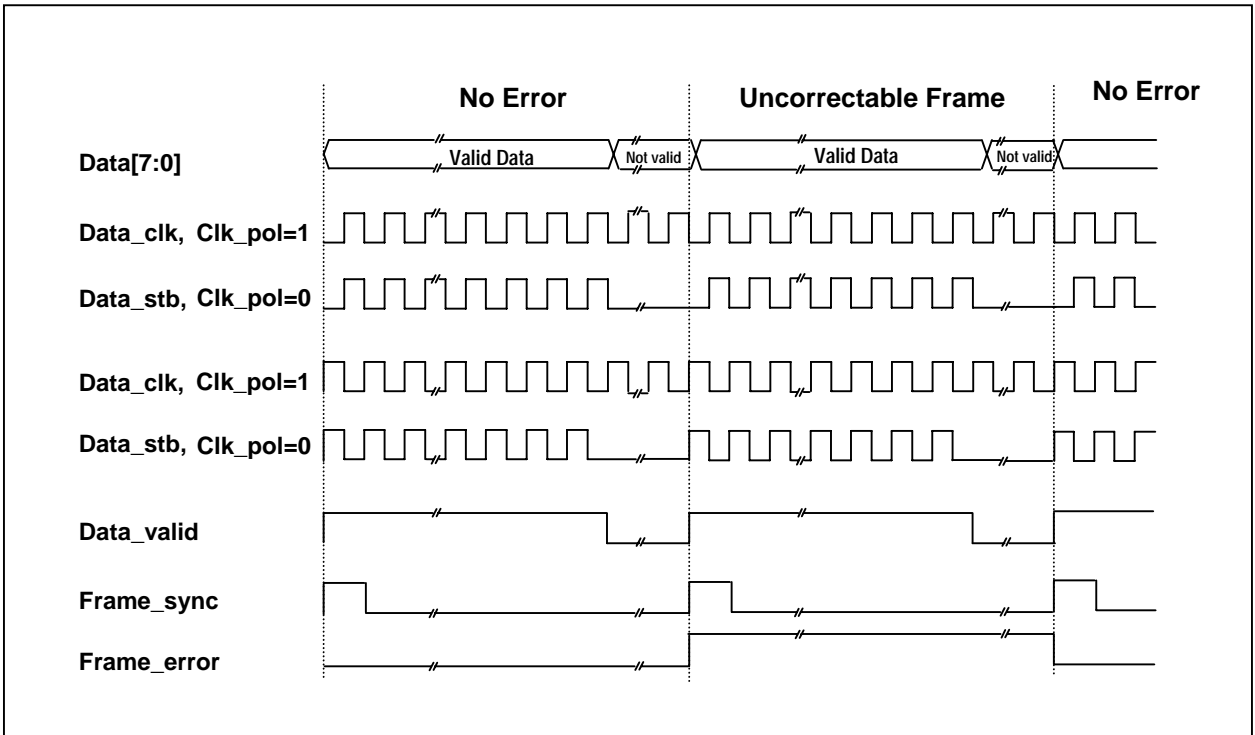
**3. ELECTRICAL CHARACTERISTICS** (continued)

**3.2 AC CHARACTERISTICS** (continued)

**Serial Output Interface**



**Parallel Output Interface**



## 4. TECHNICAL OVERVIEW

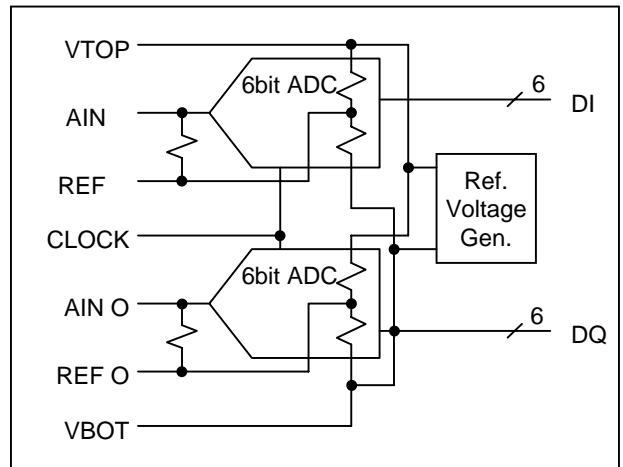
### 4.1 DUAL CHANNEL ANALOG TO DIGITAL CONVERTER

The block diagram shown below illustrates internal configuration of the Dual Channel ADC. Baseband signals, in-phase(I) and quadrature phase(Q), which are generated by down converters, are applied to the dual channel ADC and quantized to 6-bit digital codes respectively. The ADC is optimized to allow AC coupled inputs with full scale input range of 1V + or - 10%. An LSB weight is approximately 15.6 mV.

The full scale input analog conversion range ( $V_{pp}$ ) is determined by the voltages of  $V_{TOP}$  and  $V_{BOT}$  and simply equal to  $(V_{TOP} - V_{BOT})$ . The full scale range is defined as the voltage range that accommodates 63 codes of equally spaced LSBs. Also the ADC supplies its own reference voltages for A/D conversions. The voltages can be monitored by external reference pins. The  $V_{TOP}$ ,  $V_{BOT}$  represent top and bottom reference voltages respectively.  $REF_I$ ,  $REF_Q$  represent middle reference voltages for each channel. All these 4 reference voltage pins should be by-passed to GND via 0.1uF capacitors. The values of internally generated voltage of  $V_{TOP}$  and  $V_{BOT}$  are 1.5V and 0.5V respectively.  $V_{pp}$  can be adjusted by externally applying voltages to both  $V_{TOP}$  and  $V_{BOT}$  pins respectively when different conversion ranges are necessary.  $V_{TOP}$  can be adjusted as high as 1.7V and  $V_{BOT}$  can be as low as 0.3V. A larger input range can be established by taking  $V_{TOP}$  higher and  $V_{BOT}$  lower than on-chip generated voltages.

To supply necessary bias voltages for AC coupled applications,  $REF_I$  and  $REF_Q$ , which are middle reference voltages for I and Q channel, are connected to the analog input pins ( $A_{IN_I}$  and  $A_{IN_Q}$ ) respectively through 40kΩ resistors, as shown in the block diagram. For DC coupled applications, these voltages can be used to feed back offset compensation signals.

To insure optimum performance, a low impedance analog ground plane is recommended and should be separated from other digital ground planes. The analog power supplies should be by-passed at device to analog ground through 0.1uF ceramic capacitors.



### 4.2 VARIABLE RATE DEMODULATOR

The block diagram illustrates the overall configuration of the variable rate QPSK demodulator. Baseband in-phase (I) and quadrature (Q) inputs are applied to the demodulator at a fixed sampling rate. These digital samples are produced by A/D converters which employ AC coupling to minimize DC offset.

The only significant change to this configuration over the HDM8513A is the addition of the Second Frequency Translator. The carrier tracking block produces two outputs, one is the frequency correction which is provided to the First Frequency Translator. This insures that the input to the Dual FIR is always centered at zero frequency error, although there may be a phase error at this point. The second output of the Carrier Tracking function provides the phase correction to the Second

#### Frequency Translator

The carrier frequency error associated with these samples is removed digitally during tracking operations by a complex multiplier and a digitally controlled oscillator, sometimes called a numerically controlled oscillator (NCO). During initial acquisition, coarse frequency error is removed by a combination of the digital AGC within the HDM8516 and external analog tuning circuits.

A Dual filter performs the root raised cosine filtering of the frequency corrected baseband samples. This filter, which implements the function of equation (1), is always configured to have an impulse response duration of 8 symbols regardless of the programmed symbol rate. For low symbol rates, a large number of samples are used, while for high symbol rates a relatively low number of

**4. TECHNICAL OVERVIEW** (continued)

**4.2 VARIABLE RATE DEMODULATOR** (continued)

samples are processed for each filter output. The outputs of the dual filters are applied to a digital narrowband AGC which insures that the signal is optimally scaled to the Viterbi decoder to an accuracy of **+ or - 0.5 dB** to insure optimum FEC performance.

$$y[k] = \sum h[n] x[k-n] \quad (1)$$

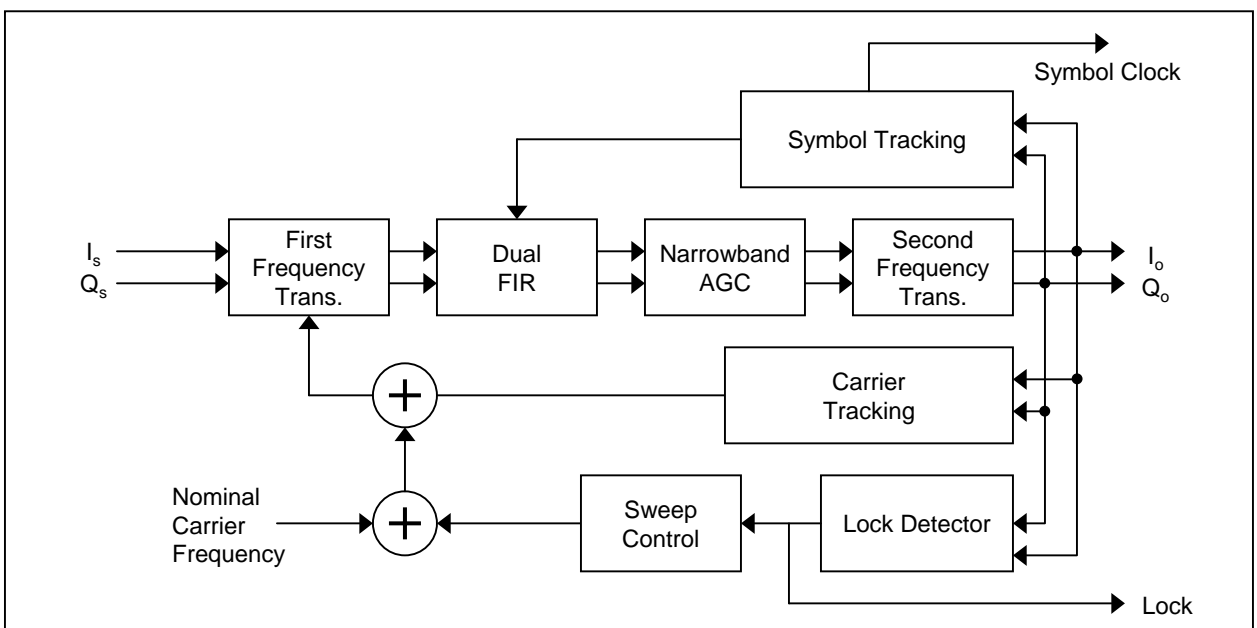
In addition to optimizing performance of the Viterbi decoder, the digital narrowband AGC also insures that the performance of the symbol timing and carrier tracking loops is independent of signal level variations. An analog wideband AGC is also employed to insure that the analog signal applied to the A/D converters is properly scaled.

Both the symbol timing and carrier tracking loops are implemented digitally, which eliminates the need for external connections to analog tuning components during steady state operation. This causes the requirements on the analog presampling filter to be relaxed, permitting a lower cost analog front end. For systems which require a narrow band presampling filter, and have the potential for significant frequency error in the LNB (several MHz) the HDM8516 provides a high resolution measure of carrier frequency to permit periodic readjustment of the front end tuner frequency to compensate for drift. The host processor periodically reads the frequency

register, then computes appropriate correction to the tuner frequency.

The nominal symbol rate and the nominal carrier frequency are programmed into the demodulator to an accuracy provided by 20 bits of resolution, and the system accuracy is equivalent to that of the fixed frequency sampling clock.

During initial acquisition, the HDM8516 provides an automated sweep program to facilitate carrier acquisition. The host processor loads a 20 bit register which determines the initial carrier frequency. A 16 bit register is programmed with the number of symbol times the receiver will dwell at each frequency. If the receiver remains at the initial frequency for the programmed number of symbol times without achieving lock, the carrier frequency is incremented by the step frequency value programmed into another 16 bit register. If no lock is achieved, the receiver will continue to increment the frequency until the maximum number of search frequencies, as determined by the value in an 8 register, is achieved. When the maximum number of search frequencies is reached, the carrier frequency returns to the initial value and the entire process is repeated. Once the host processor determines that lock is achieved by observing the lock flag, it then inhibits the sweep function and programs loop bandwidth parameters which are optimized for steady state performance.



**4. TECHNICAL OVERVIEW** (continued)

**4.3 NOISE MEASUREMENT CIRCUIT**

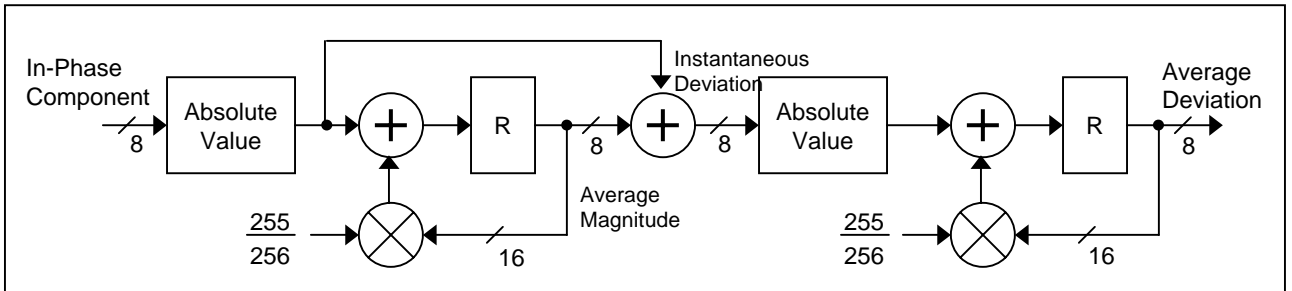
When the DBS system is being installed in any place, the most difficult part of the installation is accurate pointing of the antenna toward the satellite. Inaccurate pointing results in loss of margin and greater potential for outages in adverse weather conditions. Existing systems use information from the demodulator forward error correction circuits to provide a measure of antenna pointing. Unfortunately, this method is useful over a range of only several dB above system threshold.

The HDM8516 employs a unique circuit for accurate measure of signal strength over a 20 dB range of signal to noise ratio. This method, illustrated in the block diagram, makes use of the fact that the demodulator provides 8 bits of resolution for each of the quadrature output components. This high resolution provides a means of measuring the noise component with great

accuracy.

The eight bit in-phase demodulator filter output is detected by an absolute value circuit, then passed through an IIR to provide a measure of average signal amplitude. Each sample is then subtracted from this average amplitude to provide an instantaneous noise sample. The absolute value of these noise samples are then averaged by a second IIR to provide a measure of the noise which is roughly proportional to the noise power and inversely proportional to signal to noise ratio.

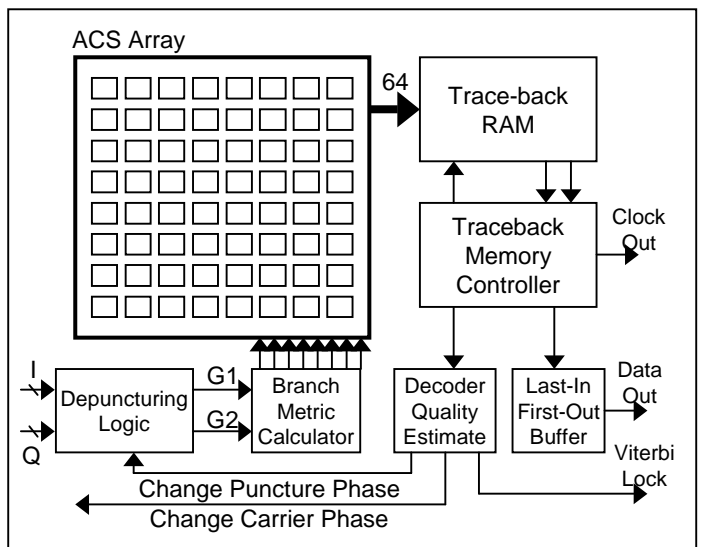
Finally, the Figure 16 illustrates the results of simulations under different noise conditions. This figure illustrates that for signal-to-noise ratio as high as 19 dB, the noise measurement circuit provides a meaningful measure of signal power with worst case resolution of 1 dB.



**4.4 VITERBI DECODER**

The Viterbi decoder accepts 4 bit soft decision samples of the in-phase (I) and quadrature (Q) components of the received signal. Once QPSK lock has been achieved, the decoder searches for the correct code rate, starting with rate 3/4, then proceeding to rate 2/3, 5/6, 7/8 and finally rate 1/2. Each of the possible synchronization phases at each rate is tested as well as the two possible carrier phase ambiguity conditions. Polarity reversal is corrected in the word synchronization logic. Viterbi lock is achieved when the trellis traceback algorithm converges, on the average, within a prescribed number of symbols.

Although the algorithm automatically tests for carrier phase ambiguity, there is no provision to automatically correct for phase reversal. Phase reversal can occur if the receiver chain, consisting of an LNB and the tuner, provides



## 4. TECHNICAL OVERVIEW (continued)

### 4.4 VITERBI DECODER (continued)

an odd number of high side frequency translation operations. an odd number of high side frequency translation operations. A system may be required to operate with different LNBS, some of which provide phase reversal. This condition may be corrected by the host processor, which can set a bit in the down converter to correct for phase reversal.

### 4.5 AUTONOMOUS ACQUISITION

The HDM8516 provides several features to permit signal acquisition with minimal interaction with the host microcontroller. The host microcontroller must configure the HDM8516 for a specific symbol rate, carrier frequency, carrier sweep conditions, and tracking loop bandwidth. The microcontroller also must monitor lock status to determine when acquisition is achieved. There are many provisions in the HDM8516 to enable the system designer to implement custom algorithms for specific requirements.

The microcontroller first must set the lower edge of the carrier search range in the Carrier Frequency registers (04, 05 and 06). Then the processor configures the Carrier Sweep Step Size register (09, 0A) to a value which is less than two times the carrier pull-in range. The number of symbols per dwell is defined in registers (0B,0C), and is typically set to a value of 500 to 1000. The total search range is set by the Number of Search Frequencies as defined in register 0D. The total sweep frequency range is this number times the Carrier Sweep Step Size. The sweep process stops once QPSK carrier lock is detected. If no lock is detected, the sweep process continuously repeats.

The QPSK demodulator may lock to any one of four different phase reference states, only one of which produces true I and Q data as it was modulated at the transmitter. If the local phase reference is plus 90 degrees or minus 90 degrees with respect to the true phase, the information provided to the Viterbi decoder will be unintelligible. If the Viterbi decoder is unable to achieve valid lock, it will reattempt lock with a 90 degree phase shift, without external intervention.

In the event that the local phase is 180 degrees from the true phase, the data provided to the Viterbi decoder will be inverted, but otherwise valid. The code employed by the Viterbi decoder is transparent

The Viterbi decoder employs the radix two algorithm. The output buffer re-serializes the data which is made available, along with the Viterbi data clock as external signals. These signals permit verification of the DVB specification which is referenced to the Viterbi decoder output.

thus the data from the Viterbi decoder will be inverted if the input is inverted. This situation is corrected in the word synchronization circuit. This circuit searches for the unscrambled sync word which occurs once per frame (every 204 bytes at the Viterbi output). Once correlation with the sync word is found, the data is reformatted as a series of bytes with the beginning of each 204 byte frame identified to provide the synchronization information required for the deinterleaver and the Reed Solomon decoder. If the polarity of the sync word is incorrect, the data is inverted before further processing without external interaction.

The HDM8516 supports five different code rates, including 1/2, 2/3, 3/4, 5/6 and 7/8. When rate 1/2 is employed, there is a one-to-one correspondence between incoming I and Q samples and G1 and G2 terms required by the Viterbi decoder. The higher rates employ punctured coding techniques which periodically cause either a G1 or G2 term to be deleted. The puncturing pattern can have 6 possible ambiguity states for rate 2/3, 4 states for rate 3/4, 6 states for rate 5/6 and 8 states for rate 7/8. As part of the Viterbi decoding acquisition process, each puncturing state of each code must be tested. Total acquisition requires search of 26 different conditions. The process starts with rate 3/4 coding and proceeds sequentially to rate 2/3, 5/6, 7/8, and finally rate 1/2.

In some systems, it may be possible to experience spectral inversion. This might occur when different combinations of LNBS and tuners are employed which implement different frequency translation schemes. Correction of spectral inversion must be corrected with host processor interaction. If the host processor detects that QPSK lock is achieved, but Viterbi lock has not occurred within a specified time, then a bit must be set in the demodulator which reverses the

**4. TECHNICAL OVERVIEW** (continued)

**4.5 AUTONOMOUS ACQUISITION** (continued)

spectrum.

SYMBOL	Bit Times	Symbols	Clock Cycles
Carrier Search	8,333	5,000	10,000
Viterbi Node Sync.	2,652	1,591	3,182
Byte Sync.	16,000	9,600	19,200
Deinterleaver Flush	19,584	11,750	23,500
Reed Solomon	1,632	979	1,958
Total Timing	48,201	26,950	57,840

The table above illustrates a typical acquisition timing. For this example, the symbol rate is one

half of the clock rate. The code rate is set to 5/6, which requires 13 trial and errors before node sync is achieved. The carrier search logic requires 10 dwells at different frequencies (500 symbols per dwell) before demodulator lock is achieved.

The total time required for acquisition could vary widely, depending upon the carrier search range and the time required for Viterbi node sync. For this example, however, the Byte Sync time and the time required to flush the deinterleaver dominates the total time. If a 90MHz clock were employed, the total acquisition time would be 0.642ms for this example

**4.6 REED SOLOMON DECODER**

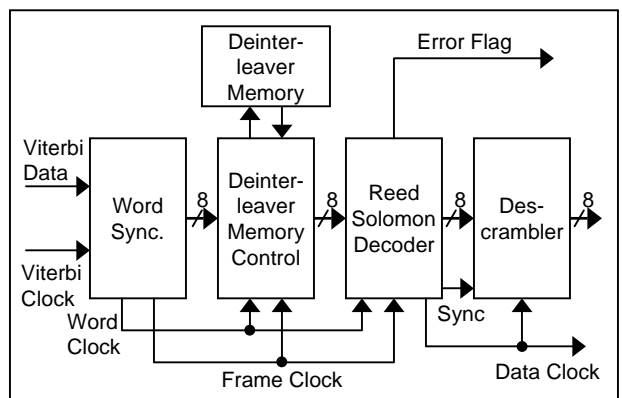
The serial output from the Viterbi is provided to the Word Sync circuits which searches for the eight bit frame sync word which occurs every 204 bytes. By detecting the polarity of the sync word, this module can correct polarity reversals in the data provided by the Viterbi decoder.

Byte serial data is provided to the convolutional deinterleaver, which reorders the received symbols. This process causes errors, which typically occur in bursts from the Viterbi decoder, to be distributed randomly over many blocks. This de-interleaved data is then provided to the Reed Solomon decoder which can reduce an error rate of  $2 \times 10^{-4}$  from the Viterbi decoder to less than 1 in  $10^{-10}$ . The Reed Solomon decoder accepts input data in blocks of 204 bytes and produces error corrected blocks of 188 bytes. Maximum 8 bytes per a RS block can be corrected in RS decoder. Reed-solomon block includes on-chip BER calculator at the output of Viterbi to monitor signal quality or estimate the SNR of incoming signal. The calculated value can be read by accessing two read registers via utility bus such as I2C. It represents the number of errors among  $2^{20}$  data bits.

The next process is descrambling, not to be confused with the descrambling which is part of conditional access. The purpose of scrambling the transmitted data and performing the inverse in the

receiver is to insure that the spectrum of the transmitted waveform is always evenly distributed without significant discrete spectral lines. Without the scrambling/descrambling process, a transmitted sequence of all ones or all zeroes would result in strong spectral components and could interfere with other signals in the same satellite transponder.

The final process is data regulation. Viterbi Data and Viterbi Clock occur irregularly according to the code rate. Data clock regulation makes it possible to interface with external common interface devices. To make external bus interface more flexible, interface mode such as parallel or serial can be selected by mode selection register.

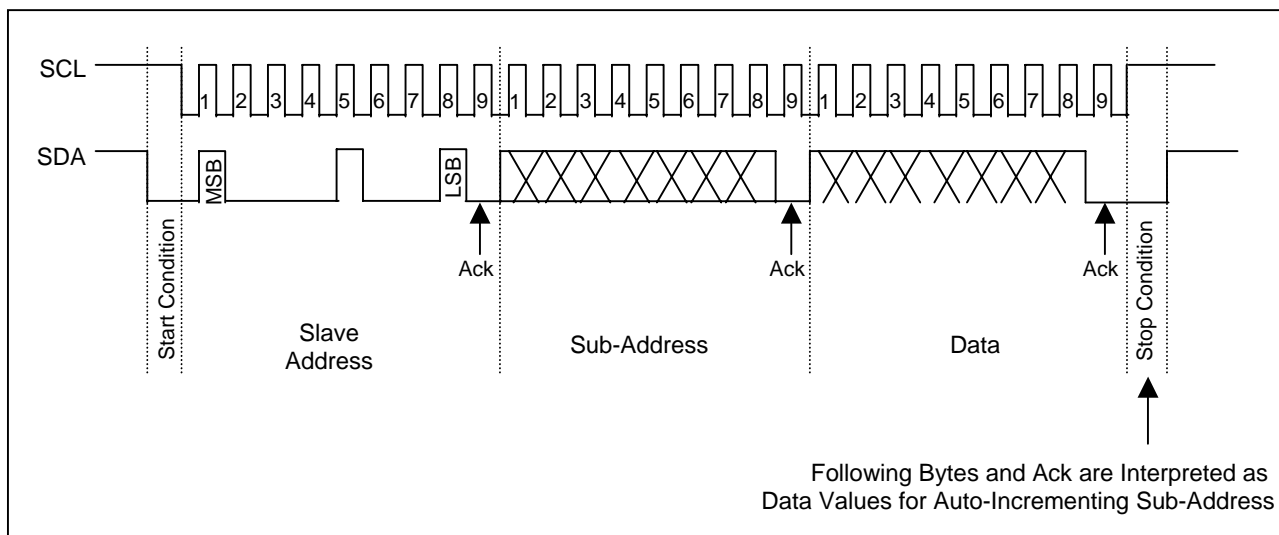


## 5. SERIAL PROGRAMMING INTERFACE

### 5.1 GENERAL

The HDM8516 utilizes a 2-wire serial programming interface(I2C) to program the device registers. The interface operates at 3.3 V input level.

The below Figure illustrates the timing relationship between the serial\_data(SDA) and serial\_clock (SCL) signals during a typical process. Both lines require external pull-up resistors.



Every data word must be 8 bits long (MSB first), followed by an acknowledge bit, generated by the receiving device. Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the slave address byte. If this is the HDM8516 address, the HDM8516 generates an acknowledge signal by pulling the SDA line low during the 9<sup>th</sup> clock pulse. During the acknowledge period, the master device must leave the SDA line high. The 8<sup>th</sup> bit of the device address byte is the read/write bit (high = read

from the addressed device, low = write to the addressed device).

Data bytes are always acknowledged during the 9<sup>th</sup> clock pulse by the addressed device.

Untimely termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the HDM8516 remains in the state defined by the last complete data byte transmitted, and any master acknowledge subsequent to reading the device address is ignored.

### 5.2 DEVICE ADDRESS

The HDM8516 device address is configured by the state of the ADDR. External ADDR pin set the state of the 7 MSBs of the HDM8516 slave address. Therefore, the device address can be configured from 74 to 75 as listed in right Table. Since bit 0 of the slave address is a Read/Write bit, the device address is given as the 7 MSBs of the slave address. Subsequent read and write addresses are given in right Table.

ADDR	7bit Device Address	8bit Device Write Address	8bit Device Read Address
0	0000000	00000000	00000001
1	0000001	00000010	00000011

**5. SERIAL PROGRAMMING INTERFACE** (continued)

**5.3 WRITE PROCESS**

A write process involves sending the device address byte with the read/write bit low, and following it with one or more bytes. The first byte following the device address byte is always assumed to be a register address, and sets an internal register address pointer. This address is an 7-bit quantity, thus allowing the addressing of up to 128 byte-wide registers. If a second byte follows the device address byte, it is assumed to be the write data for the register indexed in the first byte. Any subsequent bytes are assumed to be write data for registers whose address follows in ascending order, as the internal address pointer is incremented at the

completion of each register write. The state of this internal address pointer upon exiting a write transaction is used for any read transactions that follow.

Below Figure illustrates a typical register write sequence.

1. Master transmits the device address with the read/write bit low.
2. Master transmits the desired register address.
3. Master transmits the register write data byte.
4. Subsequent registers are written until a top condition is detected.

**Writing Sequence**



S = Start Condition  
 P = Stop Condition  
 A = Acknowledge



From Master



From HDM8516

**5.4 READ PROCESS**

A read transmission involves sending the device address byte with read/write bit high, and receiving one or more bytes. The first byte returned after the device address byte makes up the contents of the last indexed register address. Any subsequent data bytes read come from registers whose address follows in ascending order as the internal address pointer is incremented at the completion of every read. The initial register address depends on the state of the pointer at the end of the last write transaction. Because writing even one data byte to a register will increment the address pointer, typically one would want to precede a read with a write transaction that sends only the register address

byte.

Below Figure illustrates a typical register read sequence.

1. Master transmits the device address with the read/write bit low.
2. Master transmits the desired register address.
3. Master generates repeat start.
4. Master transmits the device address with the read/write bit high.
5. Slave(HDM8516) transmits the data byte to master.
6. Subsequent registers are written until a top condition is detected.

**Read Sequence**



S = Start Condition  
 P = Stop Condition  
 A = Acknowledge  
 RS = Repeat Start Condition  
 NA = Not Acknowledge



From Master



From HDM8516

## 6. FUNCTIONAL DESCRIPTION

### 6.1 CLOCK GENERATION PLL

An integrated VCO is locked to MxN times a reference frequency provided by an external clock.

#### 6.1.1. Determining Output Frequency

Fully programmable feedback and reference divider capability allows virtually any frequency to be generated, not just simple multiples of reference frequency. There are two status exist

PLL Disable Mode	PLL Enable Mode
The PLL is bypassed and the external clock is directly connected to the Internal clock	The internal clock is connected to the generated clock of the PLL.

##### 6.1.1.1 PLL disable mode

PLL control setting is as follows TDM (Bit 7 of 0x23 register) is set to one and BYPASS (Bit 4 of 0x23 register) is set to one.

##### 6.1.1.2 Normal Frequency mode

Output frequency range is limited to 160MHz. PLL control setting is as follows. TDM (Bit 7 of 0x23 register) is set to zero, and BYPASS (Bit 4 of 0x23 register) is set to zero. At this condition, the output frequency, F(ck), is actually determined by the following equation.

$$F(ck) = \frac{F(ref) \times (Feedback\ divisor)}{(Reference\ divisor)}$$

F(ck) : Frequency of output

F(ref): Frequency of reference input

Feedback divisor : M[13:0]+2,  
(0x25 and 0x26 registers)

Reference divisor : N[7:0]+1, (0x27 register)

##### 6.1.1.3 Extended Frequency mode

Output frequency range is limited to 320MHz. PLL control setting is as follows. TDM (Bit 7 of 0x23 register) is set to zero, and BYPASS (Bit 4 of 0x23 register) is set to one. At this condition, the output frequency, F(ck), is actually determined by the following Equation

$$F(ck) = \frac{F(ref) \times (Feedback\ divisor) \times (Pre\ divisor)}{(Reference\ divisor)}$$

Pre divisor :  $2^{p[1:0]+1}$ , p is Bit 2 and 3 of 0x23 register

#### 6.1.2. PLL Control Parameter setting

Para	Description
M	Feedback divisor
N	Reference divisor
p	Pre divisor
vc	VCO range control vector
lfm	Loop filter mode selector
icp	Charge pump bias current control vector

##### 6.1.2.1. vc value setting

According to Output clock frequency, determine the vc values

vc [1:0]	[1:0]	Output Clock Frequency		Unit
		min	max	
00	00	40	100	MHz
	01	20	50	
	10	10	25	
	11	5	12.5	
01	00	60	100	
	01	30	50	
	10	15	25	
	11	7.5	12.5	
10	00	80	100	
	01	40	50	
	10	20	25	
	11	10	12.5	
11	00	100	100	
	01	50	50	
	10	25	25	
	11	12.5	12.5	

##### 6.1.2.2 lfm value setting

According to Table, determine the lfm values

lfm	$\frac{(Reference\ Frequency)}{(15 \times Reference\ Divisor)}$
7	< 0.01555
0	< 0.0258
1	< 0.0421
2	< 0.070
3	< 0.114
4	< 0.187
5	< 0.309
6	> 0.309

**6. FUNCTIONAL DESCRIPTION**(continued)

**6.1 CLOCK GENERATION PLL**(continued)

6.1.2.3. icp value setting

According to lfm value, determine the icp values.

lfm	Zero value	Pole value	r1f value
7	External Filter Used		
0	0.008	0.03	40
1	0.013	0.050	24.1
2	0.021	0.082	40
3	0.032	0.135	24.1
4	0.060	0.221	24.1
5	0.100	0.360	14.7
6	0.160	0.600	8.9

According to the following Step, each parameters (Kvcop, Kpll, Kpd, Temp value, icp) are determined

Step	Formula
1	$K_{vcop} = \frac{100}{2^P}$
2	$K_{pll} = \sqrt{(\text{Zero value} \times \text{Pole value})}$
3	$K_{pd} = \frac{1000 \times K_{pll} \times \text{Feedback Divisor}}{K_{vcop} \times r1f}$
4	Temp value = $2 \times 3.14 \times K_{pd}$
5	$icp = 16.5 - \frac{16 \times \text{temp value}}{40}$

Note P: Pre Divisor.  
If icp value has fraction, truncate it.

**6.2 DiSEqC Interface**

The DiSEqC system is a communication bus between satellite receivers and satellite peripheral equipment, using only the existing coaxial cable.

6.2.1. DiSEqC mode

According to the value of DiSEqC\_mode of 0x31 register, DiSEqC mode can be changed

- 0: 22KHz tone off
- 1: 22KHz tone on
- 2: Burst mode - on for 12.5ms = '0'
- 3: Burst mode - modulated 1:2 for 12.5ms = '1'
- 4: Modulated with bytes from DiSEqC instruction

6.2.2 DiSEqC instruction

Up to eight instruction data bytes are loaded into a bank of registers(0x29 -0x30).I2C automatic register address incrementing is turn on.The number of bytes in the DiSEqC instruction must be defined in the DiSEqC\_length of 0x31 register.

When the DiSEqC instruction data bytes have been loaded, set DiSEqC\_mode of 0x31 register. At the same time, program DiSEqC\_length of 0x31register. The instruction data is modulated onto 22KHz signal and output from the DISEQC pin.

**7. REGISTER MAP**
**7.1 WRITE REGISTER MAP**

Sub Address	Default	D7	D6	D5	D4	D3	D2	D1	D0	
00	66	qs_symnco[19:12]								
01	66	qs_symnco[11:4]								
02	60	qs_symnco[3:0]				Reserved				
03	A5	qs_symk2				qs_symk1				
04	F7	qs_carnco[19:12]								
05	D0	qs_carnco[11:4]								
06	00	qs_comnco[3:0]				Reserved				
07	C6	qs_cark2_search				qs_cark1_search				
08	C6	qs_cark2_lock				qs_cark1_lock				
09	00	qs_carswpstep[15:8]								
0A	83	qs_carswpstep[7:0]								
0B	03	qs_symperdwel[15:8]								
0C	E8	qs_symperdwel[7:0]								
0D	20	qs_nbrsrchfreq								
0E	80	qs_nbagcinit								
0F	5F	auto_spt	qs_agctrken	qs_freqswphold	qs_cartrken	qs_symtrken	qs_iqbiasadjen	man_spctinv	qs_twoscompl	
10	EF	rs_reset	vb_reset	carswprst	Reserved	nbagcaccrst	wbabcaccrst	carphaccrst	symphaccrst	
11	01	qs_wbagcgain			Reserved	qs_inbhold	s_wbagchold	qs_wbagcinvl	qs_wbagcmode	
12	20	qs_period								
13	7F	qs_sigdelta2ctl								
14	07	Reserved					test_reg			
15	C2	pr_stopsync_state				pr_downsync_state				
16	01	pr_upinsync_state								
17	01	pr_stable_state								
18	04	bpsk_mode	dss_mode	auto_coderate	hi_coderate			vb_vbonly	Reserved	
19	1E	Reserved	vb_r1_2th							
1A	1E	Reserved	vb_r2_3th							
1B	28	Reserved	vb_r3_4th							
1C	3C	Reserved	vb_r5_6th							
1D	3C	Reserved	vb_r6_7th							
1E	3C	Reserved	vb_r7_8th							
1F	00	Reserved					regulate_data_clk	clk_pol	mode_serial	

**7. REGISTER MAP** (continued)

**7.1 WRITE REGISTER MAP** (continued)

Sub Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
20	01	Reserved						lookup_frame_err	auto_set_ebit
21	10	wbagc_freq_down	Reserved	qs_wbagc_thres					
22	02	Reserved					qs_factor		
23	00	diseqc_frame							
24	00	diseqc_address							
25	00	diseqc_com							
26	00	diseqc_data_1							
27	00	diseqc_data_2							
28	00	diseqc_data_3							
29	00	diseqc_data_4							
2A	00	diseqc_data_5							
2B	01	diseqc_length				diseqc_mode			diseqc_bypass
30	91	bypass_pll	pll_pd	pll_vcopd	pll_TDM	pll_p		pll_VC	
31	29	pll_tpdud		pll_LFM			pll_cnttest	Reserved	l2c_bypass
32	80	bypass_clk	kill	Rerved	pll_m[13:8]				
33	2B	pll_m[7:0]							
34	01	pll_n							
35	01	Reserved		data_ctrl_sel	Rerved	pll_icp			

**7.2 READ REGISTER MAP**

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
00	qs_nbagc_accum							
01	qs_symfreq_acc[23:16]							
02	qs_symfreq_acc[15:8]							
03	qs_symfreq_acc[7:0]							
04	qs_carphase_acc[23:16]							
05	qs_carphase_acc[15:8]							
06	qs_carphase_acc[7:0]							
07	Reserved							qs_qpsklock
08	qs_wbagcacc							
09	qs_swpfreq[15:8]							

**7. REGISTER MAP** (continued)

**7.2 READ REGISTER MAP** (continued)

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
0A	qs_swpfreq[7:0]							
0B	Reserved		qs_iout					
0C	Reserved		qs_qout					
0D	qs_noiseplr							
0E	ber_vit[15:8]							
0F	ber_vit[7:0]							
00	qs_carphase1[23:16]							
11	qs_carphase1[15:8]							
12	qs_carphase1[7:0]							
13	qs_carphase2[19:12]							
14	qs_carphase2[11:4]							
15	qs_carphase2[3:0]				Reserved			
16	sigqlty[23:16]							
17	sigqlty[15:8]							
18	sigqlty[7:0]							
19	Reserved					vb_coderate[2:0]		
1A	Reserved				rs_errors			
1B	Reserved			inversion_sig	inversion_byte	parallel_lock	rs_framesync	vb_nodesync
1C	count_coted_err[15:8]							
1D	count_coted_err[7:0]							
1E	count_undoted_err							
1F	HDM8516_ID[7:0] (F1)							
20	qs_lockaccum[9:2]							
21	qs_lockaccum[1:0]		Reserved					
22	Reserved							diseqc_end
31	ncb[7:0]							
32	Reserved		mc[13:8]					
33	mc[7:0]							
34	Reserved							pll_lock
NOTE(S)	1) Sub-address values in this table are hexadecimal 2) Default values in this table are hexadecimal 3) Reserved bits should be set to zero when writth and will return zero when read							

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION**

Field	Default Value	Register	Description																					
qs_symnco	66 66 6	00[7:0] 01[7:0] 02[7:4]	<p><b>Symbol Timing Frequency</b> The 20 bit straight binary number in this field establishes the symbol timing frequency utilized within the demodulator. Bit 7 of address 00 is the MSB and bit 4 of address 02 is the LSB. If <math>R_s</math> is the symbol rate and <math>f_c</math> is the clock frequency, the value to be stored in this 20 bit field is the integer portion of <math>R_s(2^{20})/f_c</math>.</p>																					
qs_symk2 qs_symk1	A 5	03[7:4] 03[3:0]	<p><b>Symbol Timing Loop Gain Control</b> This field establishes the K1 and K2 gain values for the second order loop filter of the symbol tracking loop. Bits 0,1,2 and 3 determine the straight-through gain, and bits 4,5,6 and 7 determine the integration path gain. The nominal value of this parameter in Hex, is expressed below for different ranges of symbol rate to clock rate ratios:</p> <table border="1"> <thead> <tr> <th>Clock/Symbol Rate</th> <th>Value</th> </tr> </thead> <tbody> <tr><td>2</td><td>FB</td></tr> <tr><td>4</td><td>DA</td></tr> <tr><td>8</td><td>B9</td></tr> <tr><td>16</td><td>98</td></tr> <tr><td>32</td><td>77</td></tr> <tr><td>64</td><td>56</td></tr> </tbody> </table>	Clock/Symbol Rate	Value	2	FB	4	DA	8	B9	16	98	32	77	64	56							
Clock/Symbol Rate	Value																							
2	FB																							
4	DA																							
8	B9																							
16	98																							
32	77																							
64	56																							
qs_carnco	F7 D0 0	04[7:0] 05[7:0] 06[7:4]	<p><b>Carrier Frequency</b> The 20 bit, two's complement number in this field establishes the nominal carrier frequency of the demodulator. Bit 7 of address 04 is the MSB and bit 4 of address 06 is the LSB. The number in this 20 bit field multiplied by the clock frequency divided by <math>2^{20}</math> is the carrier frequency in Hertz. When the carrier sweep function is active, this value defines the starting frequency.</p>																					
qs_cark2_search qs_cark1_search qs_cark2_lock qs_cark1_lock	C 6 C 6	07[7:4] 07[3:0] 08[7:4] 08[3:0]	<p><b>Carrier Loop Filter Control</b> This field establishes the K1 and K2 gain values for the second order loop filter of the carrier tracking loop. Bits 0,1,2 and 3 determine the straight-through gain, and bits 4,5,6 and 7 determine the integration path gain. The nominal value of this parameter in Hex, is expressed below for different ranges of symbol rate to clock rate ratios. Two loop filter configurations are provided at each symbol rate, one for steady state operation(08) and one which is used only for acquisition(07) to permit greater frequency pull-in. Initially the gains are set to acquisition values. When QPSK_LOCK is achieved, they are automatically switched to steady state values.</p> <table border="1"> <thead> <tr> <th>Clock/Symbol Rate</th> <th>Steady State</th> <th>Acqu.</th> </tr> </thead> <tbody> <tr><td>2</td><td>C7</td><td>C7</td></tr> <tr><td>4</td><td>A7</td><td>A7</td></tr> <tr><td>8</td><td>87</td><td>87</td></tr> <tr><td>16</td><td>67</td><td>67</td></tr> <tr><td>32</td><td>47</td><td>47</td></tr> <tr><td>64</td><td>27</td><td>27</td></tr> </tbody> </table>	Clock/Symbol Rate	Steady State	Acqu.	2	C7	C7	4	A7	A7	8	87	87	16	67	67	32	47	47	64	27	27
Clock/Symbol Rate	Steady State	Acqu.																						
2	C7	C7																						
4	A7	A7																						
8	87	87																						
16	67	67																						
32	47	47																						
64	27	27																						

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
qs_carswpstep	00 83	09[7:0] 0A[7:0]	<b>Carrier Sweep Step Size</b> This 16 bit value defines the size of the step of each carrier frequency dwell. Bit 7 of address 09 is the MSB and bit 0 of address 0A is the LSB. The number in this register is divided by $2^{16}$ , and multiplied by the clock frequency to determine the frequency step increment.
qs_symperdwell	03 E8	0B[7:0] 0C[7:0]	<b>Symbols Per Dwell</b> This 16 bit value defines the time, in symbol periods, for which the demodulator will dwell before making the next frequency step in a sweep. Bit 7 of address 0B is the MSB and bit 0 of address 0C is the LSB.
qs_nbrsrchfreq	20	0D[7:0]	<b>Number of Search Frequencies</b> This 8 bit field determines the number of frequency steps which occur during the frequency sweeping process. Combined with the frequency step size, this determines the frequency span of the carrier sweep
qs_nbagcinit	80	0E[7:0]	<b>Narrow Band AGC initial value</b> This 8 bit field establishes the initial gain of the narrow band AGC. High numbers correspond to low gain associated with low symbol rates. If the narrowband AGC function is enabled, this number is used as a starting point and the closed loop will seek the optimum setting without processor interaction.
auto_spt qs_agctrken qs_freqswphold qs_cartrken qs_symtrken qs_iqbiasadjen man_spctinv qs_twoscompl	0 1 0 1 1 1 1 1	0F[7] 0F[6] 0F[5] 0F[4] 0F[3] 0F[2] 0F[1] 0F[0]	<p><b>Bit 7. Automatic Detection of Spectrum Inversion</b> When this bit is set to one, the spectrum inversion is detected automatically.</p> <p><b>Bit 6. Narrowband AGC Mode 1 Enable</b> When this bit is set to one and the narrowband AGC is in Mode 1, the narrowband AGC self-adjusts to the optimum gain setting. When the bit is set to zero, the most recent value is held without updating.</p> <p><b>Bit 5. Sweep Hold</b> When this bit is set to one, the sweeping process is inhibited, and the nominal carrier frequency remains at the last value.</p> <p><b>Bit 4. Carrier Track Enable</b> When this bit is set to one, the carrier phase tracking function is enabled. When this bit is zero, the carrier frequency is forced to the 20 bit programmed value.</p> <p><b>Bit 3. Symbol Track Enable</b> When this bit is set to one, the symbol tracking function is enabled. When this bit is zero the symbol tracking frequency is forced to the nominal 20 bit programmed value.</p> <p><b>Bit 2. Bias Cancel Enable</b> When this bit is a one, the internal circuit which cancels DC bias on the I and Q inputs is enabled. When this function is enabled, it is assumed that the input signal is scrambled with no significant DC component on either the I or Q.</p> <p><b>Bit 1. Spectrum Invert</b> When this bit is set to one, the spectrum of the received signal is inverted. This has the effect of complementing the in-phase channel only.</p> <p><b>Bit 0. Binary/Two's Complement</b> When this bit is a zero, the system expects the six bit modulation input samples in two's complement format, otherwise the input should be in offset binary format.</p>

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
rs_reset	1	10[7]	<p><b>Bit 7. Reed Solomon Error Counter</b> When this bit is set to zero, the counters for the number of corrected errors and the number of uncorrected code words are cleared to zero.</p> <p><b>Bit 6. Viterbi Reset</b> When this bit is set to zero, the accumulator for the signal quality is cleared to zero. In normal operation, this bit is set to one.</p> <p><b>Bit 5. Carrier Sweep Function</b> When this bit is set to zero, the sweep function is disabled and the carrier frequency is forced to the preset value defined in register locations 04, 05 and 06.</p> <p><b>Bit 4. Reserved</b></p> <p><b>Bit 3. Narrowband AGC Accumulator</b> When this bit is set to zero, the accumulator in the narrowband AGC is cleared to the initial value defined in location 0E. In normal operation, this bit is set to one.</p> <p><b>Bit 2. Wideband AGC Accumulator</b> When this bit is set to zero, the accumulator in the wideband AGC is cleared to zero. In normal operation, this bit is set to one. When the wideband AGC is set to Mode 0, this bit has no effect as the integrator must be implemented in the external analog circuits.</p> <p><b>Bit 1. Carrier Phase Tracking Frequency Accumulator</b> When this bit is set to zero, the frequency accumulator in the carrier phase tracking loop is cleared to zero. This bit must be set to one in tracking operation to implement a second order loop filter otherwise the loop is first order.</p> <p><b>Bit 0. Symbol Timing Frequency Accumulator</b> When this bit is set to zero, the frequency accumulator in the symbol tracking loop is cleared to zero. This bit must be set to one in normal tracking operation to implement a second order tracking loop, otherwise the loop is first order.</p>
vb_reset	1	10[6]	
carswprst	1	10[5]	
nbagcacrst	1	10[3]	
wbagcacrst	1	10[2]	
carphacrst	1	10[1]	
sympacrst	1	10[0]	
qs_wbagcgain	000	11[7:5]	<p><b>Bits [7:5]. WB AGC Gain</b> This three bit field defines the time constant of the WB AGC in Mode 1. A value of zero corresponds to the shortest time constant and 7 corresponds to the slowest time constant.</p> <p><b>Bit 4. Reserved</b></p> <p><b>Bit 3. LNB Hold</b> When this bit is set to one, the output of LNB-Tone is held on zero.</p> <p><b>Bit 2. WB AGC Hold</b> During normal tracking operation, this bit is set to one. When this bit is set to zero and the wideband AGC is in Mode 1, the digital integrator is held to the most recent value and loop updates are inhibited.</p> <p><b>Bit 1. WB AGC Invert</b> When this bit is set to zero a high duty factor on the WB AGC output corresponds to too much gain. When the control bit is set to one, high duty factor corresponds to not enough gain.</p> <p><b>Bit 0. Wideband AGC Mode</b> When this bit is set to zero (Mode 0), the WB AGC output must be filtered with an external integrating analog filter to implement a first order feedback loop. When this bit is one (Mode 1), a digital integrator within the HDM8516 performs this function and the only external analog function required is a low pass filter to remove the high frequency components of the sigma delta converter output.</p>
qs_lnbhold	0	11[3]	
qs_wbagchold	0	11[2]	
qs_wbagcinv	0	11[1]	
qs_wbagcmode	1	11[0]	

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
qs_period	20	12[7:0]	<p><b>LNB Tone</b> This eight bit value establishes the control for LNB tone generator. If <math>f_L</math> is the desired frequency and <math>f_C</math> is the clock frequency, the value to be stored in this 8 bit field is the integer portion of <math>f_L(2^{17})/f_C</math>. The default value(20H) generates 22KHz tone at 90MHz sampling clock.</p>
qs_sigdelta2ctl	7F	13[7:0]	<p><b>Sigma Delta</b> This eight bit input value establishes the control for Sigma Delta converter. This function is independent of other demodulator functions and is provided as control for external analog components.</p>
test_reg	111	14[2:0]	<p><b>Bits [2:0]. Test port Configuration</b>  <b>00H</b> Output is tristate.  <b>01H</b> Test bits [13:8] provide the I baseband filter output. Test bits [5:0] provide the Q baseband filter output. This information is updated once per symbol period.  <b>02H</b> Test bits [15:0] provide the sixteen most significant bits of the demodulator carrier phase test bits. This information is updated once per symbol period.  <b>03H</b> Test bits [15:0] provide the sixteen most significant bits of the demodulator symbol phase test bits. This information is updated once per symbol period.  <b>04H</b> Test bits [15:8] provide the Reed Solomon output data. Test bits [7:0] provide the deinterleaver output data. This information is updated at the Reed Solomon clock rate; when the transport stream output is configured to parallel output mode, DATA_CLK may be used as an output clock for this data.  <b>05H</b> All Zero.  <b>06H</b> Test bits [13:8] provide the six bit I-channel data from the ADC. Test bits [5:0] provides the six bit Q-channel data from the ADC. This information is updated at the fixed rate sample clock.  <b>07H</b> In this mode the test pins are used as input pins. The internal ADC is disabled, and the inputs at the test pins are fed directly to the demodulator. Test bits [13:8] are used as I-channel input and test bits [5:0] are used as Q-channel input. This information is updated at the fixed rate sample clock.</p>
pr_stopsync_state pr_downsync_state	C2	15[7:4] 15[3:0]	<p><b>Viterbi Lock Threshold</b>  <b>Bit[7:4]</b> defines the lock threshold for VB_NODES SYNC. Viterbi decoder decides that the correct code rate has been found. A large number means it takes longer to find the correct code rate in automatic detection mode. It should be greater than 7. The default value is 12.  <b>Bit[3:0]</b> defines the lock fail threshold. Viterbi decoder rejects a code rate and moves on to the next code rate. A small number means Viterbi decoder tries more data before it moves to the next code rate. It should be less than 7. The default value is 2.</p>

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
pr_upinsync_state	01	16[7:0]	<b>Viterbi Unlock Threshold</b> This number defines the threshold to maintain the Viterbi lock state. A large number means it needs more bad data to get out of the viterbi lock state and re-start searching the correct code rate. The default value is 1.
pr_stablestate	01	17[7:0]	<b>Viterbi Byte-Sync control</b> Once the viterbi lock(VB_NODESYNC) is achieved, the Viterbi decoder tries to find the byte-sync. This 8-bit register is used to set "unlock-threshold" for the byte-sync. Large number means it needs more bad-data to get out of the byte-sync state, i.e. less sensitive to noise. The default value is 1.
bpsk_mode dss_mode auto_coderate hi_coderate vb_vbonly	0 0 0 001 0	18[7] 18[6] 18[5] 18[4:2] 18[1]	<p><b>Bit 7. BPSK Mode</b> When this bit is set to 0, the demodulator assumes the incoming data is QPSK-modulated. When this bit is set to 1, the demodulator assumes the incoming data is BPSK-modulated.</p> <p><b>Bit 6. DSS Mode</b> When this bit is set to 0, this device operates as DVB mode. When this bit is set to 1, this device operates as DSS mode. In that case, the roll-off factor of the Nyquist filter is set to 0.2. The default is 0 (DVB).</p> <p><b>Bit 5. Viterbi Auto Decoding Mode</b> When this bit is set to 1, the Viterbi decoder automatically finds the correct code rate of the incoming signal. When this bit is set to 0, the code rate is set to the user-defined value at bit[4:2]. The default is 0.</p> <p><b>Bit [4:2]. Depuncturing Rate</b> It defines the depuncturing rate of the Viterbi decoder. When vb_autocode is disabled, the depuncturing rate is set to this value.</p> <p style="margin-left: 40px;">0 --- 1/2 1 --- 2/3 2 --- 3/4 3 --- 5/6 4 --- 7/8 5 --- 6/7</p> <p><b>Bit 1. MPEG2 Data</b> "0" (default) means the incoming data is MPEG2 decoded. In this mode a sync byte is expected every 188 bytes."1" means non-MPEG2 data. The Viterbi decoder doesn't check the existence of the sync byte.</p> <p><b>Bit 0. Reserved</b></p>
vb_r1_2th	1E	19[6:0]	<b>Rate 1/2 Threshold Select</b> This seven bit parameter defines the threshold used in the Viterbi decoder node synchronization process. For rate 1/2, the nominal value is 30 (1EH).
vb_r2_3th	1E	1A[6:0]	<b>Rate 2/3 Threshold Select</b> This seven bit parameter defines the threshold used in the node synchronization process. For rate 2/3, the nominal value is 30 (1EH).
vb_r3_4th	28	1B[6:0]	<b>Rate 3/4 Threshold Select</b> This seven bit parameter defines the threshold used in the node synchronization process. For rate 3/4, the nominal value is 40 (28H).
vb_r_5_6th	3C	1C[6:0]	<b>Rate 5/6 Threshold Select</b> This seven bit parameter defines the threshold used in the node synchronization process. For rate 5/6, the nominal value is 60 (3CH).

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
vb_r6_7th	3C	1D[6:0]	<b>Rate 6/7 Threshold Select</b> This seven bit parameter defines the threshold used in the node synchronization process. For rate 6/7, the nominal value is 60 (3CH).
vb_r7_8th	3C	1E[6:0]	<b>Rate 7/8 Threshold Select</b> This seven bit parameter defines the threshold used in the node synchronization process. For rate 7/8, the nominal value is 60 (3CH).
regulate_data_clk clk_por mode_serial	0 0 0	1F[2] 1F[1] 1F[0]	<b>Bit 2. Regulated Data Clock</b> Enables/Disables the data and data clock regulator. When this bit is set to 1, data output and data clock are regulated by FIFO operation. When this bit is set to 0, internal data output and internal data clock are by-passed <b>Bit 1. Clock Polarity</b> This bit is used to select the DATA_CLK polarity either for serial or parallel transport interface. If this bit is set to zero(default value), the transport data and control signals are latched at the positive edge of DATA_CLK. Otherwise, the signals are latched at the negative edge of DATA_CLK. <b>Bit 0. Parallel or Serial Output</b> Controls the transport stream output of the 8515 to serial or parallel mode. "0" (default) means the 8515 MPEG output is parallel. "1" means the 8515 MPEG output is serial. The LSB of the data bus(data[0] - pin 98) is used as the serial output pin
auto_set_ebit	7F	20[0]	<b>Bit 0. Transport error Indicator Enable/Disable</b> Enables/Disables the transport error indicator, 1 bit indicator in transport header. When this bit is set to 1 and if transport error is internally detected the transport error indicator bit is set to 1. When zero this functionality is disabled.
wbagc_freq_down qs_wbagc_thres	0 10	21[7] 21[5:0]	<b>Bit 7. Wideband AGC Frequency down</b> It regulates wide band AGC frequency. When this bit is set to zero, system clock for wide band AGC frequency is sampling clock. Otherwise, system clock for wide band AGC frequency become sixteen times of sampling clock frequency. <b>Bits [5:0]. Wideband AGC threshold</b> It determines the threshold of wide band AGC accumulator. This value controls the magnitude of ADC input.
qs_factor	2	22[2:0]	<b>Scaling factor</b> This value manages to scale the soft decision demodulator outputs to the proper levels for the 4 bit soft decision Viterbi inputs. If an overflow is detected, the output is limited to maximum or minimum 6 bit values. The upper four bits of this result are passed to the Viterbi decoder. <b>00H</b> QPSK output <b>01H</b> QPSK output * 1.25 <b>02H</b> QPSK output * 1.5 <b>03H</b> QPSK output * 1.75 <b>04H</b> QPSK output * 2.00 <b>05H</b> QPSK output * 2.25 <b>06H</b> QPSK output * 2.5 <b>07H</b> QPSK output * 2.75

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
diseqc_frame	00	23[7:0]	<b>DiSEqC message frame byte</b> It defines the format of frame in DiSEqC message.
diseqc_address	00	24[7:0]	<b>DiSEqC message address byte</b> It defines the format of slave address in DiSEqC
com	00	25[7:0]	<b>DiSEqC message command byte</b> It defines the format of command in DiSEqC message
data_1 data_2 data_3 data_4 data_5	00 00 00 00 00	26[7:0] 27[7:0] 28[7:0] 29[7:0] 2A[7:0]	<b>DiSEqC message data byte(s)</b> For some DiSEqC message, additional data is carried in one or more subsequent data byte(s).
diseqc_length diseqc_mode bypass_diseqc	00 000 1	2B[7:4] 2B[3:1] 2B[0]	<b>Bits [7:4] DiSEqC message length</b> Number of byte in DiSEqC instruction, to output on DISEQC pin. <b>Bits [3:1] DiSEqC mode</b> It determines one of following DiSEqC modes. 0: 22KHz off 1: 22KHz on continuous 2: Burst mode - on for 12.5ms = '0' 3: Burst mode - modulated 1:2 for 12.5ms = '1' 4: Modulated with bytes from DiSEqC instruction. 5-7: Reserved <b>Bit 0. DiSEqC By-pass</b> When this bit is set to 1, the function of DiSEqC interface is disabled. When this bit is set to 0, DiSEqC interface is enabled, The default is 1.
pll_bypass pll_pd pll_vcopd pll_TDM pll_p pll_VC	1 0 0 1 00 01	30[7] 30[6] 30[5] 30[4] 30[3:2] 30[1:0]	<b>Bit 7. PLL by-pass</b> If this bit is set to 0 and Digital part test mode (Bit 4 of this register) is set to 0, then PLL Normal frequency mode is selected. Else if this bit is set to 1 and digital part test mode is set to 0, then PLL Extended frequency mode is selected. <b>Bit 6. PLL power down mode except VCO</b> When this bit is set to 1, PLL power down and digital circuits do not operate and charge pump is disabled. <b>Bit 5. VCO power down mode</b> When this bit is set to 1, VCO power down and does not oscillate. <b>Bit 4. Digital part test mode</b> When this bit is set to 1 and Bit 7 of this register is set to 1, the PLL is bypassed and the external clock signal is directly connected to the internal clock. When this bit is set to 0, the generated clock of the PLL is connected to the internal clock. The default is 1. <b>Bits [3:2]. Pre divisor</b> In case of Extended Frequency mode, this value is used the calculation of output Frequency. Default value is 0. <b>Bits [1:0]. VCO range control vector</b> Default value is 1.

**7. REGISTER MAP** (continued)

**7.3 WRITE REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
pll_tpdud pll_LFM pll_cnttest I2c_bypass	00 101 0 1	31[7:6] 31[5:3] 31[2] 31[0]	<p><b>Bits [7:6]. Charge pump test mode</b> Internal used Only. The default is 0.</p> <p><b>Bits [5:3]. Loop filter mode selector</b> The default is 5H.</p> <p><b>Bit 2. Counter toggle test</b> Internal used Only. The default is 0.</p> <p><b>Bit 1. Reserved</b></p> <p><b>Bit 0. I2C by-pass</b> When this bit is set to one(default), SCL_I2CO and SDA_I2CO are disabled. When this bit is zero, Data/clock can be by-passed</p>
bypass clk pll_m	1 00 2B	32[7] 32[4:0] 33[7:0]	<p><b>Bit 7. By-pass clock</b> When this bit is set to 1, the PLL is bypassed and the external clock signal is directly connected to the internal clock. When this bit is set to 0, the generated clock of the PLL is connected to the internal clock. The default is 1.</p> <p><b>M Divider Ratio</b> This 13 bit value defines a feedback divider with a divider ratio M. Bit 5 of address 25 is the MSB and bit 0 of address 26 is the LSB. The default value is 002Bh</p>
pll_n	01	34[7:0]	<p><b>N Divider Ratio</b> It defines a reference divider with a divider ratio N. The default value is 01h</p>
data_ctrl_sel pll_icp	0 0001	35[5] 35[3:0]	<p><b>Bit 5. Data control select</b> Select the reference signal used to transfer data from HDM8516 to MPEG decoder. When this bit is set to 0, it select "data_valide". When this bit is set to 0, it select "data_stb". In MPEG decoder interface, using one of them. The default is 0.</p> <p><b>Bit [3:0] Charge pump bias current control vector</b> The default value is 1.</p>

**7. REGISTER MAP** (continued)

**7.4 READ REGISTER DESCRIPTION**

Field	Default Value	Register	Description
qs_nbagc_accum		00[7:0]	<b>Narrowband AGC Accumulator</b> The current value of the 8 bit AGC accumulator may be read from this location.
qs_symfreq_acc		01[7:0] 02[7:0] 03[7:0]	<b>Symbol Timing Frequency Accumulator</b> The current value of the 24 bit frequency accumulator in the symbol timing loop filter may be read from these 3 locations.
qs_carphase_acc		04[7:0] 05[7:0] 06[7:0]	<b>Phase Tracking Frequency Accumulator</b> The current value of the 24 bit frequency accumulator in the carrier phase loop filter may be read from these 3 locations.
qs_qpsklock		07[0]	<b>QPSK Lock Flag</b> When this bit is set to one, the QPSK demodulator is phase locked.
qs_wbagcacc		08[7:0]	<b>Wide Band AGC Accumulator</b> This eight bit value represents the most significant bits of the accumulator in the first order wideband AGC loop. This data only has meaning when the wideband AGC is in Mode 0.
qs_swpfreq		09[7:0] 0A[7:0]	<b>Sweep Frequency</b> The 16 bit sweep accumulator is available at this location. Bit 7 of address 09 is the MSB and bit 0 of address 0A is the LSB. The receiver frequency is determined by adding the Sweep Frequency with the carrier frequency accumulator (read addresses 04, 05 and 06) and the nominal carrier start frequency (write addresses 04, 05 and 06).
qs_iout		0B[5:0]	<b>In-Phase</b> The six LSB bit output of the In-phase baseband filter is available at this location. This data is updated once per symbol.
qs_qout		0C[5:0]	<b>Quadrature</b> The six LSB bit output of the quadrature baseband filter is available at this location. This data is updated once per symbol.
qs_noiseplr		0D[5:0]	<b>Noise Power</b> This eight bit output provides a measure of the noise component of the signal when QPSK lock is achieved. Higher numbers correspond to lower signal-to-noise ratio conditions. The quality of this metric is improved if the narrowband AGC is disabled for a minimum of 1000 symbol periods before this parameter is read.
ber_vit		0E[7:0] 0F[7:0]	<b>BER Calculator</b> The current value of the 16bit BER is used to monitor the signal quality or estimate the SNR of incoming signal at the output of Viterbi. Bit 7 of address 0E is the MSB and bit 0 of address 0F is the LSB. It represents the number of errors among $2^{20}$ data bits.

**7. REGISTER MAP** (continued)

**7.4 READ REGISTER DESCRIPTION** (continued)

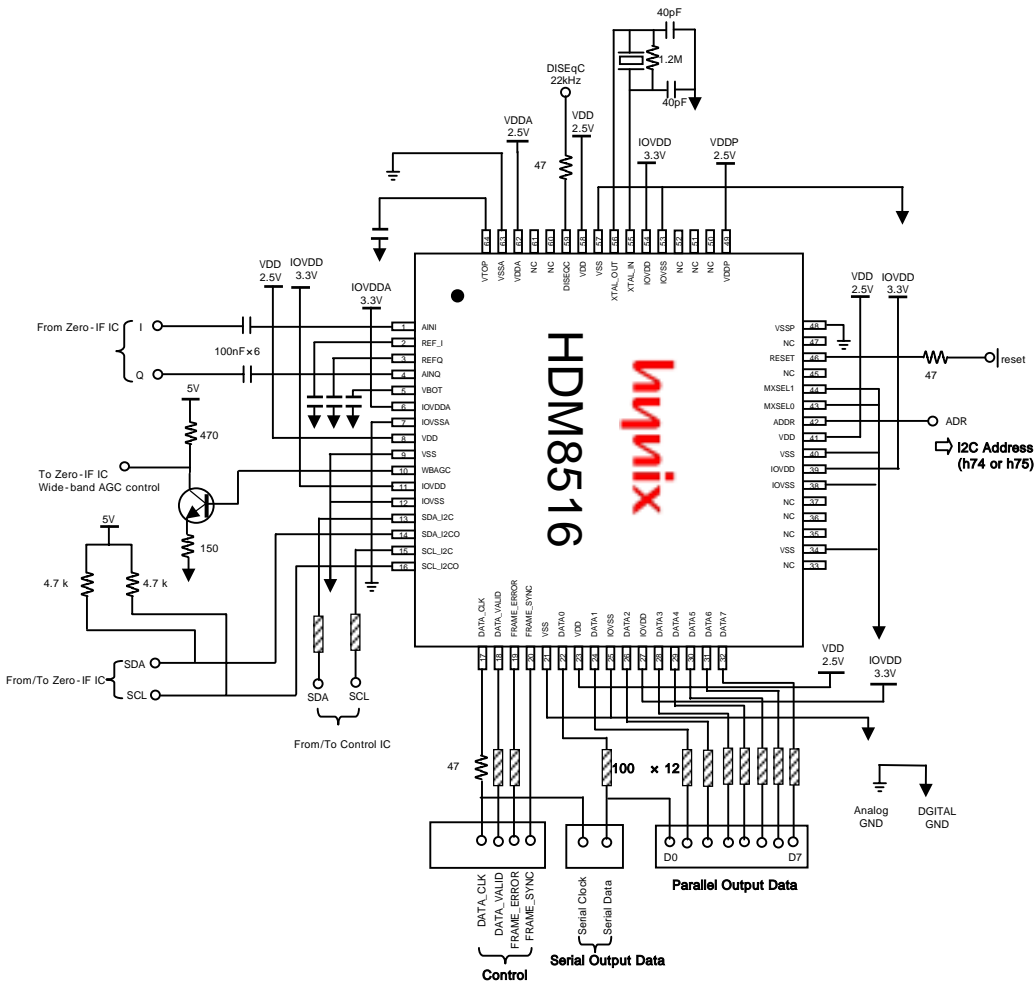
Field	Default Value	Register	Description
qs_carphase1		10[7:0] 11[7:0] 12[7:0]	<b>Carrier Frequency_1</b> This 24 bit value represents the carrier frequency of the first frequency translator.
qs_carphase2		13[7:0] 14[7:0] 15[7:0]	<b>Carrier Frequency_2</b> This 20 bit value represents the carrier frequency of second frequency translator. Bit 7 of address 13 is the MSB and bit 4 of address 15 is the LSB.
sigqlty		16[7:0] 17[7:0] 18[7:0]	<b>Signal Quality</b> This 24 bit signal provides a measure of quality of the signal processed by the Viterbi decoder. This parameter can be used to infer bit error rate and input signal-to-noise ratio for signals which are within a few dB of threshold. Bit 7 of address 16 is the MSB and bit 0 of address 18 is the LSB. The specific definition of this signal for each coding rate is TBD.
vb_coderate		19[2:0]	<b>Viterbi Rate</b> This three bit number represents the code rate of the Viterbi decoder. Rate 1/2    0 Rate 2/3    1 Rate 3/4    2 Rate 5/6    3 Rate 7/8    4
rs_errors		1A[3:0]	<b>Reed Solomon Errors</b> The four bit number at this location indicates the number of errors corrected in the most current block of 188 bytes. This number may range from 0 to 8.
inversion_sig inversion_byte parallel_lock rs_framesync vb_nodesync		1B[4:0]	<b>Bit 4. Pi/2 Ambiguity</b> When this bit is set to one, the Viterbi decoder has successfully resolved pi/2 ambiguity in the input data <b>Bit 3. Pi Ambiguity</b> When this bit is set to one, the Viterbi decoder has successfully resolved pi ambiguity in the input data. (i.e inverted data) <b>Bit 2. Viterbi Byte Sync</b> When this bit is set to one, the Viterbi decoder has successfully established byte-synchronization. <b>Bit 1. Frame Sync</b> When this bit is set to one, the FEC chip has successfully established word sync and frame sync. <b>Bit 0. Viterbi Node Sync</b> When this bit is set to one, the Viterbi decoder has successfully established node synchronization.
count_coted_err		1C[7:0] 1D[7:0]	<b>Accumulated Reed Solomon Errors</b> These two registers present a count of corrected errors since it was last reset. Bit 7 of address 1C is the MSB and bit 0 of address 1D is the LSB. These registers are reset by writing value to address 10H.

**7. REGISTER MAP** (continued)

**7.4 READ REGISTER DESCRIPTION** (continued)

Field	Default Value	Register	Description
count_uncoted_err		1E[7:0]	<b>Accumulated Reed Solomon Data</b> This register presents a count of the uncorrected code words since it was last reset. When it reaches its maximum count(255), it rolls back to zero and starts counting again. This register is reset by writing value to address 10H.
hdm8516 id		1F[7:0]	<b>Device Identifier</b> This register present device identifier. The current value of this register is F1H

## 8. APPLICATION CIRCUIT

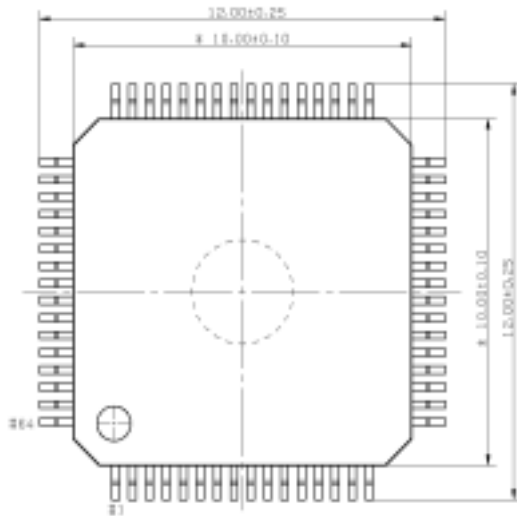


**Note**

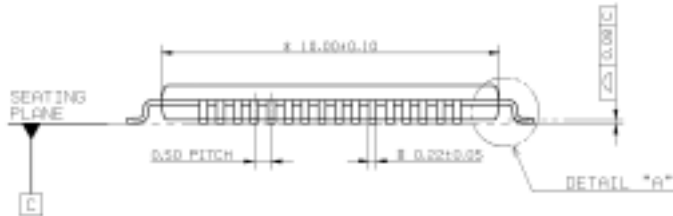
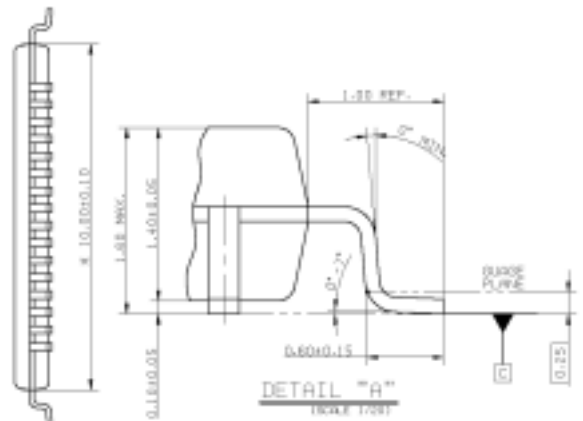
1. Pin Number(64,1,2,3,4,5) Connected Capacitor is 100nF.
2.  $\square$  is 100 Resistor(13,15,18,19,22,24,26,28,29,30,31,32)
3. As MPEG Decoder Interface, Using **DATA\_VALID/DATA\_STB(19)**  
Default value is DATA\_VALID
4. **VDDA(62)** and **VSSA(63)** is ADC power and GND.
5. **IOVDDA(6)** and **IOVSSA(7)** is ADC input PAD power and GND.
6. **Reset(46)** is Active Low Operation.
7. **Xtal\_in(55),Xtal\_out(56)** is Cystal Pad or  
**Xtal\_in(55)** is Clock Pad that input is 4MHz Pulse Signal(Vpp=3.3V)

9. PKG DEMENSION

9.1 64LQFP



NO	REVISION ITEM	DATE	NAME	NO	REVISION ITEM	DATE	NAME
1				5			
2				5			
3				6			



-NOTE-

1. DIMENSION 4 MARK DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE.
2. DIMENSION 8 MARK DOES NOT INCLUDE DAMBER PROTRUSION. ALLOWABLE DAMBER PROTRUSION SHALL BE 2.5mm TOTAL IN EXCESS OF THE 8MARK DIMENSION AT MAXIMUM METERING CONDITION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIIUS OR THE FOOT.
3. UNSPECIFIED IS ACCORDING TO JEDEC MS-026, VARIATION "BCD".

TOLERANCES	SVT	MME	DVE	TITLE	64 LQFP (10, 8010, 8)
UNLESS OTHERWISE SPECIFIED	0R-01			DWG. NO.	64P80-0072
ANGULAR: ±0.5°	02.01	S. D. K. I. H.	01 02 03	REV. NO.	
X : ±0.25	04.01			REV. NO.	
XX : ±0.1	05.01			REV. NO.	
XXX : ±0.05	06.01			REV. NO.	
DATE	1/10	UNIT	mm		